# Optimizing VC7 Performance

The jitter and phase noise performance of a set of output clocks depends upon the exact configuration of the VersaClock® 7 device. Adjacent clock outputs can cross talk. As a result, the choice of crystal frequency and type of dividers can make a difference in performance.

This application note provides suggestions for how to optimize a VC7-based configuration for jitter and phase noise performance.

## Contents

# 1. Crystal Frequency

The crystal frequency provides the reference clock for the APLL. The higher the crystal frequency, the higher the APLL loop bandwidth. A higher loop bandwidth lowers phase noise for a certain part of the phase noise plot. The general recommendation is to select a crystal frequency in the high part of the specified crystal frequency range. The best overall phase noise is achieved with crystal frequencies of 50MHz and higher. In general, lower crystal frequencies are less expensive and can be a compromise to lower cost at the expense of somewhat worse phase noise.

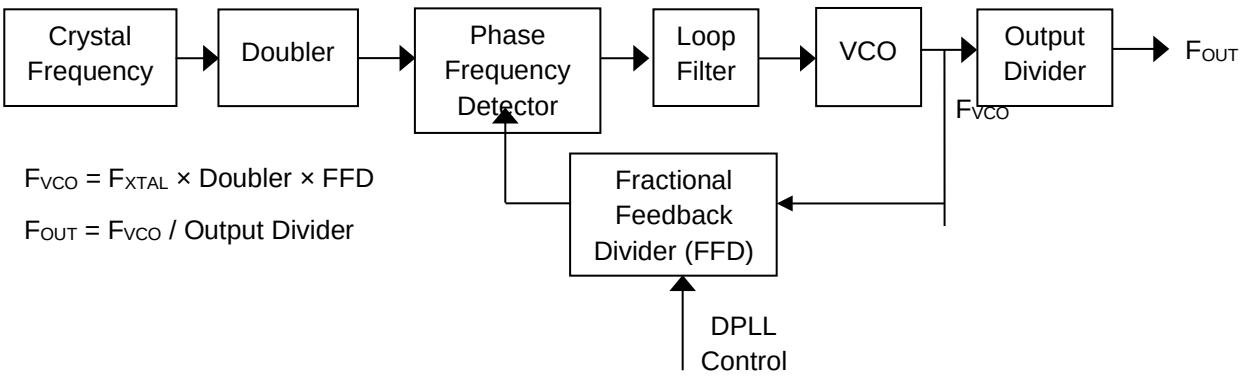


**Figure 1: VersaClock 7 APLL Diagram**

The RC310xx configured as a jitter attenuator is somewhat limited in the choice of crystal frequency. Jitter attenuation mode requires the APLL feedback divider to have a fraction. The DPLL will manipulate the fraction to keep the APLL synchronized to the reference clock. For example, a very popular VCO frequency is 10.000GHz that divides down to a lot of popular clock frequencies like 100MHz and 156.25MHz with integer divider values. Using a 50MHz crystal for this case results in a feedback divider value of 100, which is an integer. This causes issues with the jitter attenuator mode. A better choice is a 60MHz crystal where the feedback divider value is 83.333. The RC310xxAQ devices with integrated crystal have a 68MHz crystal inside to get the best possible performance from the RC310xxAQ for as many as possible popular output clock frequencies.

The RC210xx synthesizer prefers integer values for the feedback divider for the best phase noise. When the VCO is 10.000GHz, a 50MHz crystal will be good. Even better is a 62.5MHz crystal. The best is a 78.125MHz crystal and for this reason the RC210xxAQ with integrated crystal uses a 78.125MHz crystal.

# 2. Divider Values and Types

Integer divider values are better for phase noise than fractional values. Even better is a dedicated integer divider. In general, the simpler the better for noise. To divide down from the VCO frequency in the APLL to an output, there are four integer dividers (IODs) available and three fractional dividers (FODs). The APLL block has a fractional feedback divider.

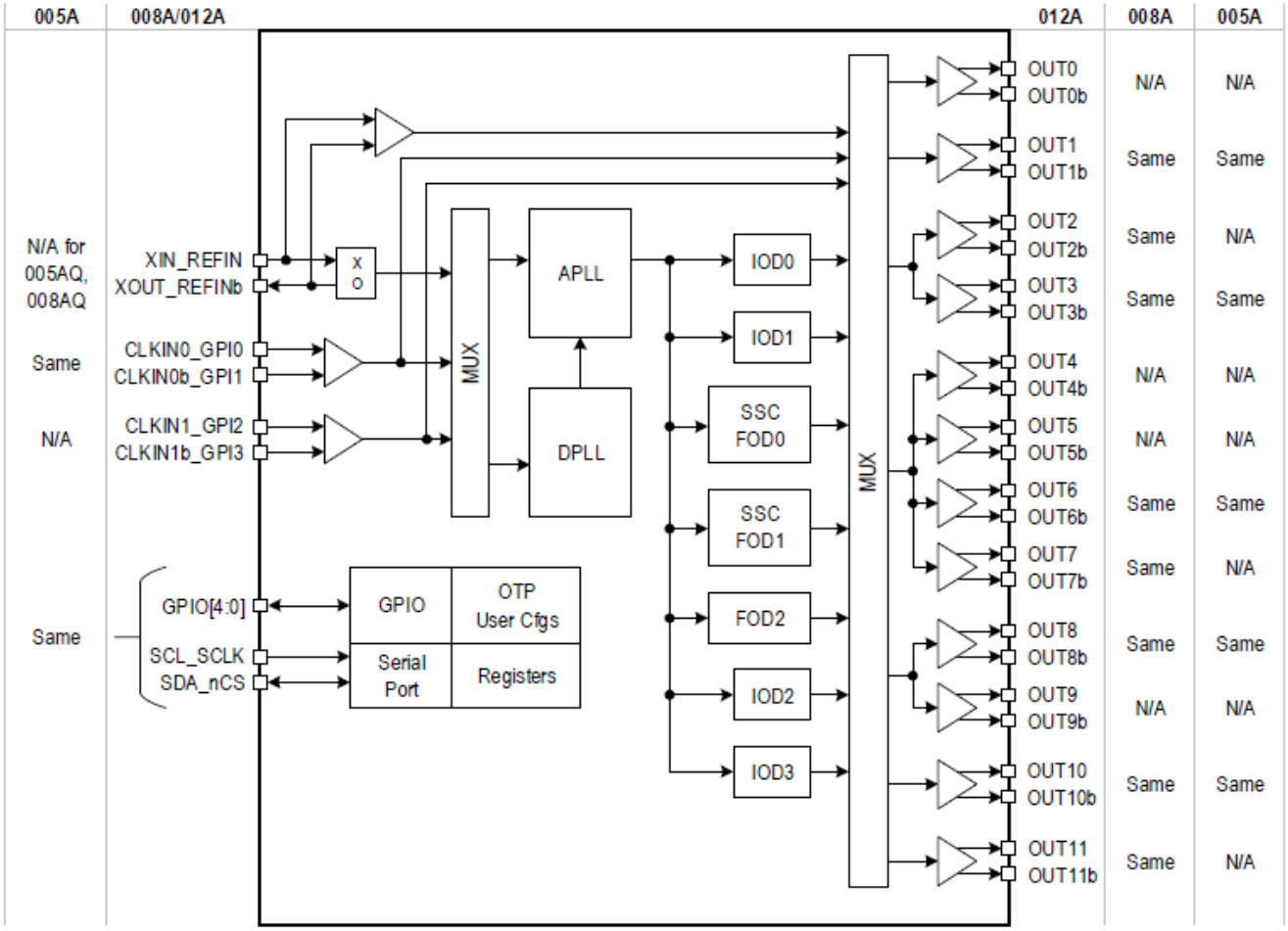


**Figure 2: VersaClock 7 Block Diagram**

The crystal to output frequency synthesis works with the following formulas:

- $F_{OUT} = F_{VCO} / OD$ → OD is the output divider and can be either an IOD or a FOD. Please note that $F_{VCO}$ has a limited range of 9.5GHz to 10.7GHz.
- $F_{VCO} = F_{XTAL} \times Doubler \times FFD$ → FFD is the Fractional Feedback Divider. Doubler is 2 when enabled and 1 when disabled.

Identify the output clocks that require the best phase noise or jitter and try to find a solution that uses integer divider values as much as possible.

Example:

Let's say we have 100MHz clocks for PCIe, 156.25MHz clocks for Ethernet, a 50MHz processor clock and 24MHz for USB. Ethernet will be the most demanding, closely followed by PCIe and then USB. The processor clock would be the least critical regarding phase noise and jitter performance. A VCO frequency of 10.000GHz would result in integer output divider values for 156.25MHz (IOD = 64), 100MHz (IOD = 100) and 50MHz (200). Dividing 10GHz by 24MHz makes an output divider value of 416.667 so this needs to be a FOD. Because 156.25MHz and 100MHz are the most critical, the best choice is an IOD. The 50MHz processor clock is not very critical so it can be either IOD or FOD and we can use whatever is left after allocating dividers for the other clocks. The 24MHz USB clock requires a FOD because of the fractional divider value.

Fractions:

Avoid fractions in a divider value that are too close to the integer value. In general, avoid fractions smaller than 0.1 and larger than 0.9. With a fraction like this, a harmonic of the frequency at the FFD output will be close to the frequency at the FFD input and cause a bead note or "spur". More about spurs is provided in the following

section. The example above with the 60MHz crystal and 10GHz VCO that results in a FFD of 83.333 is very good with a 0.333 fraction.

# 3. Allocating Output Clocks

Phase noise performance can be spoiled by cross-talk between outputs and to a lesser extend between crystal and outputs. A simple example is a 100MHz clock and a 101MHz clock. When measuring phase noise, the noise level is measured at an offset range off the carrier frequency. When measuring the 100MHz clock and a little bit of the 101MHz clock cross-talks into the 100MHz clock, the phase noise analyzer will detect the cross-talk at a 1MHz offset. It will show up as a spike in the plot, also known as a “spur”. Spurs can significantly contribute to overall jitter. For this example, it is obviously a bad idea to place the 100MHz clock and 101MHz clock side by side. Plan at least one different clock or perhaps unused output between the 100MHz and 101MHz clocks so there is a physical distance between the interfering clocks.

Clocks are square waves and consist of a sequence of harmonics. For example, the 3rd harmonic of a 33.333MHz clock is 100MHz and will also cross-talk to a 101MHz clock as described above. Harmonics are less powerful than the carrier so a spur from a harmonic will be less strong.

In VersaClock 7, outputs are grouped into clock banks. Each clock bank uses one of the output dividers – an IOD (Integer Output Divider) or an FOD (Fractional Output Divider) – to generate intended frequencies. Different output dividers are available to different clock banks. The table below shows clock banks and output dividers versus each output.

| Banks | Output Dividers Available to the Bank | Outputs | Notes |
|---|---|---|---|
| Bank0 | IOD0, IOD1, FOD0, FOD1 | OUT0/OUT0b | Available only in 12-output variant devices. |
| Bank1 | IOD0, IOD1, FOD0, FOD1 | OUT1/OUT1b | Available in 5-, 8- and 12-output variant devices. |
| Bank2 | IOD1, FOD0, FOD1 | OUT2/OUT2b, OUT3/OUT3b | Available in 5-, 8- and 12-output variant devices (5-output devices only has OUT2/OUT2b). |
| Bank3 | FOD0, FOD1, FOD2 | OUT4/OUT4b, OUT5/OUT5b, OUT6/OUT6b, OUT7/OUT7b | Available in 5-, 8- and 12-output variant devices (5-output devices only has OUT6/OUT6b, 8-output devices have OUT6/OUT6b and OUT7/OUT7b). |
| Bank4 | IOD2, FOD1, FOD2, CLKIN0, CLKIN1 | OUT8/OUT8b, OUT9/OUT9b | Available in 5-, 8- and 12-output variant devices (5- and 8-output devices only has OUT8/OUT8b). |
| Bank5 | IOD2, IOD3, FOD1, FOD2, CLKIN0, CLKIN1, XIN_REFIN | OUT10/OUT10b | Available in 5-, 8- and 12-output variant devices |
| Bank6 | IOD2, IOD3, FOD1, FOD2, CLKIN0, CLKIN1 | OUT11/OUT11b | Available in 8- and 12-output variant devices. |

When allocating output frequencies, be aware that multiple outputs from a bank will have the same frequency. With this information, let’s look at the example in section 2 again with the 156.25MHz, 100MHz, 50MHz and 24MHz clocks. The 3rd harmonic of 50MHz is at only 6.25MHz distance from 156.25MHz and there could be a 6.25MHz spur. It is recommended to have some distance between the 50MHz clock and the 156.25MHz clocks. The 4th harmonic of 24MHz is at only 4MHz distance from 100MHz, so it is recommended to have some distance between the 24MHz and 100MHz clocks. Allocating 50MHz and 100MHz side-by-side is acceptable because this is a perfect X2.

Combining the recommendations in section 2 and section 3, the allocation of output clocks for a RC21008 can be as follows:

- OUT1 (Bank1) = 24MHz
- OUT2 (Bank2) is disabled
- OUT3 (Bank 2) = 50MHz
- OUT6 (Bank 3) = 100MHz
- OUT7 (Bank 3) = 100MHz
- OUT8 (Bank 4) = 100MHz
- OUT10 (Bank 5) = 156.25MHz
- OUT11 (Bank 6)= 156.25MHz

In this example, Bank3 and Bank4 need to generate the same frequency so they can use the same output divider (FOD1). However, keep in mind that IOD will generate cleaner clocks than FOD, but Bank3 can only access FOD. Thus, the best trade-off in this case would be Bank3 selects FOD1, Bank4 selects IOD2.

Grouping outputs of the same frequency together will not only reduce noise cross-talk thus reducing possible spurs in phase noise, but simplify power supply filtering. VDDO rails supplying outputs of the same frequency can be combined while VDDO rails supplying output of different frequencies are recommended to have separate filtering circuits.

This could be a RC21008AQ with integrated 78.125MHz crystal. In case of a RC21008 with external crystal, a good choice would be a 62.5MHz crystal. None of the harmonics of 62.5MHz will be near 100MHz or 156.25MHz. A 50MHz crystal risks 6.25MHz spurs in the 156.25MHz clocks from its 3$^{rd}$ harmonic so a 50MHz crystal is less suited.

# 4. PCB Design

The PCB design around the VersaClock 7 circuit can affect the phase noise and jitter performance significantly. Clock traces can cross-talk when running in parallel for a certain distance. This is difficult to avoid for adjacent outputs. Clock traces that run at the PCB surface are called Micro Strips, and clock traces that are sandwiched between ground layers inside the PCB are called Strip-lines. Strip-lines cross-talk about 20dB less for the same distance and same length they run parallel. For the most critical clocks it is recommended to use Strip-lines. Calculators can be found online for calculating the cross-talk between parallel traces of both types.

Power supply filtering and bypassing can also play a role in cross-talk between outputs. An output driver can cause ripple on its VDDO pin. When that ripple is transferred to another VDDO it can mix with that other clock and cause a spur in the phase noise. Bypassing minimizes the ripple amplitude and filtering prevents that ripple from moving between VDDOs. VDDOs for outputs with the same frequency can be grouped together and connected to a VDD rail or VDD plane through a ferrite bead. This is done to prevent ripple of that frequency from transferring to the VDD rail or VDD plane and from there transfer to other VDDOs or perhaps other devices. Ferrite beads are also useful for preventing noise on the VDD rail or VDD plane from other devices to interfere with the VersaClock 7. For more information about power supply filtering, see the reference schematic for the VersaClock 7.

A few notes about bypassing of VDD pins:

- Each VDD pin needs its own bypass capacitor.
- A popular bypass capacitor value is 0.1μF. The value is actually less important than the RF properties of the capacitor. It is important that the bypass capacitor is a very low impedance for clock frequencies and their harmonics. With improvements in capacitor dielectric materials, it is possible to use larger values like 1μF. There are also special low inductance capacitors available that have the terminals on the long side so the distance through the capacitor is shorter. Distance equals inductance and the same is true for PCB traces. Position the bypass capacitor as close as possible to the VDD pin.

- Route from the VDD pin to the bypass capacitor first and from there route to the ferrite bead or perhaps a VDD rail. This is important to bypass (short) ripple from the VDD pin before it reaches the VDD rail.
- The ground side of a bypass capacitor usually connects to a ground plane through one or more vias. Do not share ground vias with other circuits or other bypass capacitors because this would be an easy path for ripple to pass between circuits. Each bypass capacitor needs to have its own via or multiple vias to ground.

A few notes about the PCB layout around the crystal:

- The crystal can be both a source of interference and be a sensitive point where interference enters the VersaClock 7.
- Place the crystal as close as possible to the crystal pins on the VersaClock 7 so the traces to the crystal are as short as possible.
- Remove the first ground plane underneath the crystal circuit to minimize parasitic capacitance to ground.
- The proper matching load capacitance for the crystal can be programmed in the VersaClock 7 so external capacitors on the crystal pins are not needed. When using external capacitors, these capacitors connect to the ground plane at some distance from the chip and pick up noise. It is recommended to use the on-chip programmable load capacitance to avoid this potential source of interference.

# 5. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.01 | May 23, 2023 | Updated section 3, Allocating Output Clocks. |
| 1.00 | Jun 2, 2022 | Initial release. |

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