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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of Watchdog Timer (watchdog timer interrupt)

1.0 Abstract

The following is an operation of the watchdog timer using watchdog timer interrupt.

2.0 Introduction

Operation (1) Writing to the watchdog timer start register initializes the watchdog timer to $7FFF_{16}$ and causes it to start a down count.

(2) With a count in progress, writing to the watchdog timer start register again initializes the watchdog timer to $7FFF_{16}$ and causes it to resume counting.

(3) Either executing the WAIT instruction or going to the stopped state causes the watchdog timer to hold the count in progress and to stop counting. The watchdog timer resumes counting after returning from the execution of the WAIT instruction or from the stopped state.

(4) If the watchdog timer underflows, it is initialized to $7FFF_{16}$ and continues counting. At this time, a watchdog timer interrupt occurs.

Figure 1 shows the operation timing.

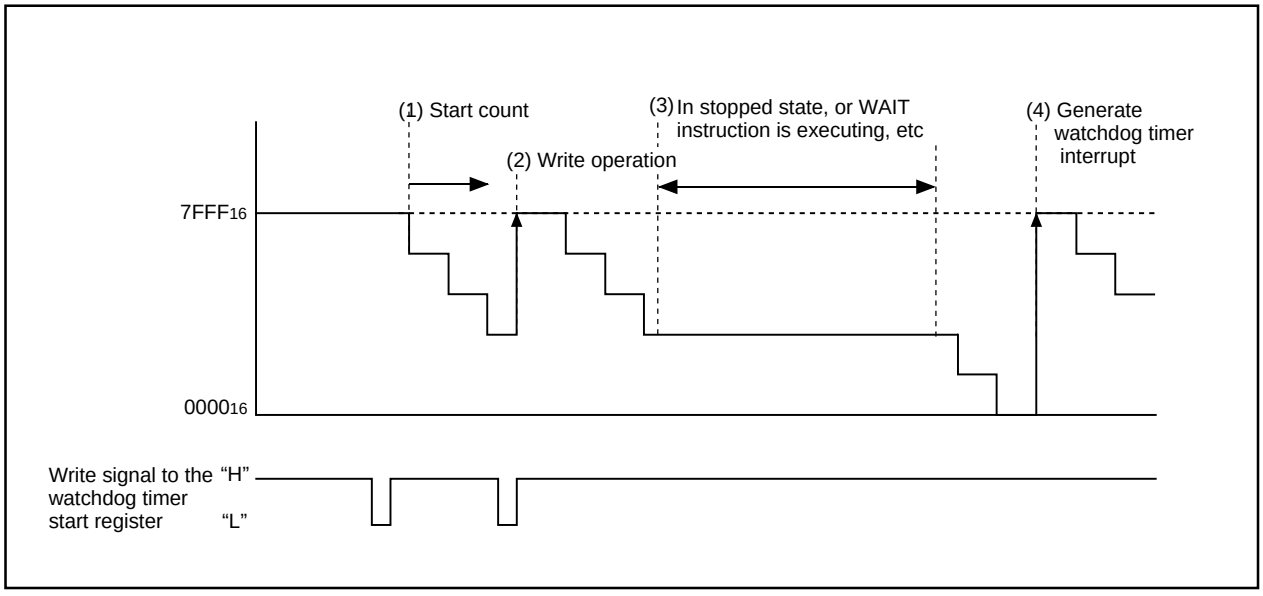
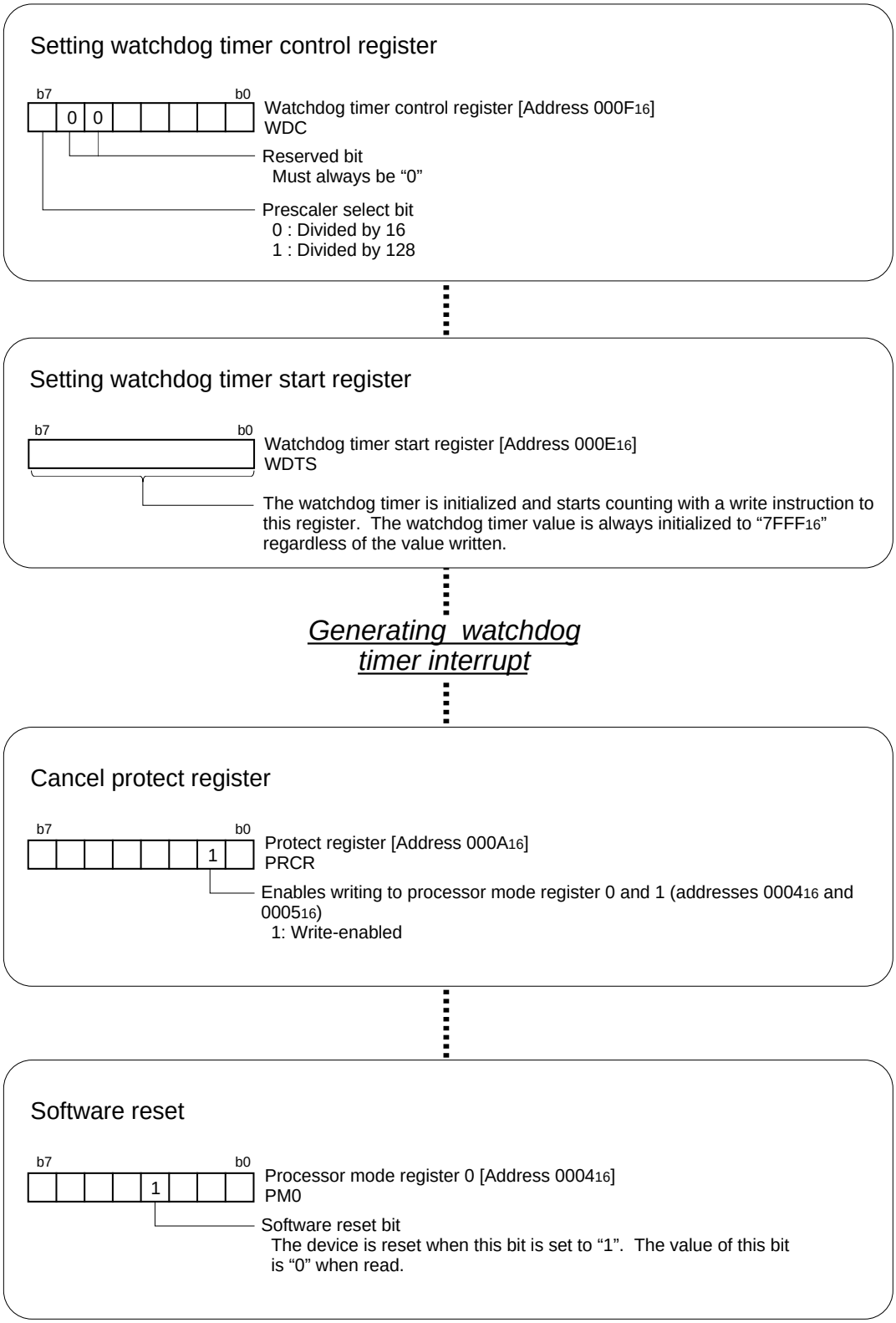


Figure 1. Operation timing of watchdog timer (watchdog timer interrupt)

3.0 Set-up procedure



4.0 Programming Code

```
;*****************************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0492_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of Watchdog Timer
;               (watchdog timer interrupt)
;   HISTORY   : 2004.03.15  Ver 1.00
;
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;
;*****************************************************************************************
;*****************************************************************************************
;       Include
;*****************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;*****************************************************************************************
;       Symbol definition
;*****************************************************************************************
RAM_TOP         .EQU    000400H     ;Start address of RAM
RAM_END         .EQU    002BFFH     ;End address of RAM
ROM_TOP         .EQU    0FFC000H    ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFFDCH    ;Start address of fixed vector
;
;*****************************************************************************************
;       Program area
;*****************************************************************************************
;=========================================================================
;       Start up
;=========================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        LDC      #RAM_END+1, ISP   ;Sets initial value in stack pointer
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr        ;Removes protect
        MOV.B    #10000000B, pm0   ; Single-chip mode
        MOV.B    #11000000B, pm1   ; Flash memory version
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High
        MOV.B    #00010010B, mcd   ; No division mode
        MOV.B    #00H, prcr        ;Protects all registers
;
;=========================================================================
;       Watchdog timer (watchdog timer interrupt)
;=========================================================================
        ; Setting watchdog timer control register
        MOV.B    #10000000B,wdc
;                |++-------------;Reserved bit (Must always be "0")
;                +---------------;Prescaler select bit(1:Divided by 128)
                                 ;(WDT cycle Approx. 209.7msec Xin=@20MHz)
        ; When Xin is selected in BCLK
        ;   Watchdog timer cycle = Prescaler division ratio(16 or 128) * watchdog timer count(32768) / BCLK
        ; When Xcin is selected in BCLK
        ;   Watchdog timer cycle = Prescaler division ratio(2) * watchdog timer count(32768) / BCLK
;
        ; Setting watchdog timer start register
        MOV.B    #1, wdts
;                +---------------;The watchdog timer is initialized and starts counting
                                 ;with a write instruction to this register.
                                 ;The watchdog timer value is always initialized to "7FFFh"
                                 ;regardless of the value written.
;
```

```
MAIN:
        ; In the application program, write to the watchdog timer start register before
        ; the watchdog timer underflows.
        ; (ex)
        ; MOV.B    #1, wdts

        ; With a count in progress,
        ; writing to the watchdog timer start register again
        ; initializes the watchdog timer and causes it to resume counting.
        ;
        ; When the watchdog timer underflows, a watchdog timer interrupt occurs.
        JMP      MAIN
;
;=============================================================================
;       Interrupt program
;=============================================================================
;-----------------------------------------------------------------------------
;       WDT interrupt occur (Detect a runaway program)
;-----------------------------------------------------------------------------
INT_WDT:
        ; Cancel protect register
        MOV.B    #02H, prcr    ;Clear the protect
;                  +----------;Enables writing to processor mode registers 0 and 1
RS_LOOP:
        ; Software reset
        BSET     pm03
        JMP      INT_WDT
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*****************************************************************************
;       Setting of fixed vector
;*****************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    INT_WDT  ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

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E-mail: support_apl@renesas.com

Data Sheet

M16C/80 group Rev. E3

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