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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of Serial I/O (transmission used for SIM interface)

1.0 Abstract

In transmitting data in UART mode (used for SIM interface), choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chooosed functions

Item	Set-up	
Transfer data format	○	Direct format
		Inverse format

2.0 Introduction

- Operation
- (1) Setting the transmit enable bit and receive enable bit to "1" and writing transmission data to the UART2 transmit buffer register readies the data transmissible status. Set UART2 transfer interrupt is enabled.
 - (2) Transmission data held in the UART2 transmit buffer register is transmitted to the UART2 transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the TxD2 pin. Then, data is transmitted, bit by bit, in sequence: LSB, ..., MSB, parity bit, and stop bit(s).
 - (3) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to "1", which indicates that transmission is completed. At this time, the UART2 transmit interrupt request bit goes to "1". The transfer clock stops at "H" level.
 - (4) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.
 - (5) If a parity error occurs, an L is output from the SIM card, and the RxD2 terminal turns to the "L" level. Check the RxD2 terminal's level within the UART2 transmission interrupt routine, and if it is found to be at the "L" level, then handle the error.

Note

- The parity error level is determined within a UART2 transmission interrupt. When a transmission interrupt request occurs, set the priority level of the transmission interrupt higher than those of other interrupts so that the interrupt routine can be immediately carried out. Either in the main routine or in an interrupt routine, the interrupt inhibition time has to be made as short as possible.
- Set the RxD2 terminal's direction register to input.

Figure 1 shows the operation timing

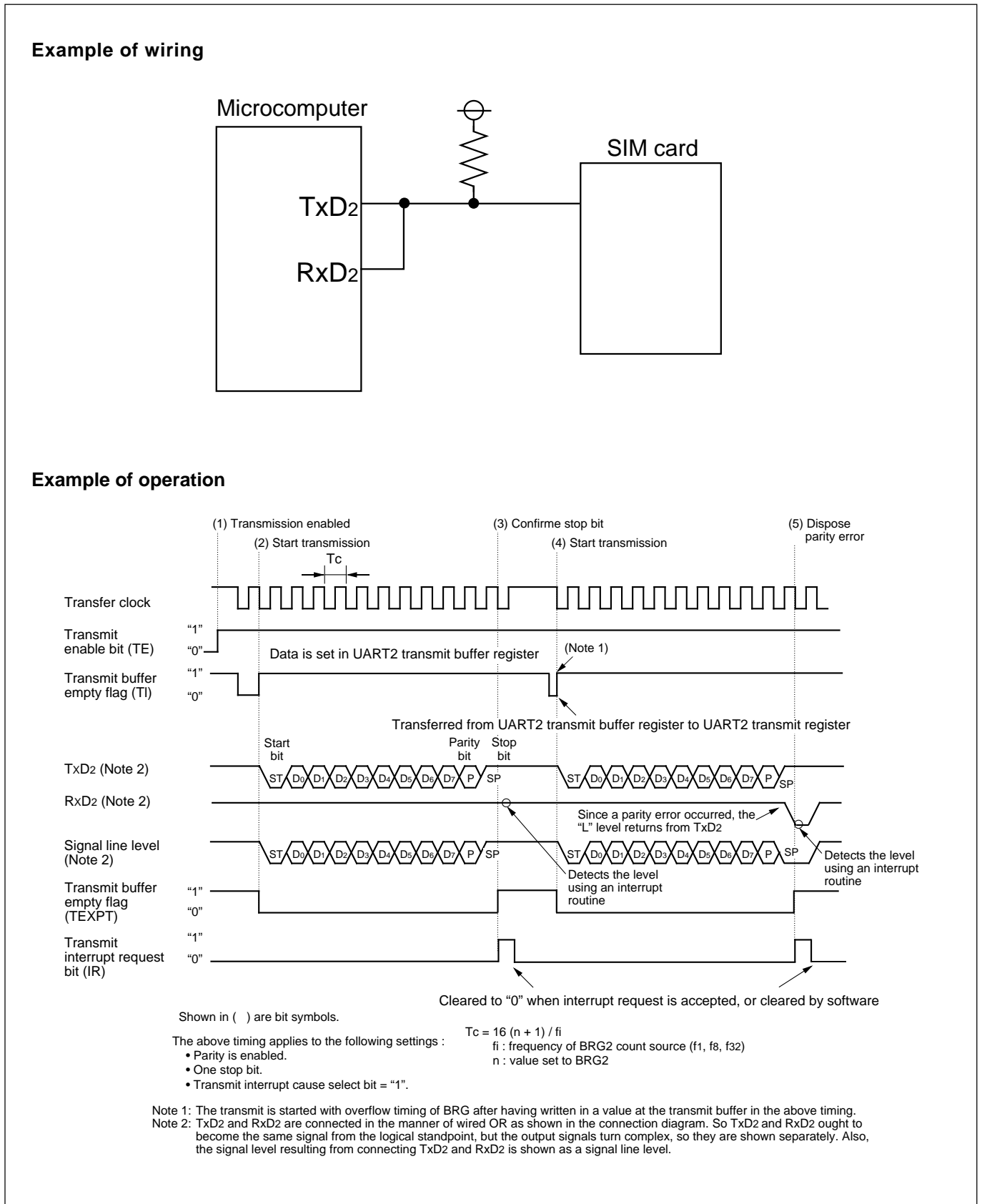
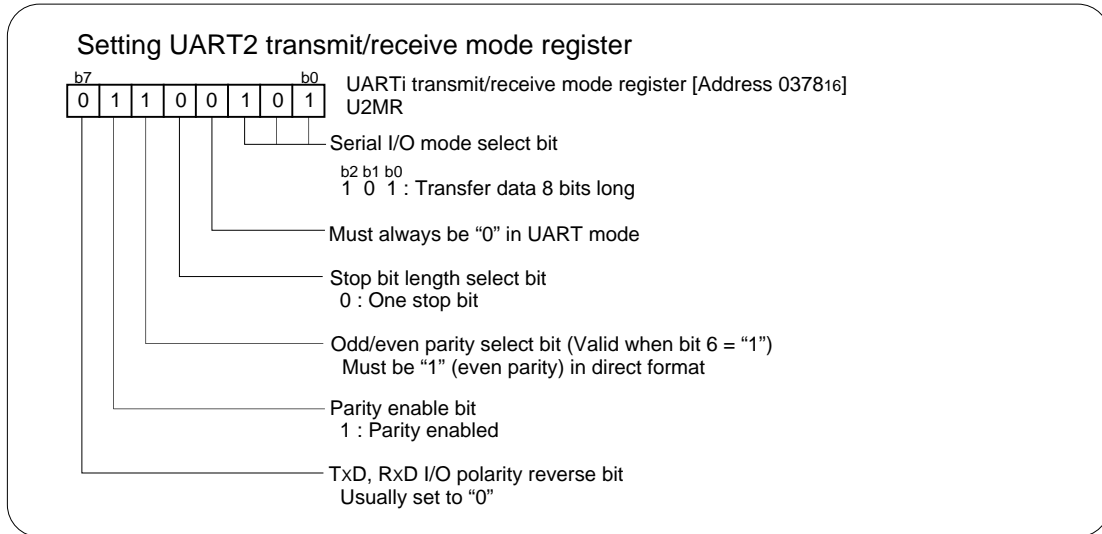
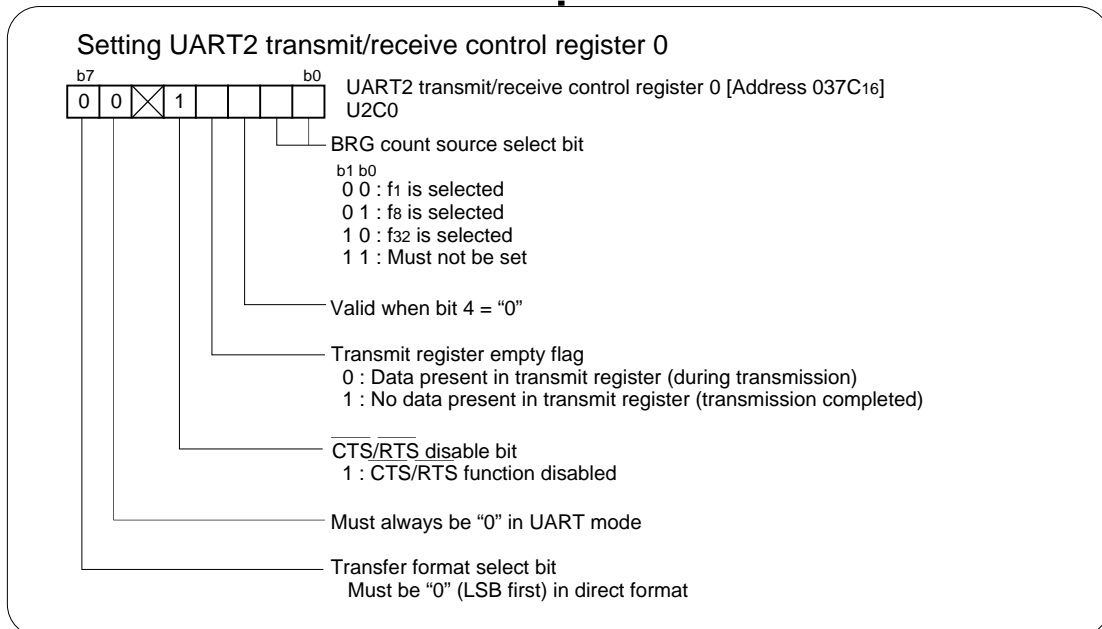


Figure 1. Operation timing of transmission in UART mode (used for SIM interface)

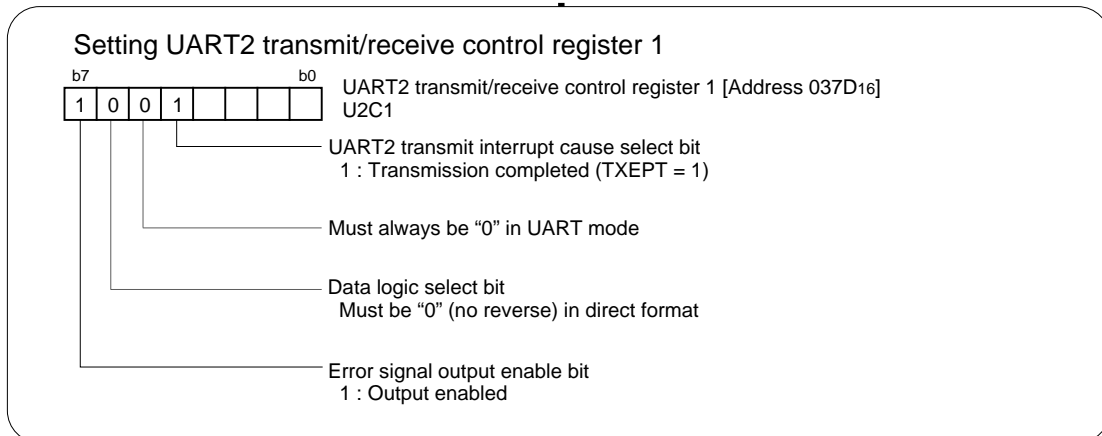
3.0 Set-up procedure



⋮



⋮

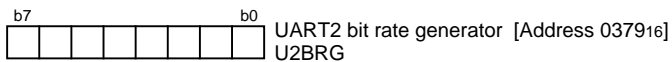


⋮

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Setting UART2 bit rate generator



Can be set to 00₁₆ to FF₁₆ (Note)

Note: Write to UARTi bit rate generator when transmission/reception is halted.

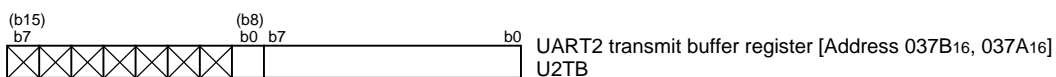
Transmit enabled



Transmit enable bit
1 : Transmission enabled

Receive enable bit
1 : Reception enabled

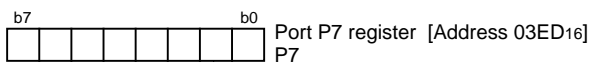
Writing transmit data



Setting transmission data

UART2 transmit interrupt

Confirm RxD2 pin level



Port P7₁ register
0 : "L" level
1 : "H" level

REIT instruction

4.0 Programming Code

```

;*****
;
; M16C/62A Program Collection
;
; FILE NAME : rjj05b0050_src.a30
; CPU      : M16C/62A Group
; FUNCTION  : Operation of Serial I/O
;            (transmission used for SIM interface)
; HISTORY  : 2003.05.16 Ver 1.00
;
; Copyright(C)2003, Renesas Technology Corp.
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; All rights reserved.
;
;*****
;*****
; Include
;*****
        .LIST      OFF          ;Stops outputting lines to the assembler list file
        .INCLUDE   sfr62a.inc   ;Reads the file that defined SFR
        .LIST      ON          ;Starts outputting lines to the assembler list file
;
;*****
; Symbol definition
;*****
RAM_TOP      .EQU    00400H    ;Start address of RAM
RAM_END      .EQU    00FFFH    ;End address of RAM
ROM_TOP      .EQU    0F8000H   ;Start address of ROM
VECT_TOP     .EQU    0FFE00H   ;Start address of variable vector
FIXED_VECT_TOP .EQU    0FFFDCH  ;Start address of fixed vector
;
;*****
; Allocation of work RAM area
;*****
        .SECTION   WORKRAM, DATA
        .ORG      RAM_TOP
WORKRAM_TOP:
C_POWER      .EQU    3
C_DATA_SIZE  .EQU    (1<< C_POWER) ;Data size
v_Trans_data: .BLKB  C_DATA_SIZE  ;Area of send data for sample
WORKRAM_END:
;
;*****
; Program area
;*****
;=====
; Start up
;=====
        .SECTION   PROGRAM, CODE ;Declares section name and section type
        .ORG      ROM_TOP       ;Declares start address
RESET:
        LDC      #RAM_END+1, ISP ;Sets initial value in stack pointer
        MOV.B   #03H, prcr      ;Removes protect
                                ;Set processor mode registers 0 and 1
        MOV.B   #00000000B, pm0 ; Single-chip mode
        MOV.B   #00000000B, pm1 ; No expansion, No wait
                                ;Set system clock control registers 0 and 1
        MOV.B   #00001000B, cm0 ; Xcin-Xcout High
        MOV.B   #00100000B, cm1 ; Xin-Xout High, Main clock is No divison
        MOV.B   #00H, prcr      ;Protects all registers
        LDINTB  #VECT_TOP       ;Sets initial value in interrupt table register
;

```

```

; Clears WORKRAM area
MOV.W  #0, R0
MOV.W  #(RAM_END-RAM_TOP)/2, R3
MOV.W  #WORKRAM_TOP, A1
SSTR.W

; Makes transmit data for sample ( 1 to C_DATA_SIZE )
MOV.B  #1, R0L ;1st data
MOV.W  #0, A0 ;Initialize offset address
MAKE_DATA:
MOV.B  R0L, v_Trans_data[A0] ;
ADD.B  #1, R0L ;
ADD.W  #1, A0 ;
CMP.W  #C_DATA_SIZE, A0 ;
JLTU  MAKE_DATA ;
;
;=====
; Serial I/O (transmission used for SIM interface)
;=====
MOV.B  #00H, s2tic ;Initializes interrupt priority level (Disables interrupt)
;
BCLR  pd7_1 ;Set the RxD2 terminal's direction register to input
MOV.B  #01100101B, u2mr ;Setting UART2 transmit/receive mode register
;
; ||| |+++-----;Serial I/O mode select bit (transfer data 8 bits long)
; ||| |+-----;Must always be "0" in UART mode
; ||| |+-----;Stop bit length select bit (0:One stop bit)
; ||+-----;Odd/even parity select bit (Valid when bit 6 = "1")
; || Must be "1" (even parity) in direct format
; |+-----;Parity enabled
; +-----;TxD,RxD I/O polarity reverse bit (Usually set to "0")
MOV.B  #00010000B, u2c0 ;Setting UART2 transmit/receive control register 0
;
; || | |++-----;BRG count source select bit (00:f1 is selected)
; || | |+-----;CTS/RTS function select bit (Valid when bit 4="0")
; || |+-----;Transmit register empty flag
; || +-----;CTS/RTS function disabled
; |+-----;Must always be "0" in UART mode
; +-----;Must be "0" (LSB first) in direct format
MOV.B  #10010000B, u2c1 ;Setting UART2 transmit/receive control register 1
;
; || |+-----;UART2 transmit interrupt cause select bit
; || (1:Transmission completed(TXEPT=1))
; |+-----;Must always be "0" in UART mode
; |+-----;Data logic select bit
; | Must be "0" (no reverse) in direct format
; +-----;Error signal output enabled bit (1:Output enabled)
MOV.B  #92, u2brg ;Setting UART2 bit rate generator
;
MOV.B  #07H, s2tic ;Set the priority level of the transmission interrupt
; (Set the priority level of the transmission interrupt
; higher than those of other interrupts)
MOV.B  #10010101B, u2c1 ;Transmit enabled
;
; | +-----;Transmission enabled
; +-----;Reception enabled
FSET  I
;

```



```

;=====
;   Main program
;=====
        MOV.W   #0, A0           ;Initializes offset
WRITE_DATA:
        MOV.B   v_Trans_data[A0], u2tb;Writing transmit data
;
WAIT_TRANS:
        BTST    txept_u2c0       ;(ex.)
        JZ      WAIT_TRANS      ;Checking the status of transmit register empty flag
;
PREPARE_NEXT_DATA:
        ADD.W   #1, A0
        AND.W   #(C_DATA_SIZE-1), A0
        JNZ    WRITE_DATA
;
COMPLETE_TRANS:
        JMP     COMPLETE_TRANS
;
;=====
;   Interrupt program
;=====
INT_UART2T:
; Check RxD2 pin (Port P71) level.
; If a parity error occurs, an L is output from the SIM card, and
; the RxD2 terminal turns to the "L" level.
; Check the RxD2 terminal's level within the UART2 transmission interrupt routine,
; and if it is found to be at the "L" level, then handle the error.
;
; Either in the main routine or in an interrupt routine, the interrupt inhibition time
; has to be made as short as possible.
        REIT
;
;=====
;   Dummy interrupt processing program
;=====
dummy:
        REIT
;
;*****
;   Setting of variable vector table
;*****
        .SECTION    VECT, ROMDATA
        .ORG        VECT_TOP+(15*4)
;
        .LWORD     INT_UART2T    ;UART2 transmit/NACK interrupt vector
        .LWORD     dummy         ;UART2 receive/ACK interrupt vector
        .LWORD     dummy         ;UART0 transmit/NACK interrupt vector
        .LWORD     dummy         ;UART0 receive/ACK interrupt vector
        .LWORD     dummy         ;UART1 transmit/NACK interrupt vector
        .LWORD     dummy         ;UART1 receive/ACK interrupt vector
;

```

```
*****
;
;   Setting of fixed vector
;*****
.SECTION    F_VECT, ROMDATA
.ORG       FIXED_VECT_TOP
;
.LWORD     dummy      ;Undefined instruction interrupt vector
.LWORD     dummy      ;Overflow (INT0 instruction) interrupt vector
.LWORD     dummy      ;BRK instruction interrupt vector
.LWORD     dummy      ;Address match interrupt vector
.LWORD     dummy      ;Single-step interrupt vector
.LWORD     dummy      ;Watchdog timer interrupt vector
.LWORD     dummy      ;DBC interrupt vector
.LWORD     dummy      ;NMI interrupt vector
.LWORD     RESET      ;Sets reset vector
;
.END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

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Data Sheet

M16C/62A group Rev. C.1

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User's Manual

M16C/62A group Rev. 1.0

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