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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of Serial I/O (transmission in UART mode)

1.0 Abstract

In transmitting data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosed functions

Item	Set-up		Item	Set-up	
Transfer clock source (Note 2)	<input type="radio"/>	Internal clock (f ₁ / f ₈ / f ₃₂)	Sleep mode (Note 2)	<input type="radio"/>	Sleep mode off
		External clock (CLKi pin)			Sleep mode selected
CTS function	<input type="radio"/>	CTS function enabled	Data logic select function (Note 3)	<input type="radio"/>	No reverse
		CTS function disabled			Reverse
Transmission interrupt factor		Transmission buffer empty	TxD, RxD I/O polarity reverse bit (Note 3)	<input type="radio"/>	No reverse
	<input type="radio"/>	Transmission complete			Reverse
CTS / RTS separation function (Note 1)	<input type="radio"/>	Pin shared by CTS and RTS	Bus collision detection function (Note 3)	<input type="radio"/>	Not selected
		CTS and RTS separate			Selected

Note 1: UART0 only. (UART1 CTS/RTS function cannot be used when this function is selected.)

Note 2: UART0, UART1 only.

Note 3: UART2 to UART4 only.

2.0 Introduction

Operation (1) Setting the transmit enable bit to "1" and writing transmission data to the UARTi transmit buffer register readies the data transmissible status.

(2) When input to the CTSi pin goes to "L", transmission starts (the CTSi pin needs to be controlled on the reception side).

(3) Transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the TxDi pin. Then, data is transmitted, bit by bit, in sequence: LSB, ..., MSB, parity bit, and stop bit(s).

(4) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to "1", which indicates that transmission is completed. At this time, the UARTi transmit interrupt request bit goes to "1". The transfer clock stops at "H" level.

(5) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.

- Note
- Select TxDi output with the function select register A and B.
 - Set CTSi pin's function select register A to I/O port and port direction register to "0".
 - When setting the function select registers A, B, and C, sets the function select registers B and/or C first, and then sets the function select register A.

Figure 1 shows the operation timing

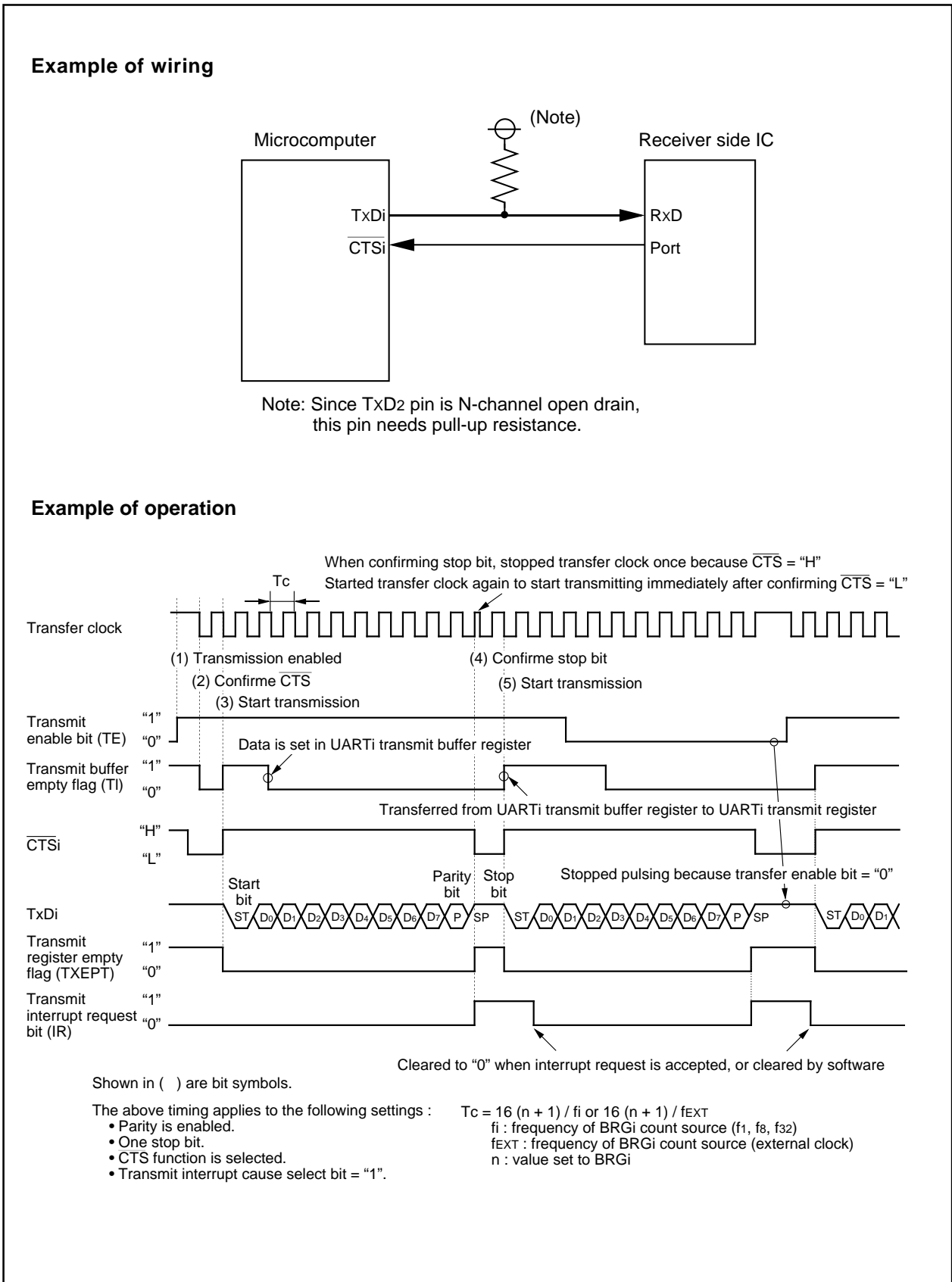
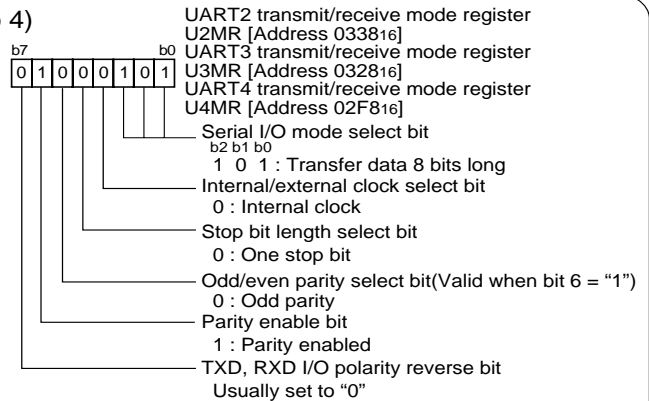
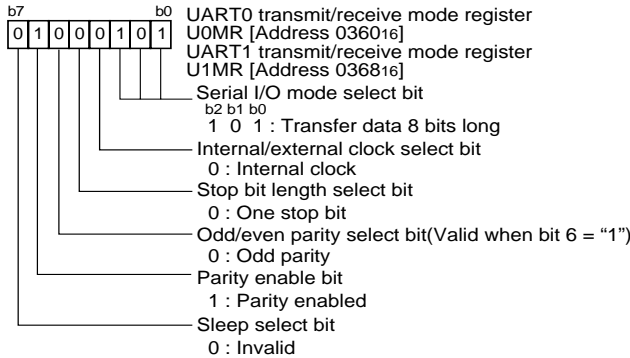


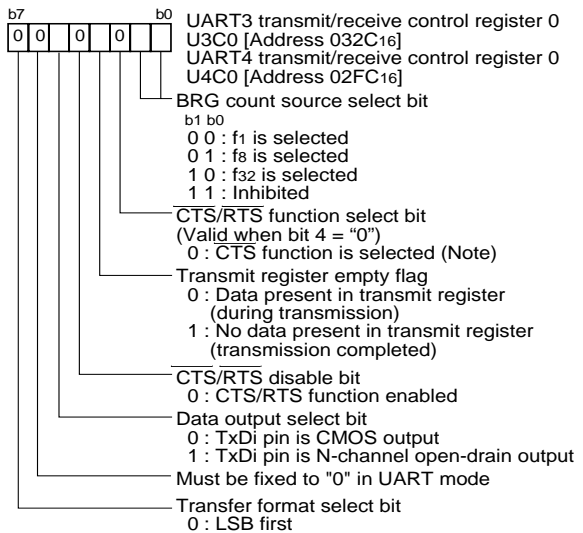
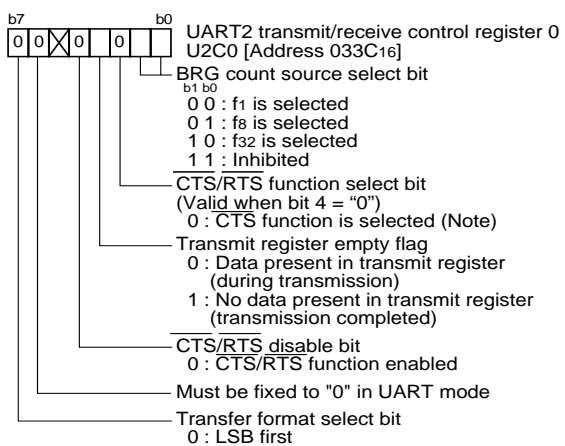
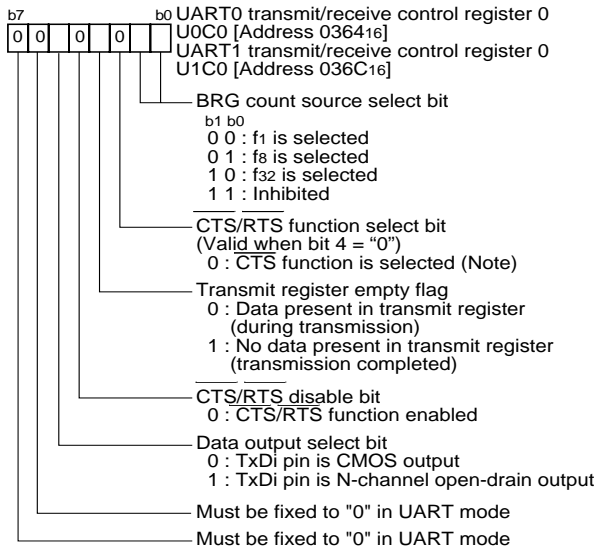
Figure 1. Operation timing of transmission in UART mode

3.0 Set-up procedure

Setting UARTi transmit/receive mode register (i=0 to 4)



Setting UARTi transmit/receive control register 0 (i=0 to 4)

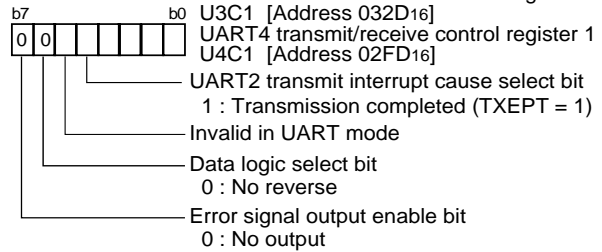
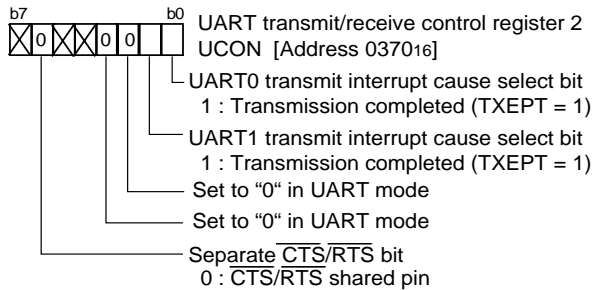


Note: Set the corresponding function select register A to I/O port and the port direction register to "0".

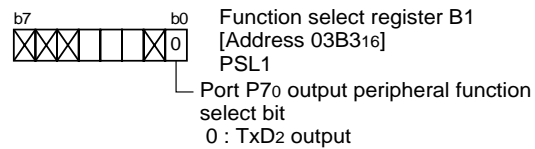
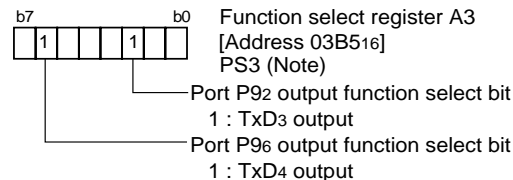
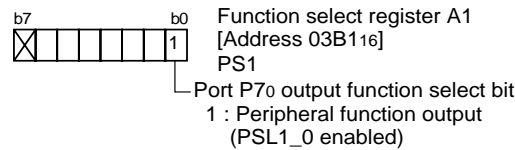
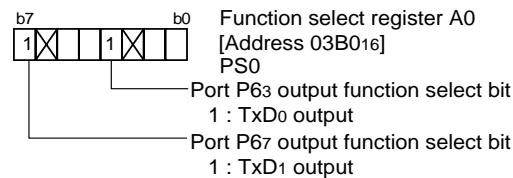
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Setting UART transmit/receive control register 2 and UARTi transmit/receive control register 1 (i=2 to 4)

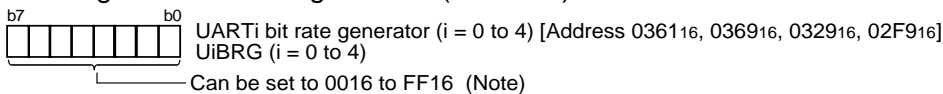


Setting function select register



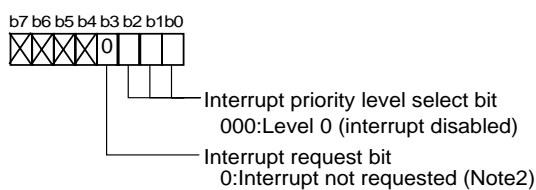
Note: Set bit 2 of the protect register (address 000A₁₆) to "1" when writing new value to this register.

Setting UARTi bit rate generator (i = 0 to 4)



Note: Write to UARTi bit rate generator when transmission/reception is halted.

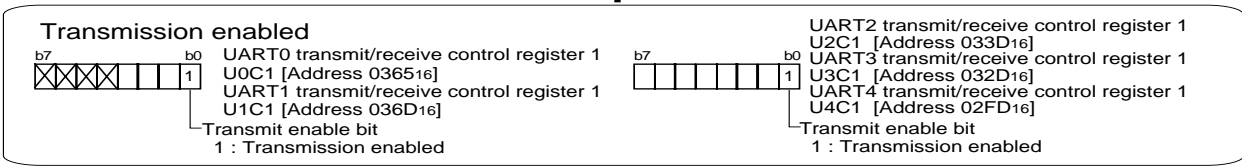
Clearing UARTi transmit interrupt request bit (i=0 to 4)



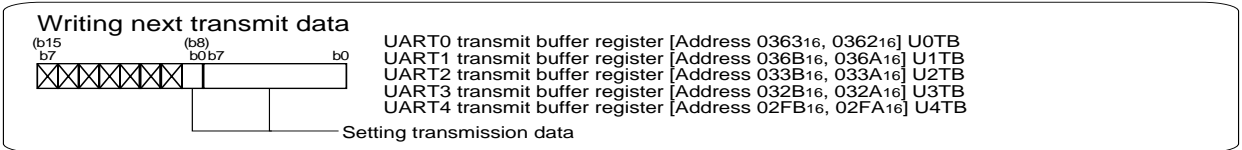
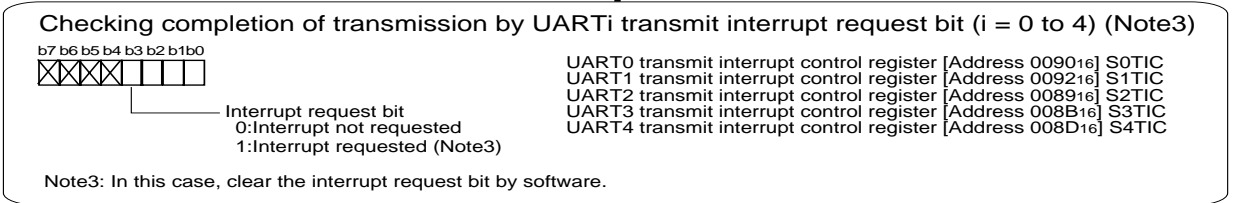
Note2: This bit can only be accessed for reset (=0), but cannot be accessed for set (=1).

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When CTS_i input level = "L"
Start transmission



Transmission is complete

4.0 Programming Code

```

;*****
;
; M16C/80 Program Collection
;
; FILE NAME : rjj05b0141_src.a30
; CPU      : M16C/80 Group
; FUNCTION  : Operation of Serial I/O
;            (transmission in UART mode)
; HISTORY   : 2004.02.16 Ver 1.00
;
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;
;*****
;*****
;      Include
;*****
;      .LIST      OFF      ;Stops outputting lines to the assembler list file
;      .INCLUDE   sfr80100.inc ;Reads the file that defined SFR
;      .LIST      ON      ;Starts outputting lines to the assembler list file
;
;*****
;      Symbol definition
;*****
RAM_TOP      .EQU    000400H ;Start address of RAM
RAM_END      .EQU    002BFFH ;End address of RAM
ROM_TOP      .EQU    0FFC000H ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFFDCH ;Start address of fixed vector
;
;*****
;      Allocation of work RAM area
;*****
;      .SECTION   WORKRAM, DATA
;      .ORG      RAM_TOP
WORKRAM_TOP:
C_POWER      .EQU    3
C_DATA_SIZE  .EQU    (1<< C_POWER) ;Data size
v_Trans_data: .BLKB  C_DATA_SIZE ;Area of send data for sample
WORKRAM_END:
;
;*****
;      Program area
;*****
;=====
;      Start up
;=====
;      .SECTION   PROGRAM, CODE ;Declares section name and section type
;      .ORG      ROM_TOP      ;Declares start address
RESET:
; Sets Processor mode, System clock and Main clock division
MOV.B #03H, prcr ;Removes protect
MOV.B #10000000B, pm0 ; Single-chip mode
MOV.B #11000000B, pm1 ; Flash memory version
MOV.B #00001000B, cm0 ; Xcin-Xcout High
MOV.B #00100000B, cm1 ; Xin-Xout High
MOV.B #00010010B, mcd ; No division mode
MOV.B #00H, prcr ;Protects all registers
;

```



```

; Clears WORKRAM area
MOV.W   #0, R0
MOV.W   #(RAM_END-RAM_TOP)/2, R3
MOV.W   #WORKRAM_TOP, A1
SSTR.W
; Makes transmit data for sample ( 1 to C_DATA_SIZE )
MOV.B   #1, R0L           ;1st data
MOV.W   #0, A0           ;Initialize offset address
MAKE_DATA:
MOV.B   R0L, v_Trans_data[A0] ;
ADD.B   #1, R0L           ;
ADD.W   #1, A0           ;
CMP.W   #C_DATA_SIZE, A0  ;
JLTU   MAKE_DATA         ;
;
;=====
;   Serial I/O (transmission in UART mode)
;=====
; Setting UART0 transmit/receive mode register
MOV.B   #01000101B, u0mr
;
;   ||| | | | ++-----;Serial I/O mode select bit (101:Transfer data 8 bits long)
;   ||| | | | +-----;Internal/external clock select bit (0:Internal clock)
;   ||| | | | +-----;Stop bit length select bit (0:One stop bit)
;   ||| | | | +-----;Odd/even parity select bit (0:Odd parity)
;   | +-----;Parity enable bit (1:Parity enabled)
;   +-----;Sleep select bit (0:Invalid)
; Setting UART0 transmit/ receive control register 0
MOV.B   #00001000B, u0c0
;
;   ||| | | | ++-----;BRG count source select bit (00:f1 is selected)
;   ||| | | | +-----;CTS function is selected (Valid when bit 4="0") (Note)
;   ||| | | | +-----;Transmit register empty flag (Written value is invalid)
;   ||| | | | +-----;CTS/RTS disable bit (0:CTS/RTS function enabled)
;   | +-----;Data output select bit (0:TxDi pin is CMOS output)
;   +-----;Must be fixed to "0" in UART mode
; Setting UART transmit/receive control register 2
MOV.B   #00000001B, ucon
;
;   ||| | | | | | +-----;UART0 transmit interrupt cause select
;   ||| | | | | |           (1:Transmission completed)
;   ||| | | | | | +-----;UART1 transmit interrupt cause select
;   ||| | | | | | +-----;Set to "0" in UART mode
;   | +-----;Nothing is assigned (When write, set "0")
;   | +-----;Separate CTS/RTS bit (0:CTS/RTS shared pin)
;   +-----;Nothing is assigned (When write, set "0")
; (Note) Set the corresponding function select register A to I/O port
; and port direction register to "0"
BCLR    pd6_0           ;Port P60 is input direction
BCLR    ps0_0           ;CTS0[P60] is I/O port
; Setting function select register
BSET    ps0_3           ;Port P63 output function select bit (1:TxD0 output)
; Setting UART0 bit rate generator
MOV.B   #129, u0brg    ;(Approx. 9600bps : fi/16(129+1) @20MHz,f1)
;                               ;(Note) Write to UARTi bit rate generator when
;                               ;       transmission/reception is halted
; Clear UART0 transmit interrupt request bit
MOV.B   #00000000B, s0tic
;
;   | +-----;Interrupt priority level select bit
;   |           (000:Level 0, interrupt disabled)
;   +-----;Interrupt request bit (0:Interrupt not requested)
; Transmission enabled
MOV.B   #00000001B, u0c1
;
;   +-----;Transmission enabled
;

```

```

=====
;      Main program
=====
      MOV.W   #0, A0           ;Initialize offset
WRITE_DATA:
      ; Writing transmit data
      MOV.B   v_Trans_data[A0], u0tb
      ; When CTS0 input level = "L", Start transmission
;
WAIT_TRANS:
      ; Checking completion of transmission by UART0 transmit interrupt request bit
      BTST   ir_s0tic
      JNC    WAIT_TRANS
      MOV.B   #00H, s0tic      ; Clear UART0 transmit interrupt request bit
;
PREPARE_NEXT_DATA:
      ADD.W   #1, A0
      AND.W   #(C_DATA_SIZE-1), A0
      JNZ    WRITE_DATA
;
COMPLETE_TRANS:
      ; Transmission is complete
      JMP     COMPLETE_TRANS
;
=====
;      Dummy interrupt processing program
=====
dummy:
      REIT
;
;*****
;      Setting of fixed vector
;*****
      .SECTION  F_VECT, ROMDATA
      .ORG     FIXED_VECT_TOP
;
      .LWORD   dummy      ;Undefined instruction
      .LWORD   dummy      ;Overflow
      .LWORD   dummy      ;BRK instruction execution
      .LWORD   dummy      ;Address match
      .LWORD   dummy      ;
      .LWORD   dummy      ;Watchdog timer
      .LWORD   dummy      ;
      .LWORD   dummy      ;NMI
      .LWORD   RESET      ;Reset
;
      .END

```

5.0 Reference

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Data Sheet

M16C/80 group Rev. E3

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M16C/80 group Rev. B

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