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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of Serial I/O (transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

1.0 Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up		Item	Set-up	
Transfer clock source	O	Internal clock (f_1 / f_8 / f_{32})	Transmission interrupt factor		Transmission buffer empty
		External clock (CLKi pin)		O	Transmission complete
$\overline{CTS}$ function		$\overline{CTS}$ function enabled	Output transfer clock to multiple pins (Note 1)		Not selected
	O	$\overline{CTS}$ function disabled		O	Selected
CLK polarity	O	Output transmission data at the falling edge of the transfer clock	$\overline{CTS}$ / $\overline{RTS}$ separation function (Note 2)	O	Pin shared by $\overline{CTS}$ and $\overline{RTS}$
					$\overline{CTS}$ and $\overline{RTS}$ separated
		Output transmission data at the rising edge of the transfer clock	Data logic select function (Note 3)	O	No reverse
					Reverse
Transfer clock	O	LSB first	TxD, RxD I/O polarity reverse bit (Note 3)	O	No reverse
		MSB first			Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, neither UART1 $\overline{CTS}$/$\overline{RTS}$ function, nor UART0 $\overline{CTS}$/$\overline{RTS}$ separation function can be utilized. Set the UART1 $\overline{CTS}$/$\overline{RTS}$ disable bit to "1".

Note 2: UART0 only. (UART1 $\overline{CTS}$/$\overline{RTS}$ function cannot be used when this function is selected.)

Note 3: UART2 to UART4 only.

2.0 Introduction

Operation (1) Setting the transmit enable bit to "1" makes data transmissible status ready.

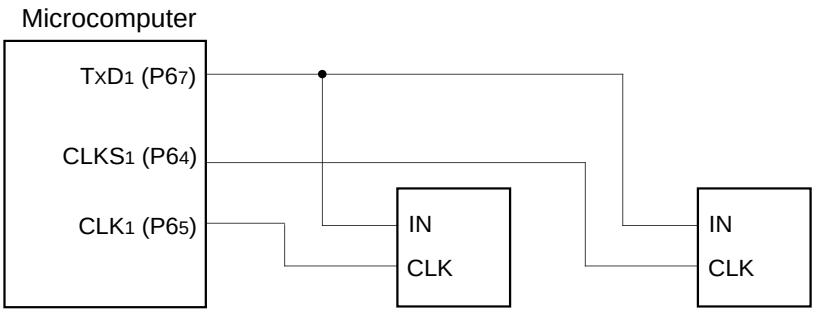
(2) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.

(3) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that the transmission is completed. The transfer clock stops at "H" level. At this time, the UART1 transmit interrupt request bit goes to "1".

(4) Setting port P65 output function select bit to "CLK_1 output" using the function select register A0 causes the transfer clock to be output to CLK_1. Setting port $P6_4$ output function select bit to "$CLKS_1$ output" using the function select registers A0 and B0 causes the transfer clock to be output to the $CLKS_1$. When selecting CLK_1 output, set port P64 to I/O port and the direction register to "1" and then output level to "H". When selecting $CLKS_1$ output, set port $P6_5$ to I/O port and the direction register to "1" and output level to "H". Change the transfer clock output pin when transmission is halted.

Figure 1 shows the operation timing

Example of wiring



Note: This applies when performing only transmission with an internal clock selected in the clock synchronous serial I/O mode.

Example of operation

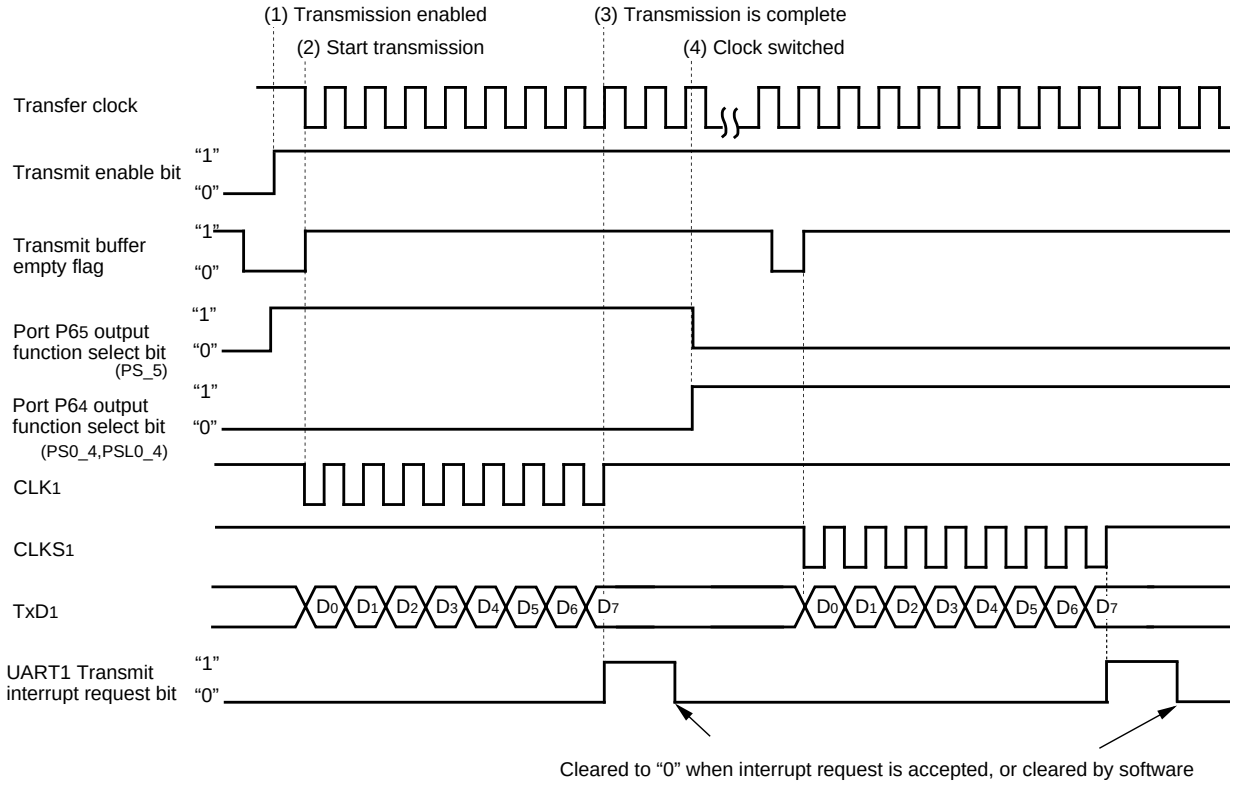
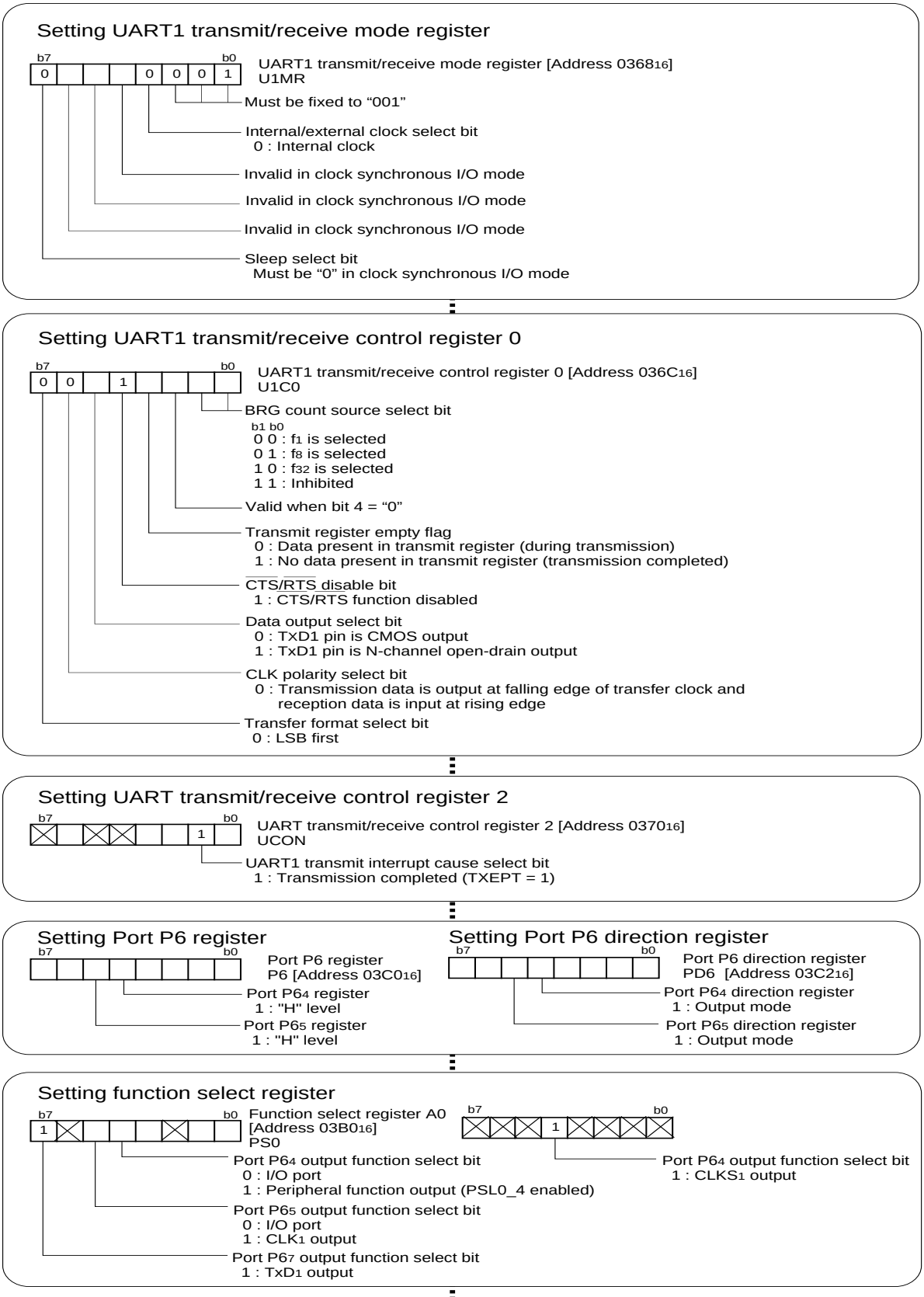


Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected

3.0 Set-up procedure



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Setting UART1 bit rate generator

b7 b0

UART1 bit rate generator [Address 0369$_{16}$]
U1BRG

Can be set to 00$_{16}$ to FF$_{16}$ (Note)

Note: Write to UART1 bit rate generator when transmission/reception is halted.

Clearing UART1 transmit interrupt request bit

b7 b6 b5 b4 b3 b2 b1 b0

UART1 transmit interrupt control register [Address 0092$_{16}$]
S1TIC

Interrupt priority level select bit
000 : Level 0 (interrupt disabled)

Interrupt request bit
0 : Interrupt not requested (Note2)

Note2: This bit can only be accessed for reset (=0), but cannot accessed for set (=1).

Transmission enabled

b7 b0

UART1 transmit/receive control register 1 [Address 036D$_{16}$]
U1C1

Transmit enable bit
1 : Transmission enabled

Writing transmit data

(b15) (b8)
b7 b0 b7 b0

UART1 transmit buffer register [Address 036B$_{16}$, 036A$_{16}$]
U1TB

Setting transmission data

Start transmission

Checking completion of transmission by UART1 transmit interrupt request bit (Note3)

b7 b6 b5 b4 b3 b2 b1 b0

UART1 transmit interrupt control register [Address 0092$_{16}$]
S1TIC

Interrupt request bit
0 : Interrupt not requested
1 : Interrupt requested (Note3)

Note3: In this case, clear the interrupt request bit by software.

Switching clock ouput pin

(1) When clocks are output from CLK1

b7 b0

Function select register A0
[Address 03B0$_{16}$]
PS0

Port P6$_4$ output function select bit
0 : I/O port

Port P6$_5$ output function select bit
1 : CLK$_1$ output

(2) When clocks are output from CLKS1

b7 b0

Function select register A0
[Address 03B0$_{16}$]
PS0

b7 b0

Port P6$_4$ output function select bit
1 : Peripheral function output (PSL0_4 enabled)

Port P6$_5$ output function select bit
0 : I/O port

Writing next transmit data

(b15) (b8)
b7 b0 b7 b0

UART1 transmit buffer register [Address 036B$_{16}$, 036A$_{16}$]
U1TB

Setting transmission data

Transmission is complete

4.0 Programming Code

```
;*****************************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0139_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of Serial I/O
;               (transmission in clock-synchronous serial I/O mode,
;                transfer clock output from multiple pins function)
;   HISTORY   : 2004.02.16  Ver 1.00
;
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;
;*****************************************************************************************
;*****************************************************************************************
;       Include
;*****************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;*****************************************************************************************
;       Symbol definition
;*****************************************************************************************
RAM_TOP          .EQU    000400H    ;Start address of RAM
RAM_END          .EQU    002BFFH    ;End address of RAM
ROM_TOP          .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP   .EQU    0FFFFDCH   ;Start address of fixed vector
;
C_OUTPUT_CLK     .EQU    00000H     ;
C_OUTPUT_CLKS    .EQU    0FFFFH     ;
;*****************************************************************************************
;       Allocation of work RAM area
;*****************************************************************************************
        .SECTION    WORKRAM, DATA
        .ORG        RAM_TOP
WORKRAM_TOP:
C_POWER          .EQU    3
C_DATA_SIZE      .EQU    (1<< C_POWER)  ;Data size
v_Trans_data:    .BLKB   C_DATA_SIZE    ;Area of send data for sample
flg_Switch:      .BLKW   1              ;Flag for switching output pin
WORKRAM_END:
;
;*****************************************************************************************
;       Program area
;*****************************************************************************************
;=========================================================================
;       Start up
;=========================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr        ;Removes protect
        MOV.B    #10000000B, pm0   ; Single-chip mode
        MOV.B    #11000000B, pm1   ; Flash memory version
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High
        MOV.B    #00010010B, mcd   ; No division mode
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
        ; Clears WORKRAM area
        MOV.W    #0, R0
        MOV.W    #(RAM_END-RAM_TOP)/2, R3
        MOV.W    #WORKRAM_TOP, A1
        SSTR.W
        ; Makes transmission data for sample ( 1 to C_DATA_SIZE )
        MOV.B    #1, R0L               ;1st data
        MOV.W    #0, A0                ;Initialize offset address
MAKE_DATA:                             ;
        MOV.B    R0L, v_Trans_data[A0] ;
        ADD.B    #1, R0L               ;
        ADD.W    #1, A0                ;
        CMP.W    #C_DATA_SIZE, A0      ;
        JLTU     MAKE_DATA             ;
;
;=============================================================================
;       Serial I/O (transmission in clock-synchronous serial I/O mode,
;                transfer clock output from multiple pins function selected)
;=============================================================================
        ; Setting UART1 transmit/receive mode register
        MOV.B    #00000001B, u1mr
;                |||||+++---------;Must be fixed to "001"
;                ||||+------------;Internal/external clock select bit (0:Internal clock)
;                |+++-------------;Invalid in clock synchronous I/O mode
;                +----------------;Sleep select bit
;                                  (Must always be "0" in clock synchronous I/O mode)
        ; Setting UART1 transmit/receive control register 0
        MOV.B    #00011000B, u1c0
;                ||||||++---------;BRG count source select bit (00:f1 is selected)
;                |||||+-----------;(Valid when bit 4="0")
;                ||||+------------;Transmit register empty flag (Written value is invalid)
;                |||+-------------;CTS/RTS disable bit (1:CTS/RTS function disabled)
;                ||+--------------;Data output select bit (0:TxDi pin is CMOS output)
;                |+---------------;CLK polarity select bit
;                |                 (0:Transmission data is output at falling edge of
;                |                    transfer clock and
;                |                    reception data is input at rising edge)
;                +----------------;Transfer format select bit (0:LSB first)
        ; Setting UART transmit/receive control register 2
        BSET     u1irs             ;UART1 transmit interrupt cause select
                                   ;(1:Transmission completed(TXEPT=1))
        ; Setting Port P6 register
        BSET     p6_5              ;CLK1[P65] (1:"H" level)
        BSET     p6_4              ;CLKS1[P64] (1:"H" level)
        ; Setting Port P6 direction register
        BSET     pd6_5             ;Port P65 direction register (1:P65 output)
        BSET     pd6_4             ;Port P64 direction register (1:P64 output)
        ; Setting function select register (Selecting CLK1 output and TxD1 output)
        MOV.B    #10100000B, ps0
;                | |+-------------;Port P64 output function select bit (0:P64 is I/O port)
;                | +--------------;Port P65 output function select bit (1:CLK1 output)
;                +----------------;Port P67 output function select bit (1:TxD1 output)
        ; Setting UART1 bit rate generator (1MHz, @20MHz f1)
        MOV.B    #9, u1brg
        ; Clear UART1 transmit interrupt request bit
        MOV.B    #00000000B, s1tic
;                    |+++---------;Interrupt priority level select bit
;                    |             (000:Level 0, interrupt disabled)
;                    +------------;Interrupt request bit (0:Interrupt not requested)
        ; Transmission enabled
        MOV.B    #00000001B, u1c1
;                       +---------;Transmission enabled
;
```

```
;===============================================================================
;       Main program
;===============================================================================
        ; Initialize flag for switching output pin
        BTST    ps0_5
        STZX.W  #C_OUTPUT_CLKS, #C_OUTPUT_CLK, flg_Switch
;
        MOV.W   #0, A0          ;Initialize offset
WRITE_DATA:
        ; Writing transmit data
        MOV.B   v_Trans_data[A0], u1tbl
        ; Start transmission
;
WAIT_TRANS:
        ; Checking completion of transmission by UART1 transmit interrupt request bit
        BTST    ir_s1tic
        JNC     WAIT_TRANS
        MOV.B   #00H, s1tic     ; Clear UART1 transmit interrupt request bit
;
SWITCH_CLKPIN:
        ; Switching clock output pin
        ; (This sample switches clock output pin by 1 byte transmission)
        ; Change output pin to CLK1 from CLKS1
        CMP.W   #C_OUTPUT_CLKS, flg_Switch
        JNE     CHG_CLKS_OUT
        MOV.W   #C_OUTPUT_CLK, flg_Switch
        ; (1) When clocks are output from CLK1
        MOV.B   #10100000B, ps0
;                | |+------------;(0:P64 is I/O port)
;                | +-------------;(1:CLK1 output)
;                +---------------;(1:TxD1 output)
        JMP     END_SWITCH_CLKPIN
CHG_CLKS_OUT:
        ; Change output pin to CLKS1 from CLK1
        MOV.W   #C_OUTPUT_CLKS, flg_Switch
        ; (2) When clocks are output from CLKS1
        BSET    psl0_4          ;(1:CLKS1 output)
        MOV.B   #10010000B, ps0
;                | |+------------;(1:P64 peripheral function output, psl0_4 enabled)
;                | +-------------;(0:P65 is I/O port)
;                +---------------;(1:TxD1 output)
END_SWITCH_CLKPIN:
;
PREPARE_NEXT_DATA:
        ADD.W   #1, A0
        AND.W   #(C_DATA_SIZE-1), A0
        JNZ     WRITE_DATA
;
COMPLETE_TRANS:
        ; Transmission is complete
        JMP     COMPLETE_TRANS
```

```
;===============================================================================
;       Dummy interrupt processing program
;===============================================================================
dummy:
        REIT
;
;*******************************************************************************
;
;       Setting of fixed vector
;*******************************************************************************
;
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

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Data Sheet

M16C/80 group Rev. E3
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