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M16C/64 Group

Operation of serial I/O (transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

**(transmission in clock-synchronous serial I/O mode,
 transfer clock output from multiple pins function)**
3. Chosen functions
Table 1. Chosen functions

Item	Set-up		Item	Set-up	
Transfer clock source	<input type="radio"/>	Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	Transmission interrupt factor	<input type="checkbox"/>	Transmission buffer empty
	<input type="checkbox"/>	External clock (CLKi pin)		<input type="radio"/>	Transmission complete
CTS function	<input type="checkbox"/>	CTS function enabled	Output transfer clock to multiple pins (Note 1)	<input type="checkbox"/>	Not selected
	<input type="radio"/>	CTS function disable		<input type="radio"/>	Selected
CLK polarity	<input type="radio"/>	Output transmission data at the falling edge of the transfer clock	Data logic select function	<input type="radio"/>	No reverse
	<input type="checkbox"/>	Output transmission data at the rising edge of the transfer clock		<input type="checkbox"/>	Reverse
Transfer clock	<input type="radio"/>	LSB first	TxD, RxD I/O polarity reverse bit	<input type="radio"/>	No reverse
	<input type="checkbox"/>	MSB first		<input type="checkbox"/>	Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{\text{CTS}}$ / $\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}$ / $\overline{\text{RTS}}$ disable bit to “1”.

4. Operation

(1) Setting the transmit enable bit to “1” makes data transmissible status ready.

(2) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.

(3) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that the transmission is completed. The transfer clock stops at “H” level. At this time, the UART1 transmit interrupt request bit goes to “1”.

(4) Setting CLK/CLKS select bit 1 to “1” and setting CLK/CLKS select bit 0 to “1” causes the CLKs1 pin to go to the transfer clock output pin. Change the transfer clock output pin when transmission is halted.

(transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

Figure 1 shows the operation timing.

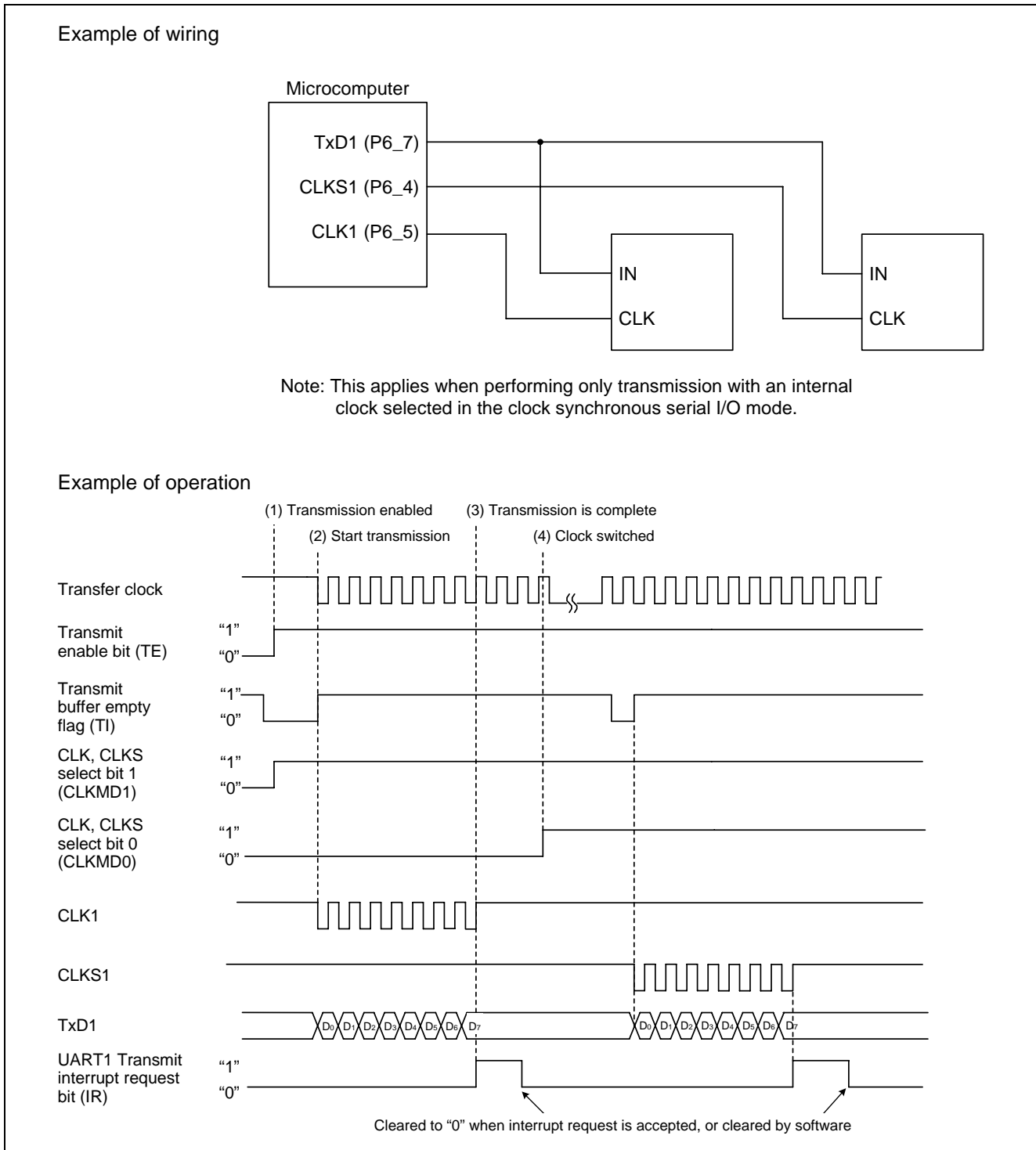
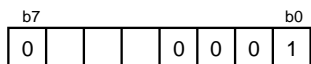


Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function selected

(transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

5. Set-up procedure

Setting UART1 transmit/receive mode register



UART1 transmit/receive mode register [Address 0258h]
U1MR

Must be fixed to "001"

Internal/external clock select bit

0 : Internal clock

Invalid in clock synchronous I/O mode

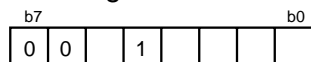
Invalid in clock synchronous I/O mode

Invalid in clock synchronous I/O mode

TxD, RxD I/O polarity reverse bit

Usually set to "0"

Setting UART1 transmit/receive control register 0



UART1 transmit/receive control register [Address 025Ch] U1C0

UiBRG count source select bit

b1 b0

0 0 : f1SIO or f2SIO is selected

0 1 : f8SIO is selected

1 0 : f32SIO is selected

1 1 : Do not set to this value

CTS/RTS function select bit (Valid when bit4 = "0")

Transmit register empty flag

0 : Data present in transmit register (during transmission)

1 : No data present in transmit register (transmission completed)

CTS/RTS disable bit

1 : CTS/RTS function disabled

Data output select bit

0 : Pins TxDi/SDAi and SCLi are CMOS output

1 : Pins TxDi/SDAi and SCLi are N-channel open-drain output

CLK polarity select bit

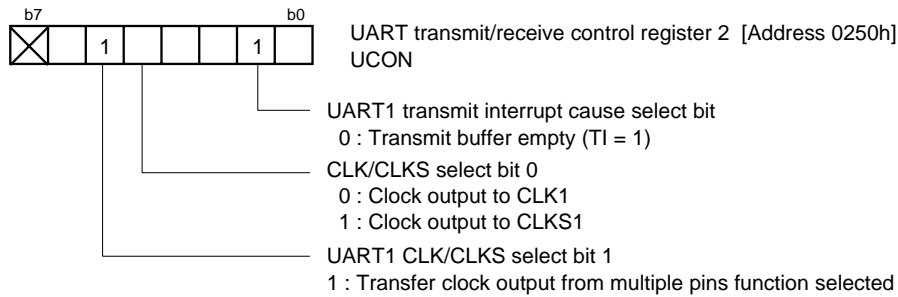
0 : Transmission data is output at falling edge of transfer clock and
reception data is input at rising edge

Transfer format select bit

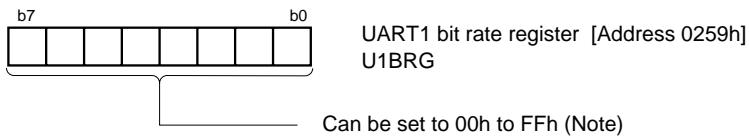
0 : LSB first

(transmission in clock-synchronous serial I/O mode, transfer clock output from multiple pins function)

Setting UART transmit/receive control register 2

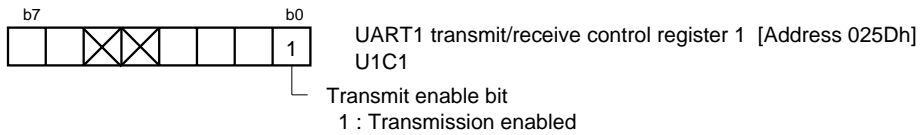


Setting UART1 bit rate register

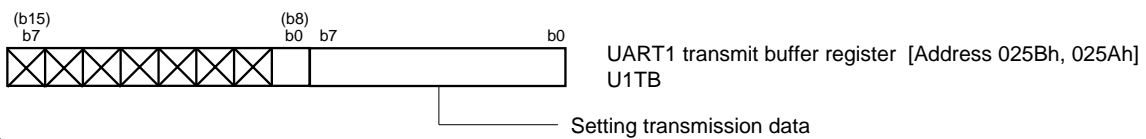


Note : Write to UARTi bit rate register when transmission/reception is halted.

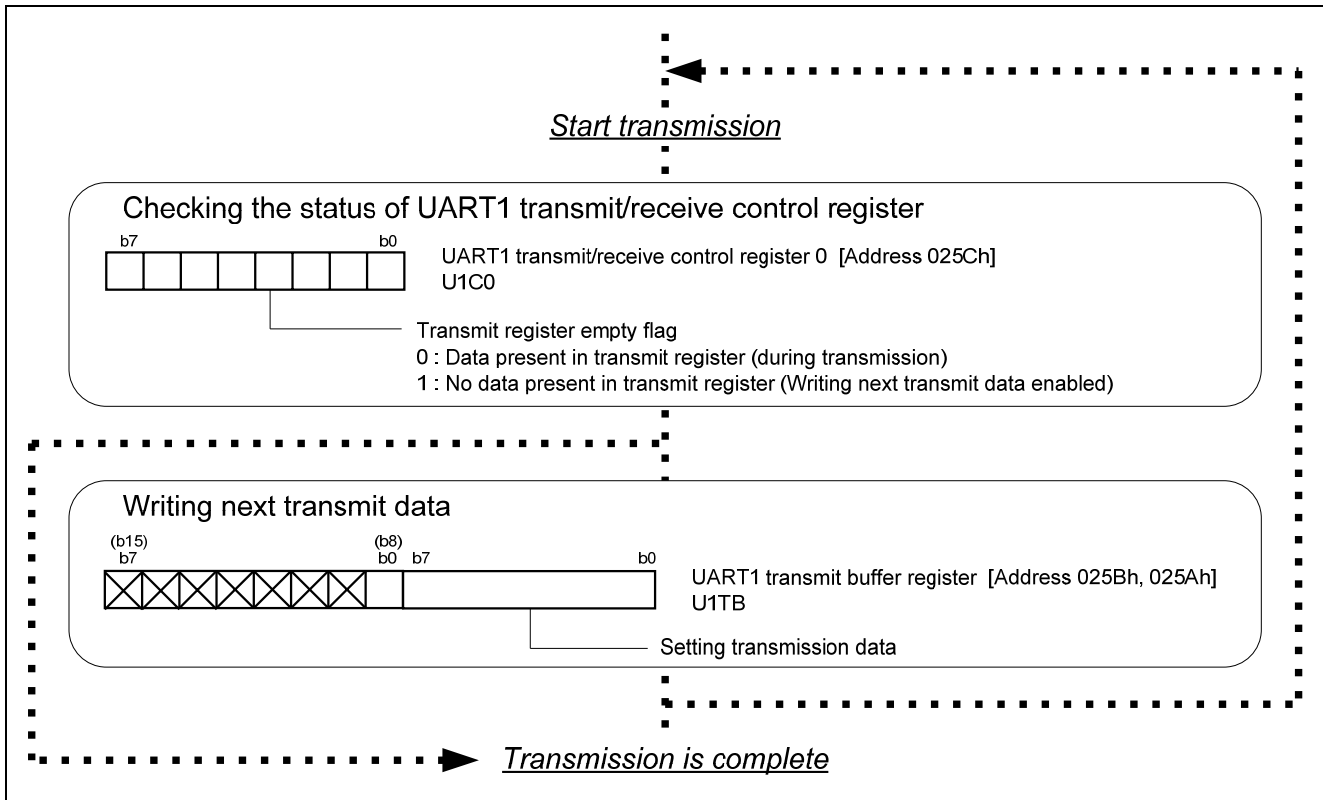
Transmission enabled



Writing transmit data



(transmission in clock-synchronous serial I/O mode,
transfer clock output from multiple pins function)



6. Reference

Hardware manual

M16C/64 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update

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(transmission in clock-synchronous serial I/O mode,
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Revision

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