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Renesas Electronics Corporation

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M16C/Tiny Series

Operation of Serial I/O (Reception in Clock-Asynchronous Serial I/O Mode)

1. Abstract

In receiving data in clock-asynchronous serial I/O mode, choose functions from those listed in Table1. Operations of the checked items are described below.

Table 1. Chosed Functions

Item	Set-up		Item	Set-up	
Transfer clock source	Yes	Internal clock (f1/f2/f3/f32)	$\overline{\text{CTS/RTS}}$ separated function (Note 1)	Yes	$\overline{\text{CTS/RTS}}$ shared pin
		External clock (CLKi pin)			$\overline{\text{CTS/RTS}}$ separated
RTS function	Yes	RTS function enabled	Data logic select (Note 2)	Yes	No reverse
		$\overline{\text{RTS}}$ function disabled			Reverse
			TxD, RxD I/O polarity reverse function (Note 2)	Yes	No reverse
					Reverse

Note 1: UART0 only

Note 2: UART2 only.

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/26, M16C/26A, M16C/28, M16C/29 microcomputers. However, some functions may have been modified.

Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Operation of Serial I/O

- (1) Setting the receive enable bit to “1” readies data-receivable status. At this time, output from the $\overline{\text{RTSi}}$ pin goes to “L” level to inform the transmission side that the receivable status is ready.
- (2) When the first bit (the start bit) of reception data is received from the RxDi pin, output from the $\overline{\text{RTSi}}$ goes to “H” level. Then, data is received, bit by bit, in sequence: LSB, ..., MSB, and stop bit(s).
- (3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. At this time, the receive complete flag goes to “1” to indicate that the reception is completed, the UARTi receive interrupt request bit goes to “1”, and output from the RTS pin goes to “H” level.
- (4) The receive complete flag goes to “0” when the lower-order byte of the UARTi buffer register is read.

Figure 1 shows the operation timing.

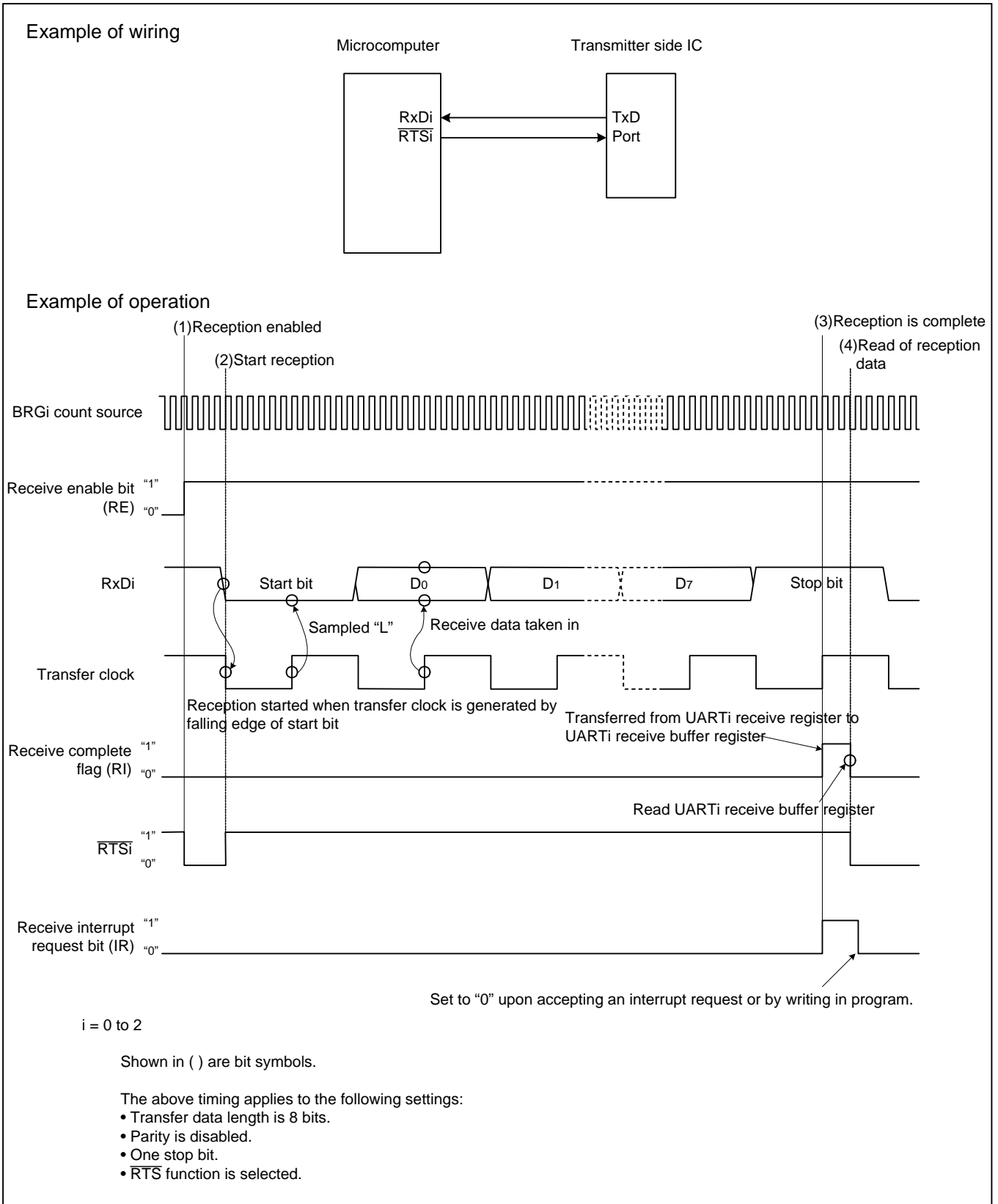
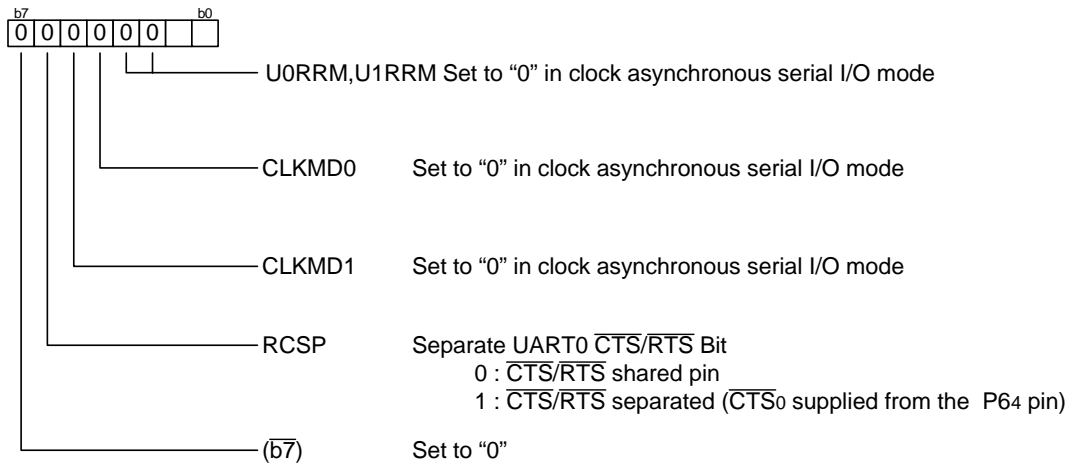
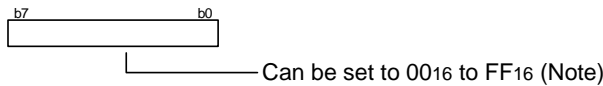


Figure 1. Operation Timing of Reception in Clock-Asynchronous Serial I/O Mode

(3) Setting UART transmit/receive control register 2



(4) Setting UARTi baud rate generation register (i=0,1)

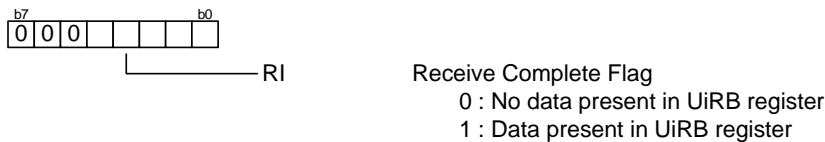


Note: Write to UARTi baud rate generation register when transmission/reception is halted.

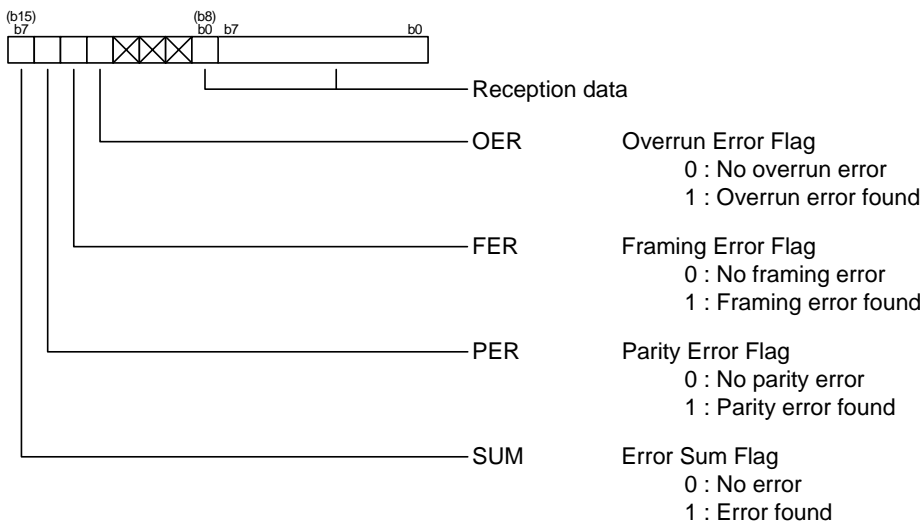
(5) Transmission enabled (UARTi transmit/receive control register 1) (i=0,1))



(6) Checking the status of UARTi receive buffer register (i=0,1)

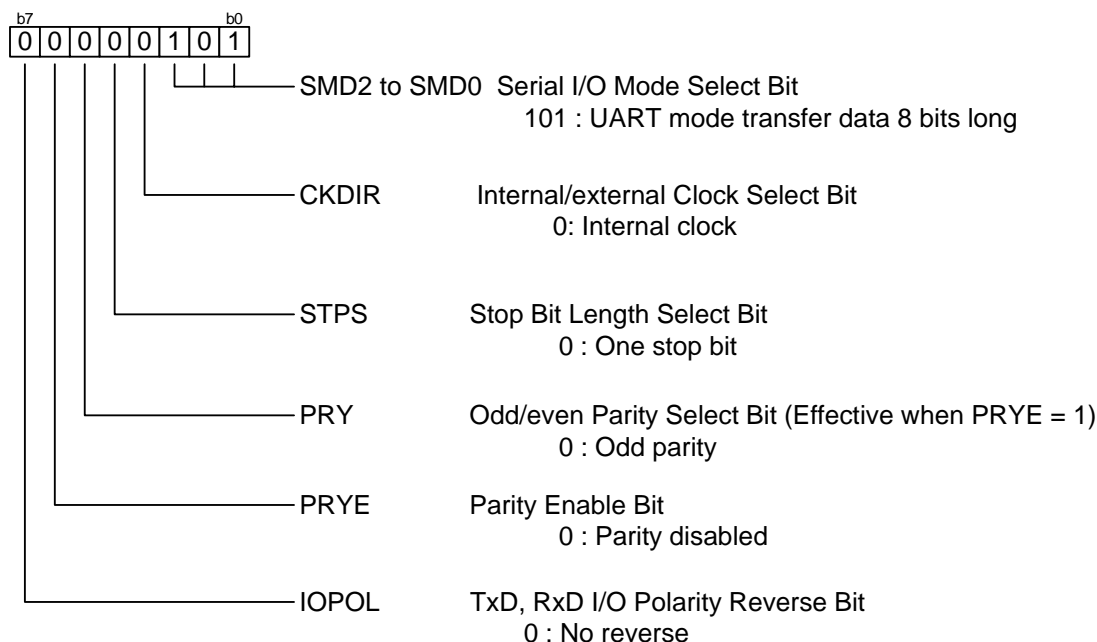


(7) Reading out reception data and checking error (Read UARTi reception buffer register (i=0,1))

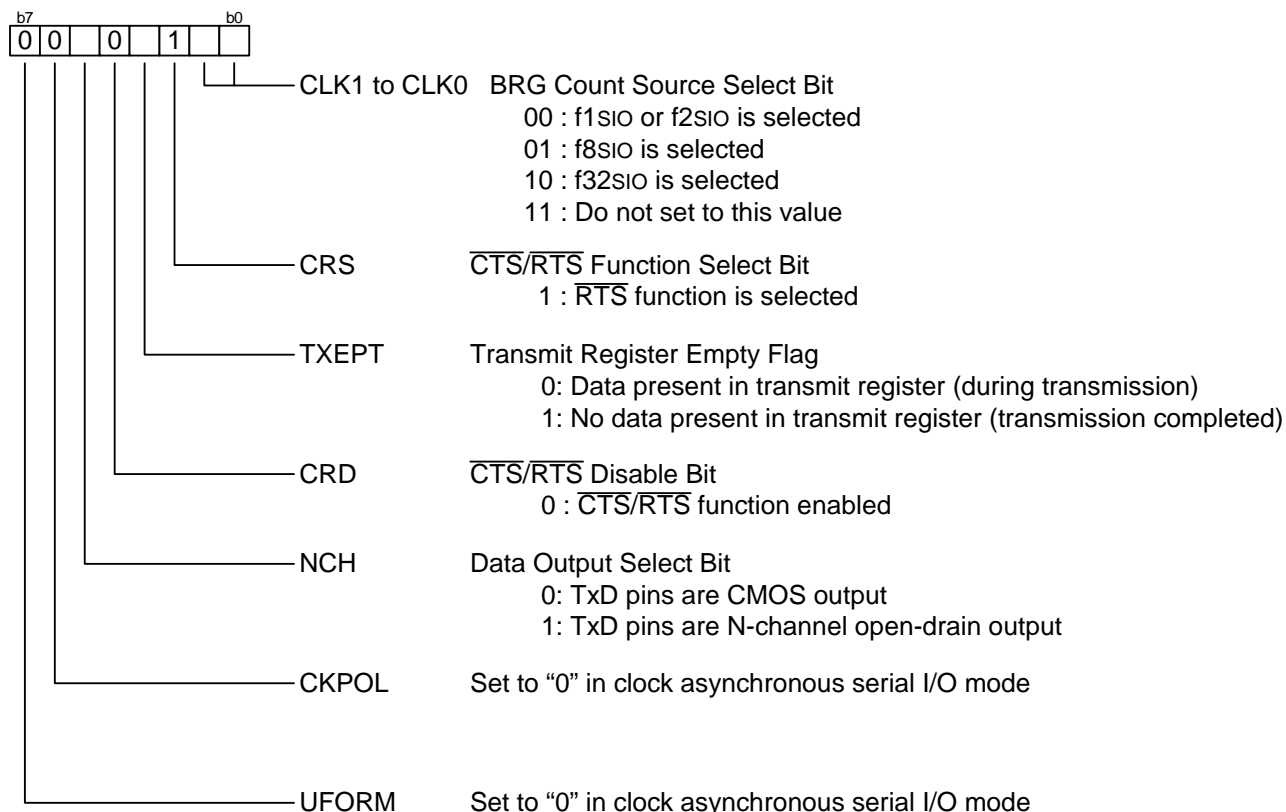


3.1.2 UART2

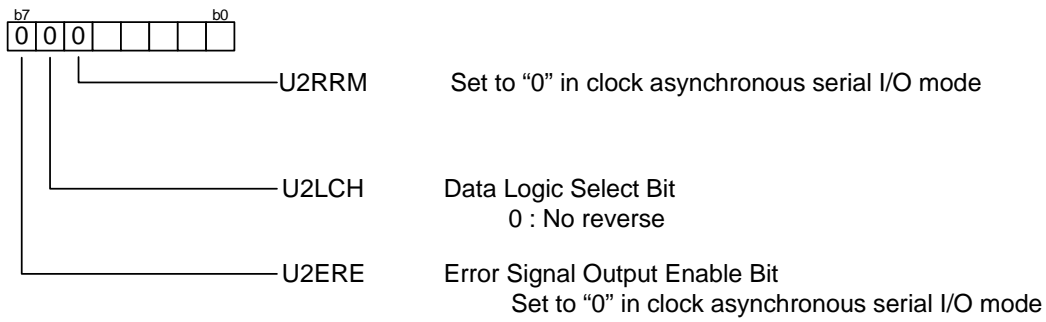
(1) Setting UART2 transmit/receive mode register



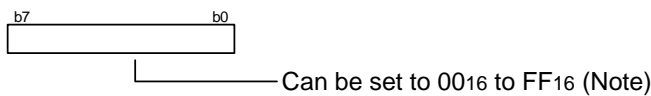
(2) Setting UART2 transmit/receive control register 0



(3) Setting UART2 transmit/receive control register 1



(4) Setting UART2 baud rate generation register

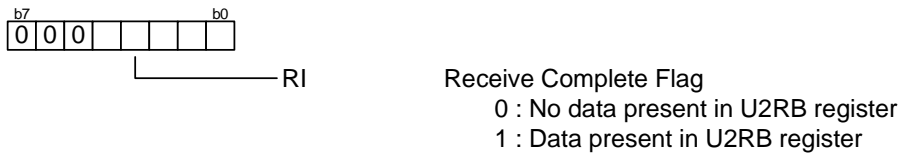


Note: Write to UART2 baud rate generation register when transmission/reception is halted.

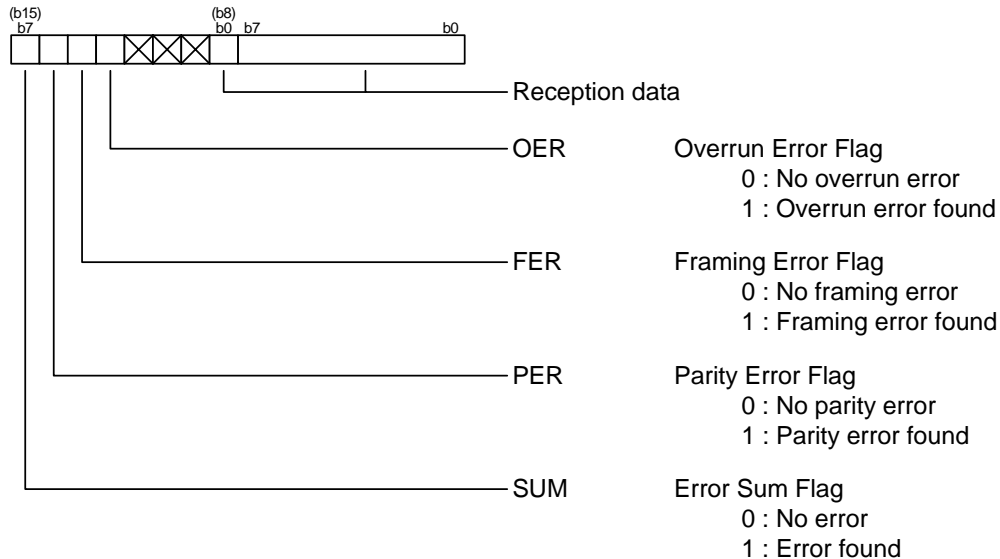
(5) Transmission enabled (UART2 transmit/receive control register 1)



(6) Checking the status of UARTi receive buffer register (i=0,1)



(7) Reading out reception data and checking error (Read UART2 reception buffer register)



4. Sample Program

4.1 UART0

```

/*****
 *
 * FILE NAME :
 * CPU : M16C/Tiny series
 * Function : Operation of UART0
 * (Clock asynchronous serial I/O receive)
 * Version : 1.00
 *
 * Copyright (C)2004, Renesas Technology Corp.
 * Copyright (C)2004, Renesas Solutions Corp.
 *
 *****/
/*****
 * include file
 *****/
#include "sfr28.h"

/*****
 * Function Definition
 *****/

/*****
 * main
 *****/
unsigned short recevie_data;

void main(void) {

    u0mr = 0x05; /* UART0 transmit/receive mode register setting
                UART mode transfer data 8 bits long
                Internal clokc select
                One stop bit
                Parity disabled
                */

    u0c0 = 0x04; /* UART0 transmit/receive control register 0 setting
                ~RTS function select
                ~CTS/~RTS function enabled
                TxD0 pin is CMOS output
                Transmission data is output at falling edge of transfer
                clock and reception data is input at rising edge
                LSB first
                */

    ucon = 0x00; /* UART transmit/receive control register 2 setting
                UART0 tansmit interrupt cause is selected to "Transmit bufffer empty(TI=1)"
                ~CTS/~RTS shared pin
                */

    u0brg = 129; /* Setting UART0 bit rate generator (Approx 9600bps @20MHz f1) */

    u0c1 = 0x04; /* UART transmit/receive control register 1 setting
                Reception enabled
                */

    while (1) {

        while (!ri_u0c1) { /* Check & wait the status of UART0 receive complete flag */
        }

        recevie_data = u0rb; /* Recevie data read */

    }
}

```

4.2 UART2

```

/*****
*
*   FILE NAME :
*   CPU       : M16C/Tiny series
*   Function  : Operation of UART2
*               (Clock asynchronous serial I/O receive)
*   Version   : 1.00
*
*   Copyright (C)2004, Renesas Technology Corp.
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*
*****/
/*****
*   include file
*****/
#include "sfr28.h"

/*****
*   Function Definition
*****/

/*****
*   main
*****/
    unsigned short  recevie_data;

void main(void) {

    u2mr = 0x05; /* UART2 transmint/receive mode register setting
                 UART mode transfer data 8 bits long
                 Internal clokc select
                 One stop bit
                 Parity disabled
                 */

    u2c0 = 0x04; /* UART2 transmint/receive control register 0 setting
                 ~RTS function select
                 ~CTS/~RTS function enabled
                 Tx0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
                 */

    u2c1 = 0x00; /* UART transmint/receive control register 1 setting
                 UART0 tansmit interrupt cause is selected to "Transmit bufffer empty(TI=1)"
                 */

    u2brg = 129; /* Setting UART2 bit rate generator (Approx 9600bps @20MHz f1) */

    u2c1 = 0x04; /* UART transmint/receive control register 1 setting
                 Reception enabled
                 */

    while (1) {

        while (!ri_u2c1) { /* Check & wait the status of UART0 receive complete flag */
        }

        recevie_data = u2rb; /* Recevie data read */

    }
}

```

5. Reference

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Hardware Manual

M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual

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REVISION HISTORY

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