

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## M16C/62A Group

### Operation of DMAC (repeated transfer mode)

#### 1.0 Abstract

In repeat transfer mode, choose functions from the items shown in Table 1. Operations of the circled items are described below.

**Table 1. Chosed functions**

Item	Set-up
Transfer space	Fixed address from an arbitrary 1 M bytes space
	<input type="radio"/> Arbitrary 1 M bytes space from a fixed address
	Fixed address from fixed address
Unit of transfer	8 bits
	<input type="radio"/> 16 bits

#### 2.0 Introduction

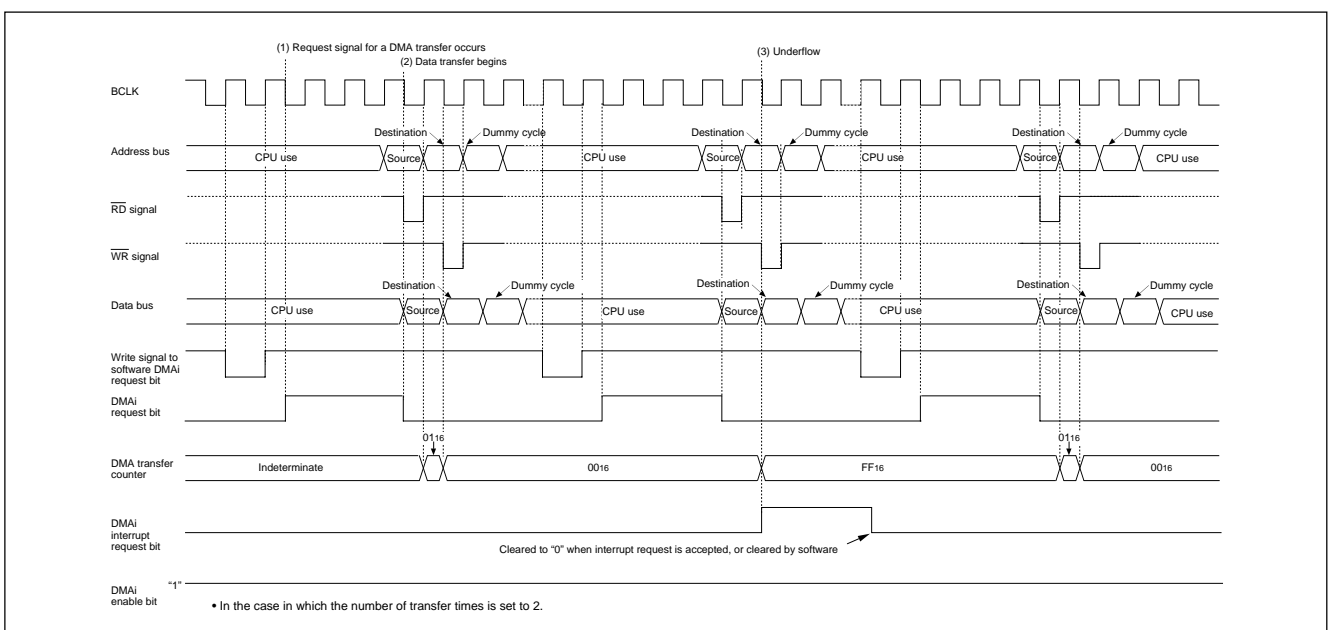
Operation (1) When software trigger is selected, setting software DMA request bit to "1" generates a DMA transfer request signal.

(2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi forward-direction address pointer are transferred to the address indicated by the DMAi destination pointer. When data transfer starts directly after DMAC becomes active, the value of the DMAi transfer counter reload register is reloaded to the DMAi transfer counter, and the value of the DMAi source pointer is reloaded by the DMAi forward-direction address pointer. Each time a DMA transfer request signal is generated, 2 byte of data is transferred. The DMAi transfer counter is down counted, and the DMAi forward-direction address pointer is up counted.

(3) Though DMAi transfer counter is underflowed, DMA enable bit is still "1". The DMA interrupt request bit changes to "1" simultaneously.

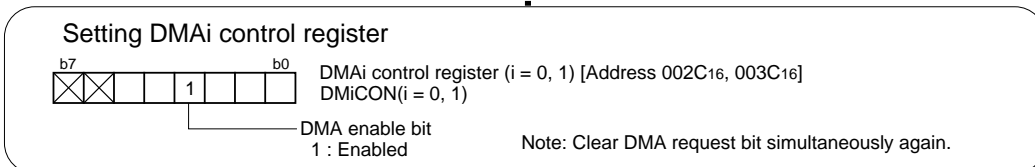
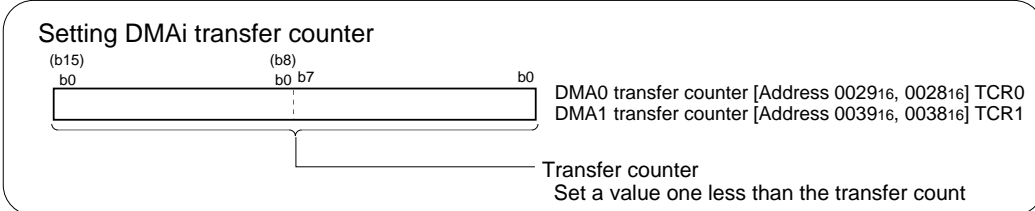
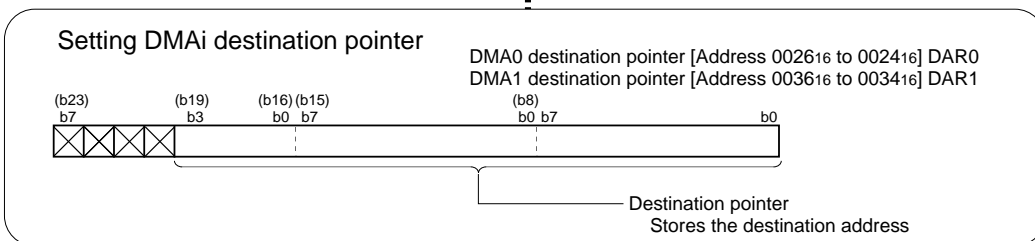
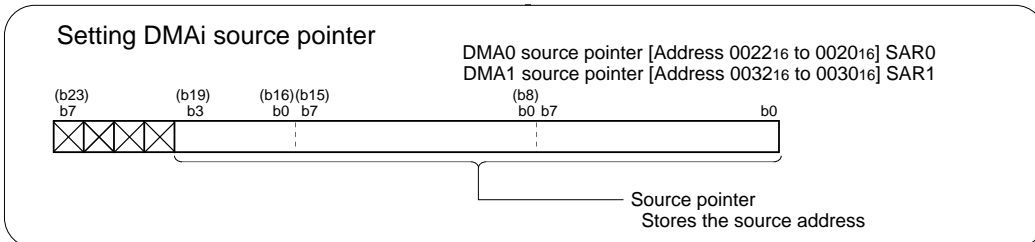
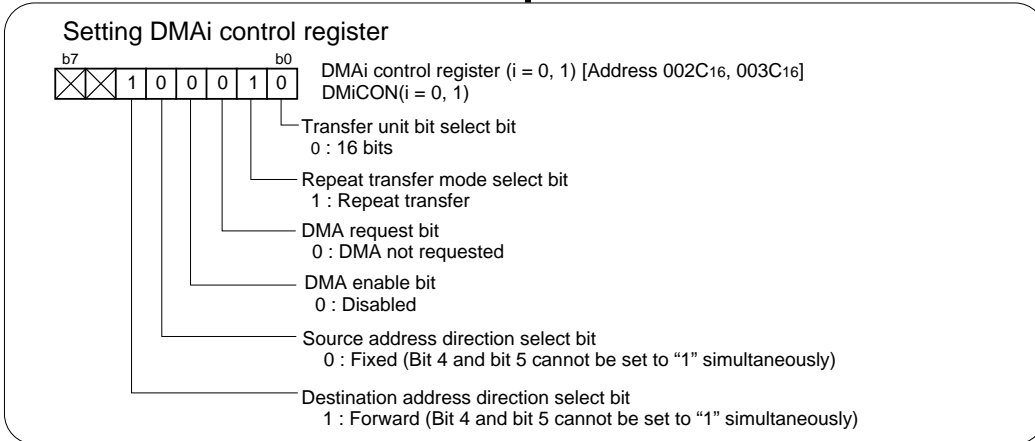
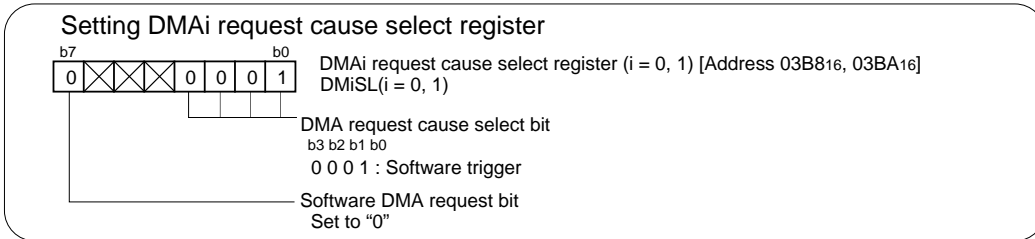
(4) After DMAi transfer counter is underflowed, when the next DMA request is generated, DMA transfer is repeated from (1).

Figure 1 shows an example of operation



**Figure 1. Example of operation of repeated transfer mode**

### 3.0 Set-up procedure



When software DMA request bit = "1"

Start DMA transmission

### 4.0 Programming Code

```

;*****
;
; M16C/62A Program Collection
;
; FILE NAME : rjj05b0063_src.a30
; CPU      : M16C/62A Group
; FUNCTION  : Operation of DMAC
;           (repeated transfer mode)
; HISTORY   : 2003.05.16 Ver 1.00
;
; Copyright(C)2003, Renesas Technology Corp.
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; All rights reserved.
;
;*****
;*****
; Include
;*****
;*****
;      .LIST      OFF          ;Stops outputting lines to the assembler list file
;      .INCLUDE   sfr62a.inc   ;Reads the file that defined SFR
;      .LIST      ON          ;Starts outputting lines to the assembler list file
;
;*****
;      Symbol definition
;*****
RAM_TOP      .EQU    00400H    ;Start address of RAM
RAM_END      .EQU    00FFFH    ;End address of RAM
ROM_TOP      .EQU    0F8000H   ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFDC   ;Start address of fixed vector
C_CNT_DMA    .EQU    8        ;DMA transfer counter
;*****
;      Allocation of work RAM area
;*****
;      .SECTION   WORKRAM, DATA
;      .ORG      RAM_TOP
WORKRAM_TOP:
v_Src_DMA:   .BLKW   1        ;DMA source
v_Dst_DMA:   .BLKW   (C_CNT_DMA);DMA destination area
WORKRAM_END:
;
;*****
;      Program area
;*****
;*****
;      Start up
;*****
;*****
;      .SECTION   PROGRAM, CODE ;Declares section name and section type
;      .ORG      ROM_TOP      ;Declares start address
RESET:
MOV.B #03H, prcr ;Removes protect
;Set processor mode registers 0 and 1
MOV.B #00000000B, pm0 ; Single-chip mode
MOV.B #00000000B, pm1 ; No expansion, No wait
;Set system clock control registers 0 and 1
MOV.B #00001000B, cm0 ; Xcin-Xcout High
MOV.B #00100000B, cm1 ; Xin-Xout High, Main clock is No divison
MOV.B #00H, prcr ;Protects all registers
;

```

```

;=====
;   DMAC (repeated transfer mode)
;=====
MOV.W   #055AAH, v_Src_DMA   ;Set DMA transmit data
;
MOV.B   #00100010B, dm0con   ;Setting DMA0 control register
;           |||||+-----;Transfer unit bit select bit (0:16bits)
;           |||||+-----;Repeat transfer mode select bit (1:Repeat transfer)
;           |||+-----;DMA request bit (0:DMA not requested)
;           |+-----;DMA enable bit (0:Disabled)
;           |+-----;Source address direction select bit (0:Fixed)
;           +-----;Destination address direction select bit (1:Forward)
;
MOV.B   #00000001B, dm0sl    ;Setting DMA0 request cause select register
;           |  ++++-----;DMA request cause select bit (0001:Software trigger)
;           +-----;Software DMA request bit (Set to "0")
;
MOV.W   #(v_Src_DMA & 0FFFFh), sar0   ;Set DMA0 source pointer M,L
MOV.B   #(v_Src_DMA >> 16),   sar0h   ;Set DMA0 source pointer H
;
MOV.W   #(v_Dst_DMA & 0FFFFh), dar0   ;Set DMA0 destination pointer M,L
MOV.B   #(v_Dst_DMA >> 16),   dar0h   ;Set DMA0 destination pointer H
;
MOV.W   #(C_CNT_DMA-1), tcr0   ;Setting DMA0 transfer counter
;
MOV.B   #00101010B, dm0con     ;Setting DMA0 control register
;           |+-----;Clear DMA request bit simultaneously
;           +-----;DMA enable bit (1:Enabled)
;
BSET    dsr_dm0sl              ;Start DMA transmission by
;                               ;software DMA request bit = "1"
;
MAIN:
JMP     MAIN
;
;=====
;   Dummy interrupt processing program
;=====
dummy:
REIT
;
;*****
;   Setting of fixed vector
;*****
.SECTION   F_VECT, ROMDATA
.ORG      FIXED_VECT_TOP
;
.LWORD    dummy   ;Undefined instruction interrupt vector
.LWORD    dummy   ;Overflow (INT0 instruction) interrupt vector
.LWORD    dummy   ;BRK instruction interrupt vector
.LWORD    dummy   ;Address match interrupt vector
.LWORD    dummy   ;Single-step interrupt vector
.LWORD    dummy   ;Watchdog timer interrupt vector
.LWORD    dummy   ;DBC interrupt vector
.LWORD    dummy   ;NMI interrupt vector
.LWORD    RESET   ;Sets reset vector
;
.END

```

**5.0 Reference**

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**Technical Support**

E-mail: [support\\_apl@renesas.com](mailto:support_apl@renesas.com)

**Data Sheet**

M16C/62A group Rev. C.1  
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**User's Manual**

M16C/62A group Rev. 1.0  
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