

This application note explains the overall delay affected by feedback trace delay. An LVCMOS ZDB is used as an example. Figure 1 shows a general LVCMOS Zero Delay Buffer (ZDB) schematic.

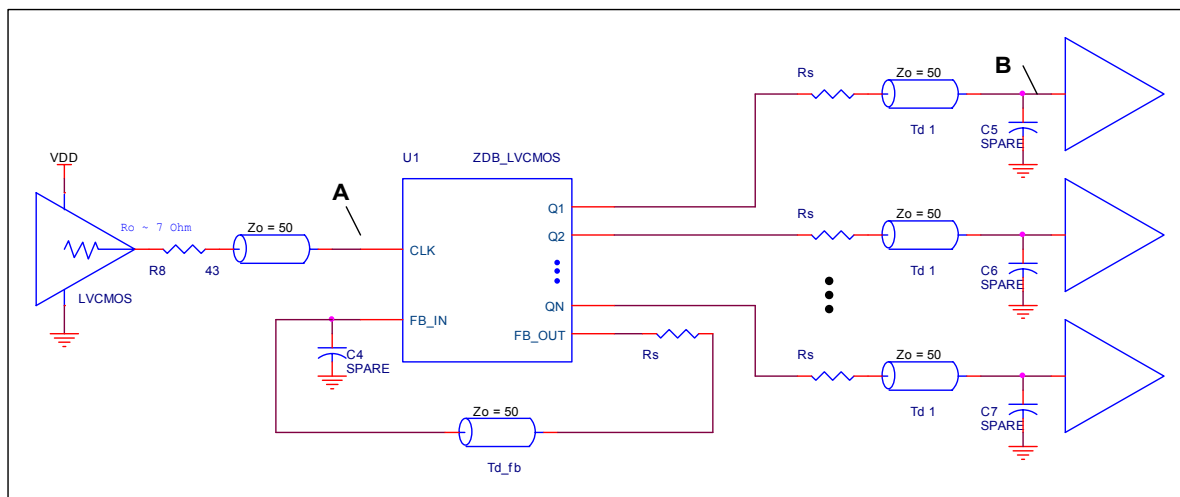


Figure 1 A ZDB Schematic Example

Delay between Point A to Point B
 $T_{ab} = Td1 - Td_{fb} + SPO + T_{skew}$

Where

$Td1$ = trace delay of the outputs

Td_{fb} = trace delay of feedback path

SPO is static phase offset. SPO is given in the data sheet. Ideal SPO should be 0 second

T_{skew} is skew between the outputs. Ideal T_{skew} should be 0 second.

To explain how the output and feedback trace delays affects the overall delay, we assume the SPO and the skew are 0 second.

Case 1) Zero Delay

If $Td1 = Td_{fb}$, then the $T_{ab} = 0$ (zero delay)

Case 2) Delay

If $Td1 > Td_{fb}$, then the $T_{ab} > 0$ (positive delay, or point B clock edge occur lagging point A clock edge)

Case 3) Advance

If $Td1 < Td_{fb}$, then the $T_{ab} < 0$ (negative delay, or point B clock edge occur leading point A clock edge)

The trace delay is approximately 100ps to 175ps per inch. Sometimes, it is difficult to control the trace delay. If possible, adding spare footprint for small value capacitors C4 to C7 will allow delay fine tuning after the board layout. Slightly increase the small C4 value has similar affect of adding delay to the feedback path.

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