HiPerClockS™ Application Note
Power Dissipation
For High Speed LVCMOS Buffer

This application note describes the power dissipation and junction temperature calculation for LVCMOS clock buffers with series termination and parallel termination. ICS8701 is used as an example to describe the calculations. A similar approach can be used for calculating the power dissipation and junction temperature for other clock buffers with LVCMOS drivers.

LVCMOS Power Dissipation for Serial Termination

The total power dissipation ***Pd_total*** is composed of Static Power Dissipation ***Pd_static*** and Dynamic Power Dissipation ***Pd_dynamic***.

Pd_total = Pd_static + Pd_dynamic

Where
Pd_static is static power dissipation under DC conditions
Pd_dynamic is dynamic power dissipation due to clocking.

Static Power Dissipation

Static power dissipation is the power dissipation when the part is not switching. There are two sections in the ICS8701 circuitry, core and output driver. The core circuitry draws current I_{DDI} from the V_{DD} supply. The output driver circuitry draws current I_{DDO} from the V_{DDO} Supply.

The static power dissipation ***Pd_static*** is composed of Core static power dissipation, ***Pd_core_static*** and output driver static power dissipation, ***Pd_drive_static***

Pd_static = Pd_core_static + Pd_drive_static

Where
$Pd\_core\_static = I_{DDI} * V_{DD}$
$Pd\_drive\_static = I_{DDO} * V_{DDO}$

Since the supply current I_{DD} data provided in the data sheet is the sum of I_{DDI} and I_{DDO}

$I_{DD} = I_{DDI}+I_{DDO}$

For $V_{DD} = V_{DDO}$, the total static power can be calculated as

$Pd\_static = V_{DD}*I_{DD}$

Dynamic Power Dissipation

Dynamic power dissipation ***Pd_dynamic*** is composed of ***Pd_drive_dynamic*** and ***Pd_Rout***. For ICS8701, frequency has a very small effect on the core supply current I_{DDI}. To simplify the calculation, using the worst case I_{DDI} in the static power dissipation covers the core dynamic power dissipation. The dynamic core power dissipation is not required to be included in this section. Serial termination scheme is used as an example to calculate the dynamic power dissipation.

Pd_dynamic = Pd_drive_dynamic + Pd_Rout

Pd_output_dynamic is the power dissipation within the output driver circuitry and can be calculated as

$$Pd\_drive\_dynamic = Cpd * (V_{DDO})^2 * F * N\_out$$

Where
Cpd is Power dissipation capacitor per output
F is driver clock frequency
N_out is total number of outputs enable. For 8701, N_out = 20
V_{DDO} is output power supply voltage.

Pd_Rout is power dissipation on the output impedance due to loading condition. For series termination as shown in Figure 1, the output current will hold the peak current for a short period of time. The duration depends on the time delay of the transmission line Td.

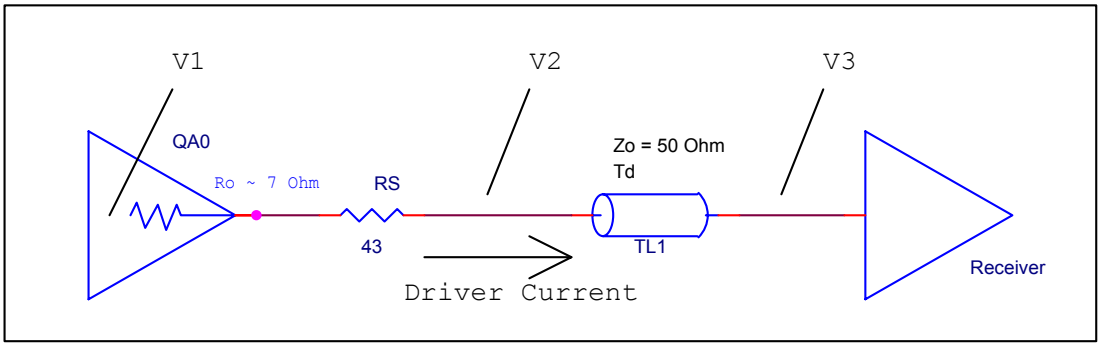

Figure 1 LVCMOS output Series Termination

Figure 2 shows the timing diagram for the load current, related voltages on each point, and the power dissipation on Ro. For Td < ¼ T, (where T is clock period), during each clock period, the load current will hold the peak load current ***I_load_peak*** for a duration of 2xTd for PMOS ON, NMOS OFF and additional 2xTd for PMOS OFF and NMOS ON. Calculating the power dissipation on the clock buffer chip due to the load current should not include the power dissipation on the loading. This element should only include power dissipation on the output resistor R_O.

$$Pd\_Rout = [I\_load\_peak]^2 * R_O * 2 * (2*Td/T) * N\_load$$

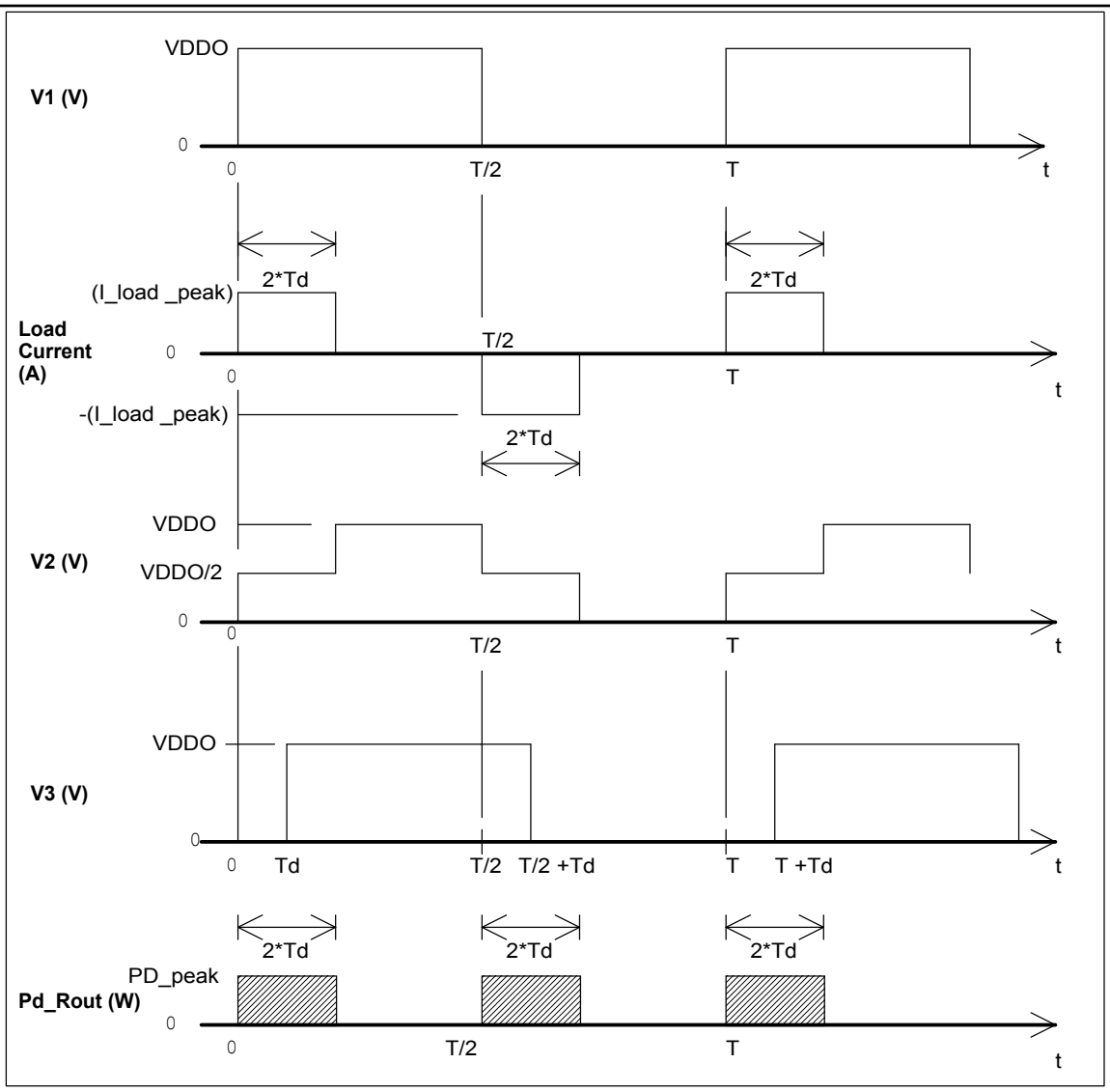

Figure 2 Time Diagram for Voltage, Load Current and Power Dissipation on Rout

For series termination, $R_O + R_S = Z_O$, the peak load current is

$I\_load\_peak = V_{DDO}/(2*Z_O)$

The peak power dissipation on R_O is

$Pd\_peak = (I\_load\_peak)^2 * R_O$

The peak power Pd_peak will hold for 4*Td per clock period. Therefore the total average power dissipation for all N_load is

$Pd\_Rout = [V_{DDO}/(2*Z_O)]^2 * R_O * (4*Td/T) * N\_load$

Where
Td is the time delay for the transmission line
T is clock period
Z_O is characteristic impedance of the transmission line.
N_load is number of output being loaded with series termination

Summary

Power Dissipation

To calculate Power Dissipation for series terminations

$$Pd\_total = Pd\_static + Pd\_dynamic$$
$$= Pd\_core\_static + Pd\_drive\_static + Pd\_drive\_dynamic + Pd\_Rout$$

Where,

$$Pd\_core\_static = I_{DD} * V_{DD}$$
$$Pd\_drive\_static = I_{DDO} * V_{DDO}$$
$$Pd\_drive\_dynamic = Cpd * F * (V_{DDO})^2 * N\_out$$

For transmission line delay Td less than ¼ T, clock time period

$$Pd\_Rout = [V_{DDO}/(2*Z_O)]^2 * R_O * 2 * (2*Td/T) * N\_load$$

Junction Temperature

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pads and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125 °C

$$T_j = T_A + \theta_{AJ} * P\_Total$$

Where,
T_A is ambient temperature
θ_{AJ} is thermo resistance

Example:

For ICS8701 with series termination,

All outputs enabled and loaded with one to one series termination.
Z_O = 50 Ohm, Td = 1 nsec,
Clock frequency, F = 100 MHz (or time period, T=10 nsec)

$R_S = Z_O – R_O$ = 50 Ohm – 7 Ohm = 43 Ohm
V_{DD}max =V_{DDO}max =3.465V

To calculated maximum static power dissipation, the power supply current I_{DD} given in the data sheet is combination of core power current I_{DDI} and driver power current I_{DDO}

P_core_static_max = V_{DD}max * I_{DD}max
= 3.465V * 95mA
= 329.2mW

The core static power and the driver static power can be calculated separately using I_{DDI} and I_{DDO}. The I_{DD}_max current can be split to I_{DDI}_max = 50 mA, I_{DDO}_max = 45mA

P_core_static_max = I_{DD}*V_{DD} = 50 mA * 3.465V = 173.3 mW
P_drive_static_max = I_{DDO}*V_{DDO} = 45mA * 3.465V = 155.9 mW
P_static = P_core_static_max + P_drive_static_max = 329.2 mW

Dynamic power dissipation

Cpd_max = 15pF
Pd_dynamic_max = Cdp_max * Fclk * (V_{DDO}_max)^2 * N_out
= 15 pF * 100MHz * (3.465V)^2 * 20
= 360 mW

Pd_Rout = [V_{DDO}/(2*Z_O)]^2 * R_O * 2 * (2*Td/T) * N_load
= [3.465V/(2*50 Ohm)]^2 * 7 * 2* (2* 1nsec/10nsec) * 20
= 67.2 mW

Pd_total = 756.4 mW

Junction Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{AJ} must be used. Assuming a moderate airflow of 200 linear feet per minute and a multi-layer board, the appropriate value for ICS8701 is 42.1 °C/W shown in the data sheet. The Tj for an ambient temperature of T_A = 70 °C for this example is

$T_j = T_A + P\_Total*\theta_{AJ}$

= 70 °C + 0.756 W * 42.1 °C/W
= 101.8 °C

Tj should be kept below 125 °C.

Figure 3 and Figure 4 show charts of the power dissipation and junction temperature for ICS8701 under the following environment:

Transmission line delay Td = 1ns
V_{DD} =3.465V
V_{DDO} = 3.465V
Z_O = 50 Ohm
R_S = 43 Ohm

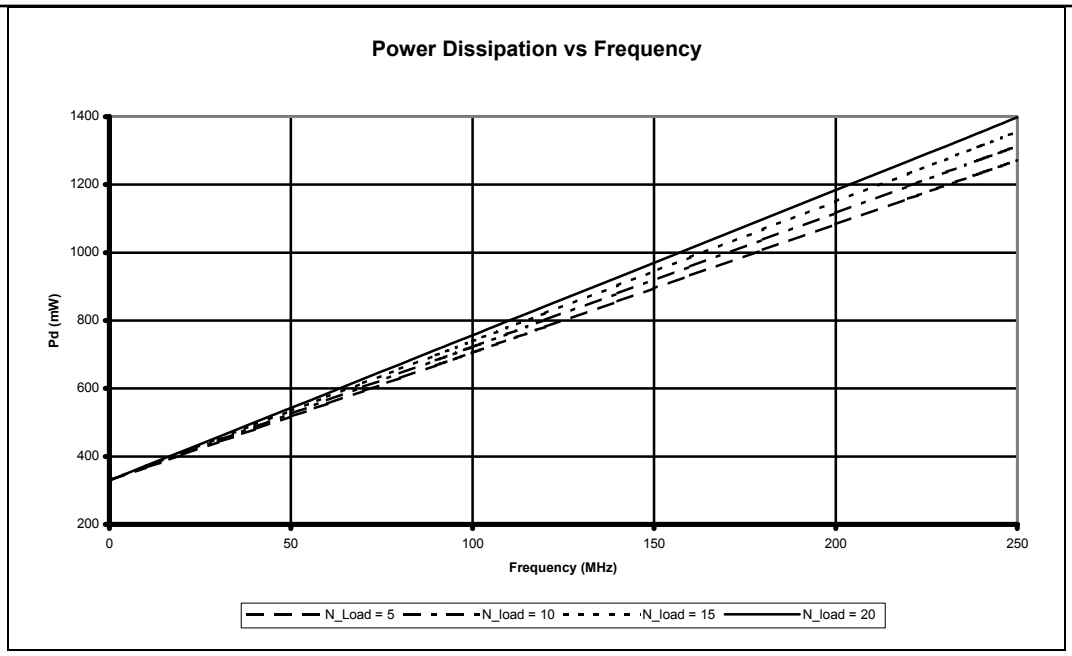

Figure 3 ICS8701 Power Dissipation for Series Termination vs Clock Frequency

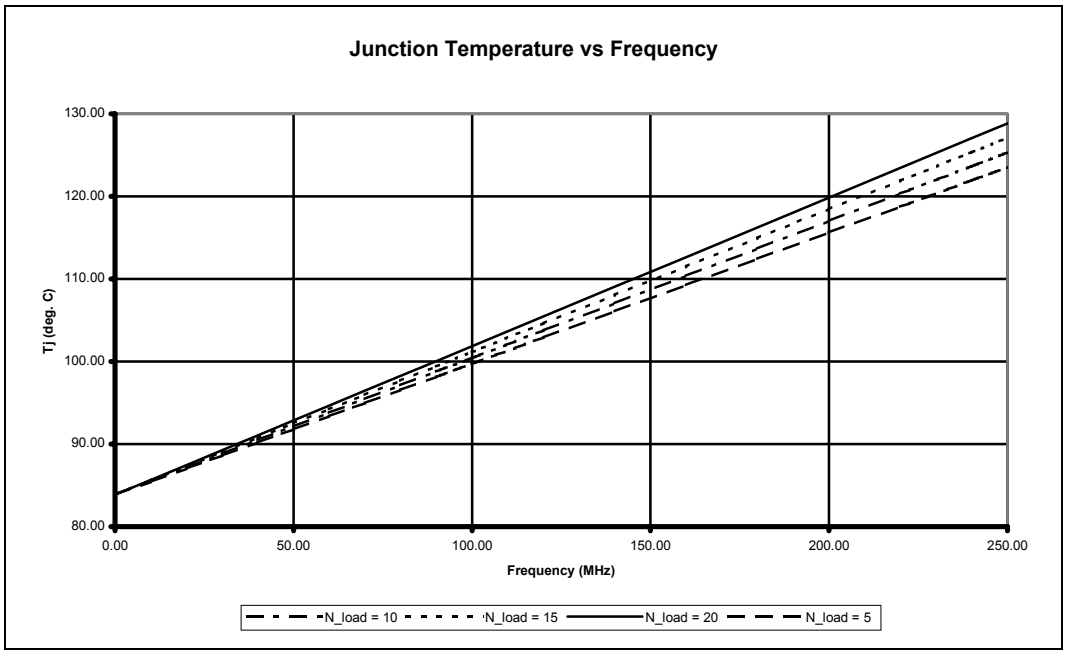

Figure 4 Junction Temperature vs Clock Frequency

LVCMOS Power Dissipation for Parallel Termination

Figure 5 shows a parallel termination that configure for characterization. In actual application, the Figure 6 is an equivalent termination of the Figure 5. Both circuit and have equal result of power dissipation on the buffer. This section, Figure 5 is used for calculation.

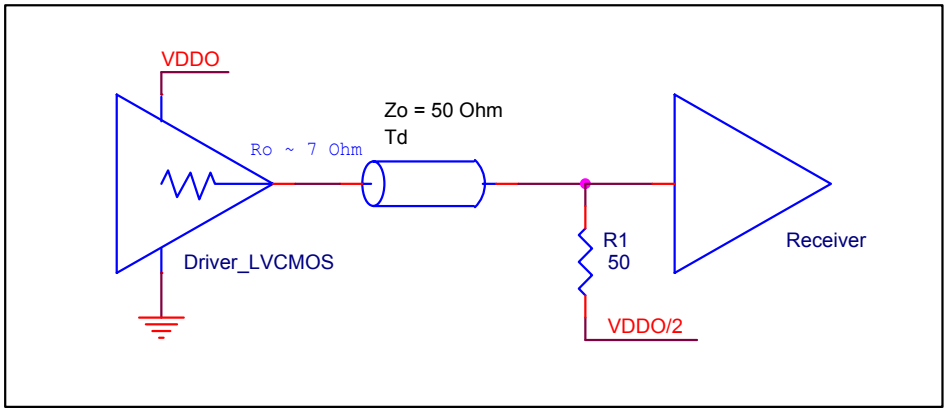

Figure 5 LVCMOS Driver Standard Parallel Termination

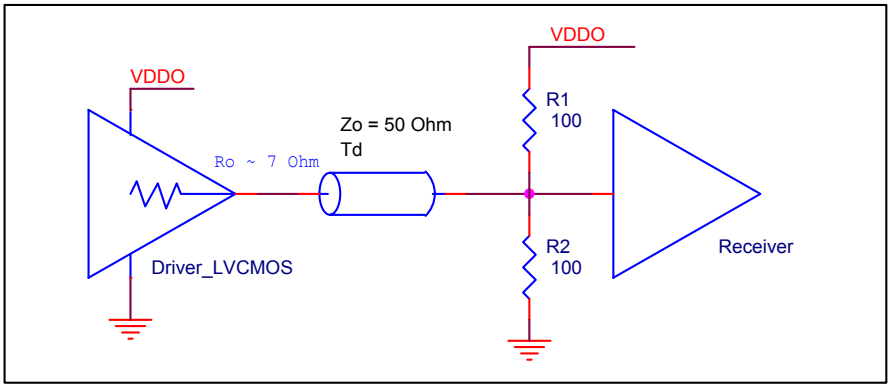

Figure 6 LVCMOS Driver Equivalent Parallel Termination

To calculate Power Dissipation for parallel terminations

Pd_total ***= Pd_static + Pd_dynamic***
= Pd_core_static + Pd_drive_static + Pd_drive_dynamic + Pd_Rout

The ***Pd_core_static, Pd_drive_static and Pd_drive_dynamic*** are same as the results obtained from serial termination.

Pd_Rout is power dissipation on the output impedance due to loading condition. For parallel matched load termination with characteristic impedance Z_O, the driver "sees" the loading impedance of Z_O. The power ***Pd_Rout*** dissipates at PMOS when the output is logic high, and the power dissipated at NMOS when the output is logic low.

$$Pd\_Rout = [(V_{DDO}/2)/(Rout+Z_O)]^2 * R_O * N\_load$$

Where
R_O is output impedance the LVCMOS driver.
Z_O is characteristic impedance of the transmission line.
N_load is number of output being loaded with series termination

To calculate ***Pd_Rout*** for Parallel termination

Pd_Rout = $[(V_{DDO}/2)/(Rout + Z_O)]^2 * R_O * N\_load$
= $[(3.465V/2)/(7\ Ohm + 50\ Ohm)]^2 * 7 * 20$
= 129.3 mW

For frequency F=100MHz, the total power dissipation is

Pd_total = Pd_static + Pd_dymanic + Pd_out
= 329.2 mW + 360 mW + 129.3 mW
= 818.5 mW

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{AJ} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value for ICS8701 is 42.1 °C/W shown in the data sheet. The Tj for an ambient temperature of T_A = 70 °C for this example is

$$T_j = T_A + P\_Total*\theta_{AJ}$$

= 70 °C + 0.819 W * 42.1 °C/W
= 104.4 °C

Tj should be kept below 125 °C.

Figure 7 and Figure 8 show charts of the power dissipation and junction temperature for ICS8701 under the following environment:

V_{DD} =3.465V
V_{DDO} = 3.465V
Z_O = 50 Ohm
R1 = 50 Ohm

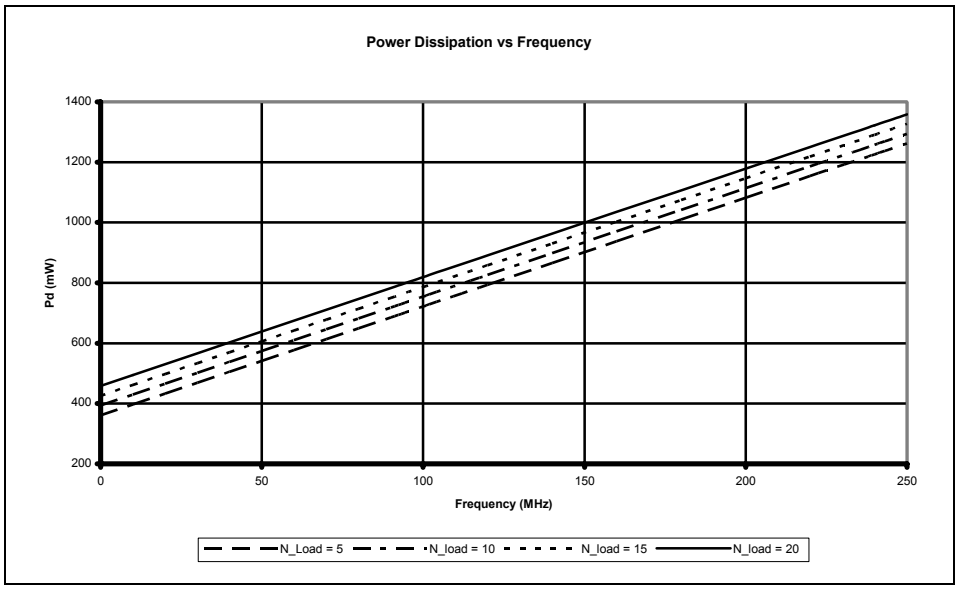

Figure 5 ICS8701 Power Dissipation for Parallel Termination vs Clock Frequency

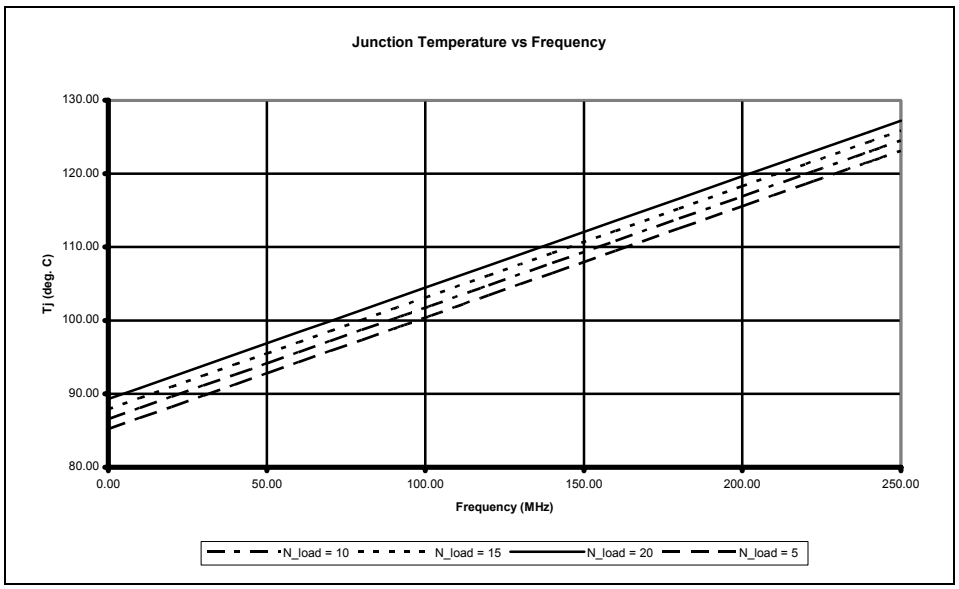

Figure 6 Junction Temperature for Parallel Termination vs Clock Frequency

Writte By: Ming Lim
Any comments, please send e-mail to ming@icst.com

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.