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M16C/64A, M16C/65 Group

Multi-Master I^{2}C-bus Interface

1. Abstract

The multi-master I^{2}C-bus interface (I^{2}C interface) is a serial communication circuit based on the I^{2}C-bus data transmit/receive format, and is equipped with arbitration lost detection that makes multi-master communication possible.

This document describes how to use the I^{2}C interface function.

Note: I^{2}C-bus is a trademark of Phillips, Netherlands.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: M16C/64A Group
  M16C/65 Group

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

The I^2C interface is a serial communication circuit based on the I^2C-bus data transmit/receive format, and is equipped with arbitration lost detection and clock synchronous functions.

3.1 General Call

A general call can be detected when the address data is all 0's (1).

Note:

1. The master transmits general call address 00h to all slaves.

3.2 Addressing Format

7-bit addressing format is supported.

Only the 7 high-order bits of the I^2C address register (slave address) are compared with the address data.

3.3 I^2C Interface Related Pins

- SCLMM pins: Clock I/O pins of the I^2C interface.
- SDAMM pins: Data I/O pins of the I^2C interface.

3.4 Selectable Functions

The functions below can be selected when using the I^{2}C interface.

(1) Communication mode
There are four communication modes available when performing data communication:

- Master transmission: Start and stop conditions are generated (master mode). Address and control data are output to the SDA in synchronization with the SCLMM clock generated by the master device.
- Master reception: Data from the transmitting device is received in synchronization with the SCLMM clock generated by the master device.
- Slave transmission: Start and stop conditions generated by the master device are received (slave mode). Control data is output in synchronization with the clock generated by the master device.
- Slave reception: Data from the transmitting device is received in synchronization with the clock generated by the master device.

(2) SCL mode
SCL mode can be selected from the following:

- Standard clock mode: The bit rate can be selected in the range 16.1 to 100 kHz.
- High-speed clock mode: The bit rate can be selected in the range 32.3 to 400 kHz.

(3) ACK clock
ACK clock can be selected from the following:

- ACK clock not available: No ACK clocks are generated after a data transfer.
- ACK clock available: The master generates an ACK clock each time 1 byte of data is transferred.

(4) Data format
Data format can be selected from the following:

- Addressing format: The received slave address and bits SAD6 to SAD0 in the S0Di register are compared. (i = 0 to 2). When an address match is found, or when a general call is received, an interrupt request is generated and additional data is transmitted and received.
- Free data format: An interrupt request is generated and additional data is transmitted and received regardless of the received slave address.

4. Data Transmit/Receive Example

The data transmit/receive examples are described in this section. The conditions for the examples are below.

- Slave address: 7 bits
- Data: 8 bits
- ACK clock available
- Standard clock mode, bit rate: 100 kbps (fIIC: 20 MHz; fVIIC: 4 MHz)
  20 MHz (fIIC) divided-by-5 = 4 MHz (fVIIC),
  4 MHz (fVIIC) divided-by-8 and further divided-by-5 = 100 kbps (bit rate).
- In receive mode, ACK is returned for data other than the last data. NACK is returned after the last data is received.
- When receiving data, I^{2}C-bus interrupt at the eighth clock (before the ACK clock): Disabled
- Stop condition detection interrupt: Enabled
- Timeout detection interrupt: Disabled
- Set own slave address to the S0D0 register (do not use registers S0D1 or S0D2).

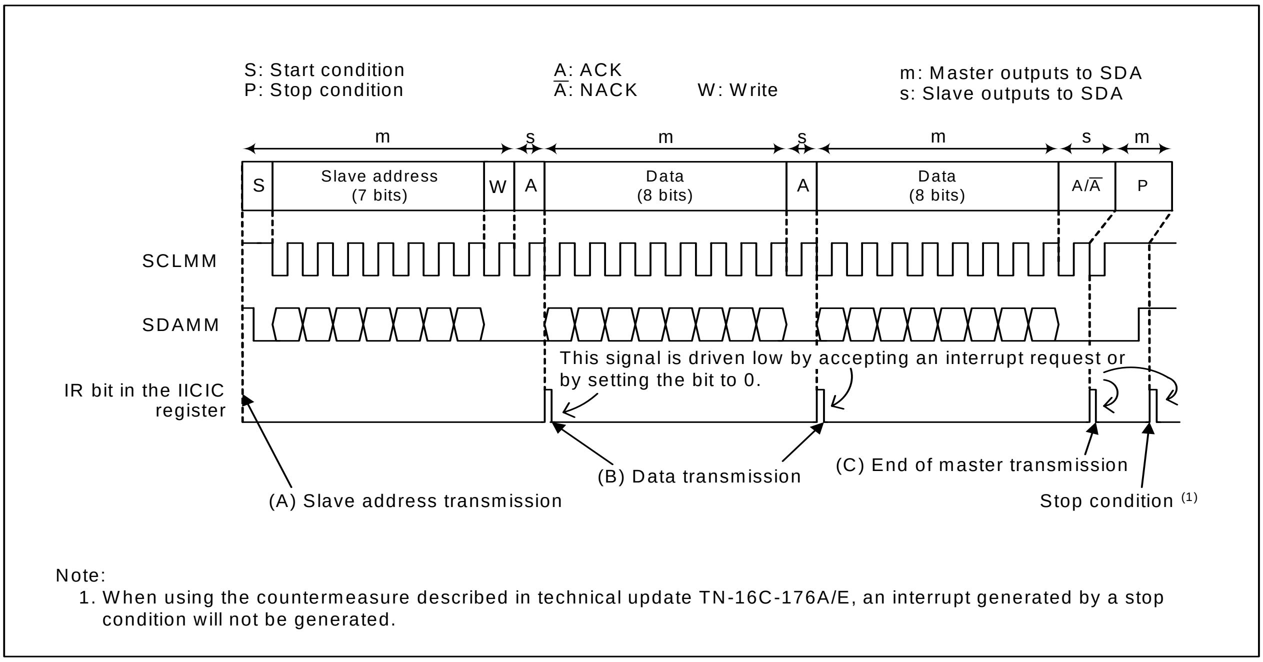
While receiving data, if an interrupt is enabled at the eighth clock, ACK or NACK can be set after each byte of received data is checked.

4.1 Initial Settings

Follow the initial setting procedures below for 4.2 Master Transmission to 4.5 Slave Transmission.
(1) Write own slave address to bits SAD6 to SAD0 in the S0D0 register.
(2) Write 85h to the S20 register (CCR value: 5, standard clock mode selected, ACK clock available).
(3) Write 18h to the S4D0 register (fVIIC: fIIC divided-by-5, timeout detection, interrupt disabled).
(4) Write 01h to the S3D0 register (while receiving data, an I^{2}C-bus interrupt is disabled at the eighth clock (before the ACK clock) and a stop condition detection interrupt is enabled).
(5) Write 0Fh to the S10 register (slave receive mode).
(6) Write 98h to the S2D0 register (SSC value: 18h; start/stop condition generation timing: long mode).
(7) Write 08h to the S1D0 register (bit counter: 8, I^{2}C interface enabled, addressing format; input level: I^{2}C-bus input).
If the MCU uses a single-master system and the MCU itself is the master, start the initial setting procedures from step (2).

4.2 Master Transmission

Master transmission is described in this section. The initial settings are described in 4.1 Initial Settings.
Initial settings are assumed to be completed. Programs (A) to (C) below refer to (A) to (C) in the following figure.



Note:
1. When using the countermeasure described in technical update TN-16C-176A/E, an interrupt generated by a stop condition will not be generated.

Figure 4.1 Example of Master Transmission

(A) Slave address transmission
- (1) The BB bit in the S10 register must be 0 (bus free).
- (2) Write E0h to the S10 register (start condition standby).
- (3) Write a slave address to the upper 7 bits and set the least significant bit to 0 (start condition generated, then slave address transmitted).

After a stop condition is generated and the BB bit becomes 0, the S10 register is write disabled for 1.5 cycles of fVIIC. Therefore, when writing E0h to the S10 register and a slave address to the S00 register during the 1.5 fVIIC cycles, a start condition is not generated.
When generating a start condition immediately after the BB bit changes from 1 to 0, confirm that both the TRX and MST bits are 1 (transmission mode and master mode) after step (1), and then execute step (2).

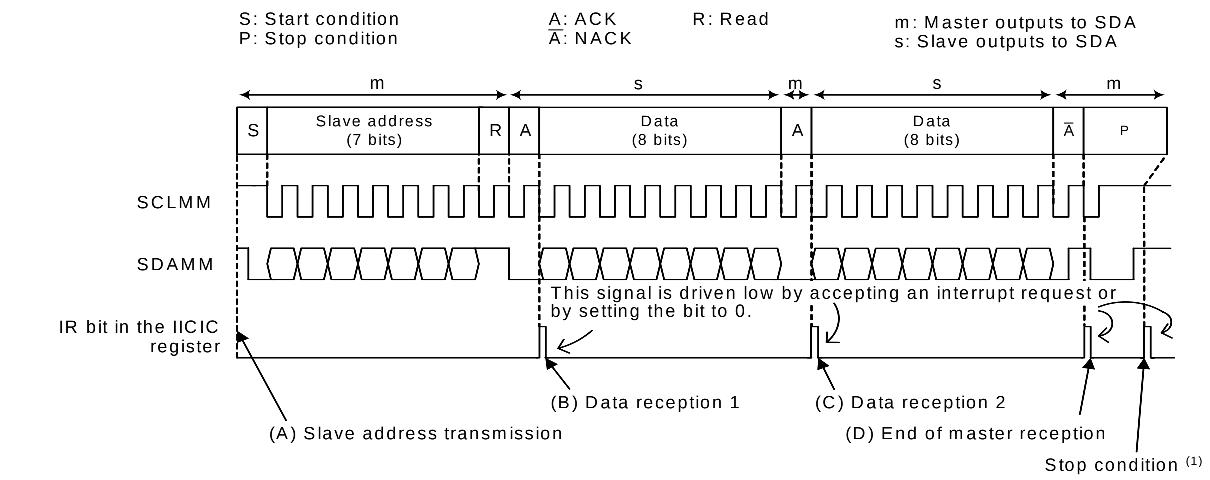
(B) Data transmission (in the I^{2}C-bus interrupt routine)
- (1) Write transmit data to the S00 register (data transmission).

(C) Completion of master transmission (in the I^{2}C-bus interrupt routine)
- (1) Write C0h to the S10 register (stop condition standby).
- (2) Write dummy data to the S00 register (stop condition generated).

When the transmission is completed or ACK is not returned from the slave device (NACK returned), master transmission should be completed as shown in the example above.
If the slave device or other master device drives the SCLMM line low, use the countermeasure described in technical update (TN-16C-176A/E). An I^{2}C-bus interface interrupt generated by a stop condition will not be generated.

4.3 Master Reception

Master reception is described in this section. The initial settings are described in 4.1 Initial Settings.
Initial settings are assumed to be completed. Programs (A) to (D) below refer to (A) to (D) in the following figure.



Note:
1. When using the countermeasure described in technical update TN-16C-176A/E, an interrupt generated by a stop condition will not be generated.

Figure 4.2 Example of Master Reception

(A) Slave address transmission
(1) The BB bit in the S10 register must be 0 (bus free).
(2) Write E0h to the S10 register (start condition standby).
(3) Write a slave address to the upper 7 bits (MSB) and a 1 to the LSB (start condition generated, then slave address transmitted).

(B) Data reception 1 (after slave address transmission) (in the I^{2}C-bus interrupt routine)
(1) Write AFh to the S10 register (master receive mode).
(2) Set the ACKBIT bit in the S20 register to 0 (ACK is available) because the data is not the last one.
(3) Write dummy data to the S00 register.

(C) Data reception 2 (data reception) (in the I^{2}C-bus interrupt routine)
(1) Read the received data from the S00 register.
(2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
(3) Write dummy data to the S00 register.

(D) End of master reception (in the I^{2}C-bus interrupt routine).
(1) Read the received data from the S00 register.
(2) Write C0h to the S10 register (stop condition standby state).
(3) Write dummy data to the S00 register (stop condition generated).

If the slave device or other master device drives the SCLMM line low, use the countermeasure described in technical update TN-16C-176A/E. An I^{2}C-bus interface interrupt generated by a stop condition will not be generated.

4.4 Slave Reception

Slave reception is described in this section. The initial settings are described in 4.1 Initial Settings.
Initial settings are assumed to be completed. Programs (A) to (C) below refer to (A) to (C) in the following diagram.

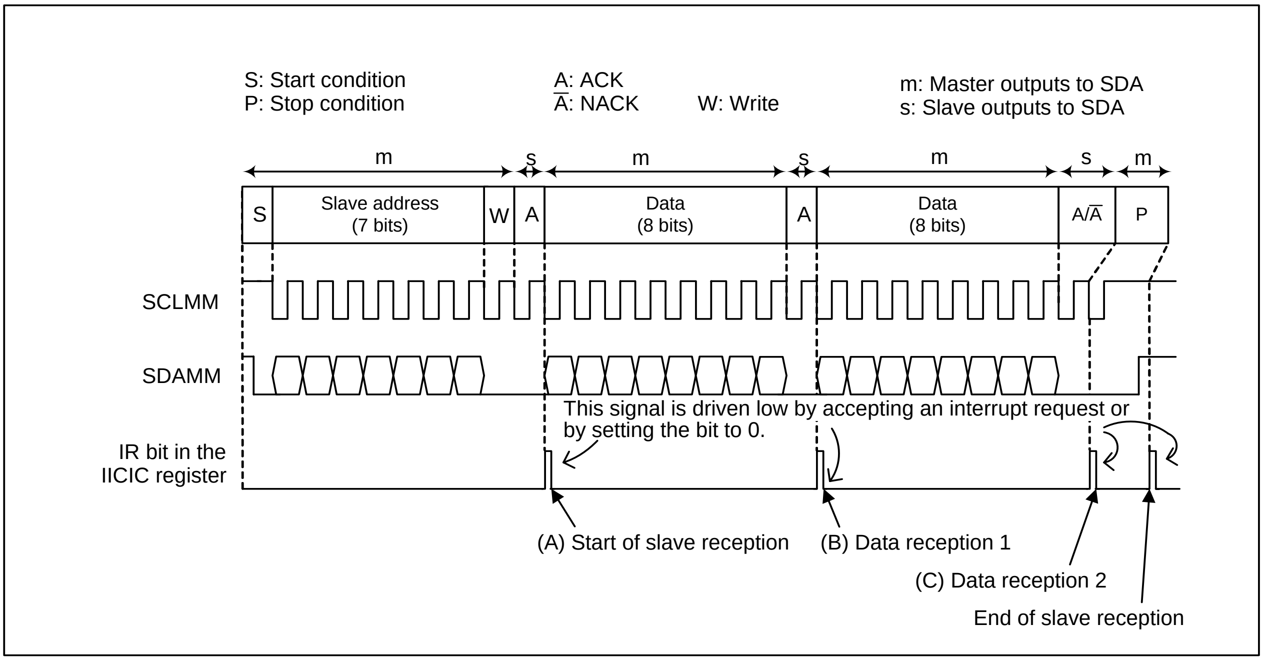


Figure 4.3 Example of Slave Reception

(A) Start of slave reception (in the I^{2}C-bus interrupt routine)
(1) Check the content of S10 register. When the TRX bit is 0, the I^{2}C interface is in slave receive mode.
(2) Write dummy data to the S00 register.

(B) Data reception 1 (in the I^{2}C-bus interrupt routine)
(1) Read the received data from the S00 register.
(2) Set the ACKBIT bit in the S20 register to 0 (ACK is available) because the data is not the last one.
(3) Write dummy data to the S00 register.

(C) Data reception 2 (in the I^{2}C-bus interrupt routine)
(1) Read the received data from the S00 register
(2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
(3) Write dummy data to the S00 register.

4.5 Slave Transmission

Slave transmission is described in this section. The initial settings are described in 4.1 Initial Settings.
Initial settings are assumed to be completed. Programs (A) and (B) below refer to (A) and (B) in the following diagram.
When arbitration lost is detected, the TRX bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, after arbitration lost is detected, read the S00 register. When bit 0 in the S00 register is 1, write 4Fh (slave transmit mode) to the S10 register and execute slave transmission.

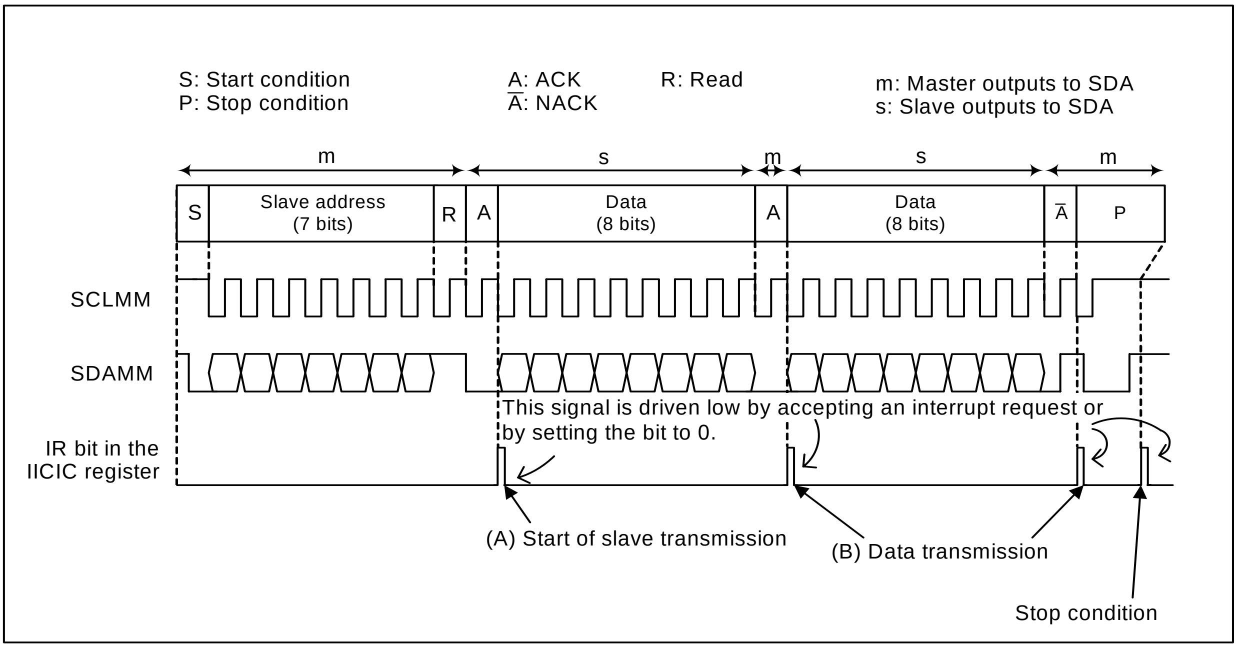


Figure 4.4 Example of Slave Transmission

(A) Start of slave transmission (in the I^{2}C-bus interrupt routine)

(1) Check the content of the S10 register. When the TRX bit is set to 1, the I^{2}C interface is in slave transmit mode.

(2) Write transmit data to the S00 register.

(B) Data transmission (in the I^{2}C-bus interrupt routine)

(1) Write transmit data to the S00 register

Write dummy data to the S00 register even if an interrupt occurs at an ACK clock of the last transmit data. When the S00 register is written, the SCLMM pin becomes high-impedance.

5. Arbitration Lost

The following describes the operation of the I^2C-bus interface when arbitration lost occurs. Figure 5.1 shows the Operation Timing of the Arbitration Lost Detect Flag.

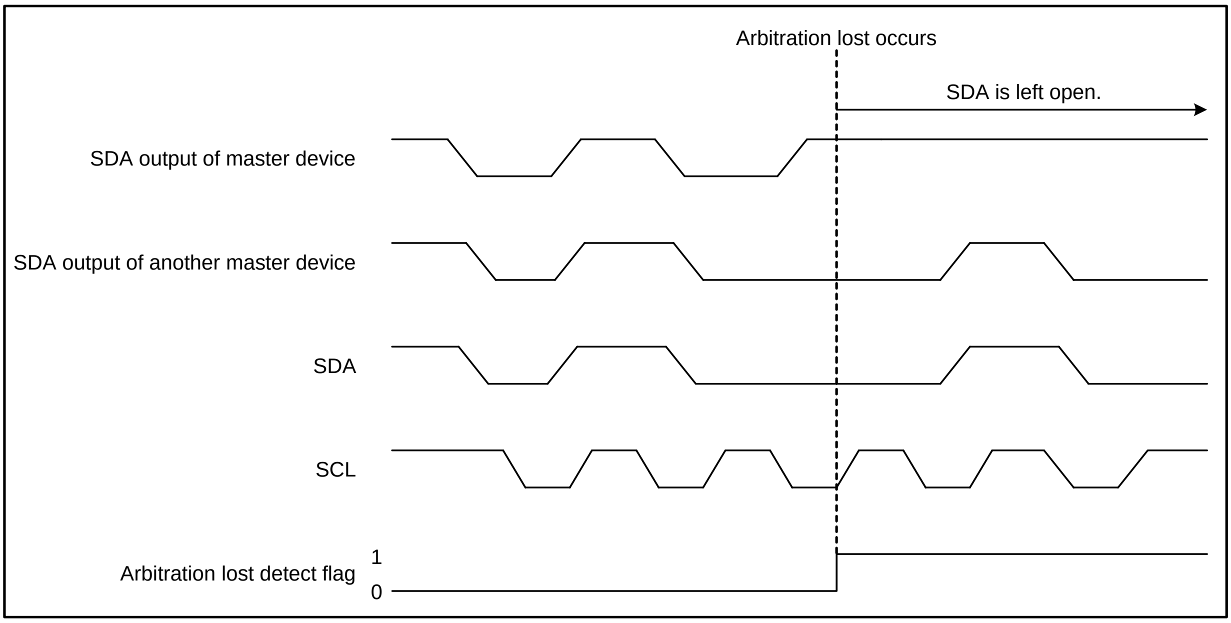

Arbitration lost occurs
SDA is left open.
SDA output of master device
SDA output of another master device
SDA
SCL
Arbitration lost detect flag
1
0

Figure 5.1 Operation Timing of the Arbitration Lost Detect Flag

When arbitration lost occurs, the arbitration lost detect flag becomes 1.

(1) Arbitration lost occurs while transmitting a slave address.
When arbitration lost is detected, the communication mode automatically changes to slave reception enabling the slave address to be received.
If the selected data format is the addressing format, the slave address can be resolved by reading the AAS bit in the S10 register.

(2) Arbitration lost occurs while transmitting data following the slave address.
When arbitration lost is detected, the communication mode automatically changes to slave reception, enabling the data to be received.

6. Interrupt

The I^{2}C-bus interface has the following interrupt sources:

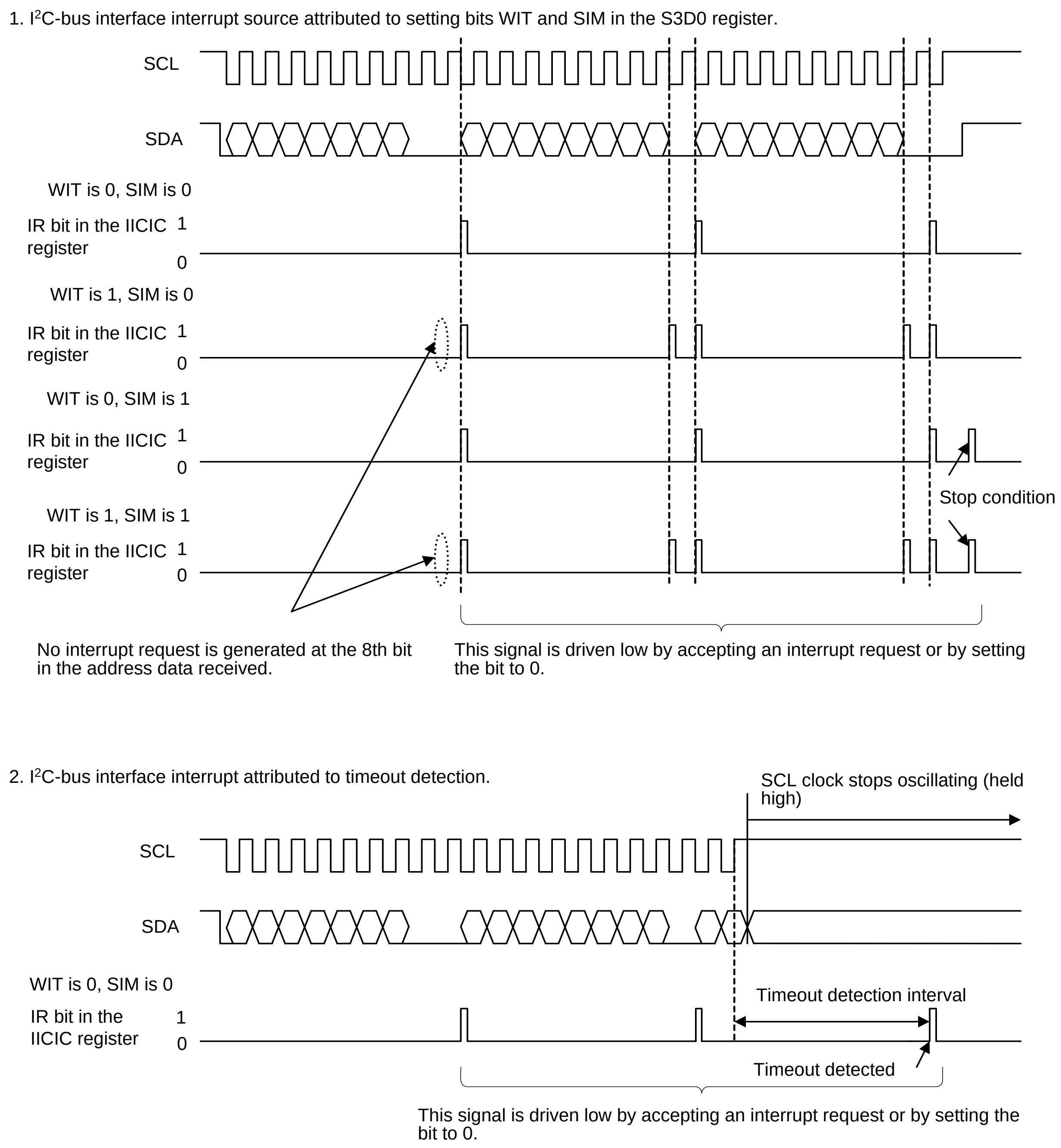
(1) Interrupt when 9-bit transmission/reception is completed (including ACK/NACK)
The interrupt source can be determined by reading the WIT bit in the S3D0 register. When the WIT bit is 0, it is determined that the generated interrupt is attributable to this interrupt source.

(2) Interrupt when 8 bits are received
Setting the WIT bit to 1 enables this interrupt source.
The interrupt source can be determined by reading the WIT bit. When the WIT bit is 1, it is determined that the generated interrupt is attributable to this interrupt source.
If no determination is made of ACK/NACK transmissions, there is no need to use this interrupt.

(3) Interrupt when a stop condition is detected
Setting the SIM bit in the S3D0 register to 1 enables this interrupt source.
The interrupt source can be determined by reading the SCPIN bit in the S4D0 register. When a stop condition is detected, the SCPIN bit becomes 1.

(4) Interrupt when the SCL clock remains high for more than a predetermined time during communication
Setting the TOE bit in the S4D0 register to 1 enables this interrupt source.
The interrupt source can be determined by reading the TOF bit in the S4D0 register. When the SCL clock remains high for more than a predetermined time during communication, the TOF bit becomes 1.

Figure 6.1 shows the I^{2}C-bus Interface Interrupt Request Generation Timing.


1. I2C-bus interface interrupt source attributed to setting bits WIT and SIM in the S3D0 register.
SCL
SDA
WIT is 0, SIM is 0
IR bit in the IICIC register
1
0
WIT is 1, SIM is 0
IR bit in the IICIC register
1
0
WIT is 0, SIM is 1
IR bit in the IICIC register
1
0
Stop condition
WIT is 1, SIM is 1
IR bit in the IICIC register
1
0
No interrupt request is generated at the 8th bit in the address data received.
This signal is driven low by accepting an interrupt request or by setting the bit to 0.
2. I2C-bus interface interrupt attributed to timeout detection.
SCL clock stops oscillating (held high)
SCL
SDA
WIT is 0, SIM is 0
IR bit in the IICIC register
1
0
Timeout detection interval
Timeout detected
This signal is driven low by accepting an interrupt request or by setting the bit to 0.

The above figure assumes the following:
1. The TRX bit in the S10 register is 0 (receive mode).
2. The ACKCLK bit in the S20 register is 1 (ACK is available).

Figure 6.1 I^{2}C-bus Interface Interrupt Request Generation Timing

7. Notes on I^{2}C Interface

7.1 Generating Start Condition

After a stop condition is generated and the BB bit becomes 0 (bus free), the S10 register is write disabled for 1.5 cycles of fVIIC. Therefore, when writing E0h to the S10 register and a slave address to the S00 register during the 1.5 fVIIC cycles, and a start condition is not generated.
When generating a start condition immediately after the BB bit changes from 1 to 0, confirm that both the TRX and MST bits are 1 after step (1), and then execute step (2).

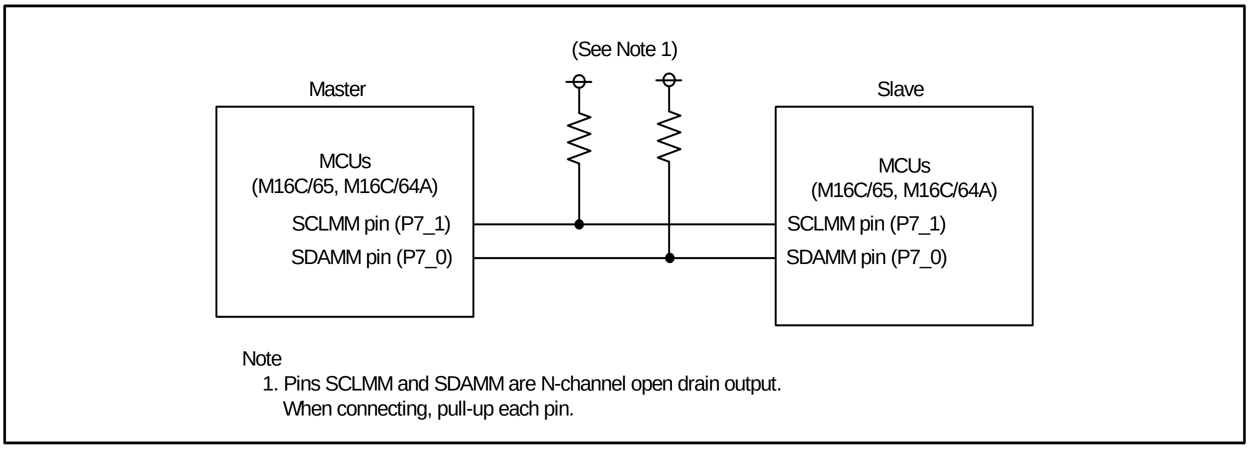
Step:
(1) Write E0h to the S10 register.
The I^{2}C interface enters the start condition standby state and the SDAMM pin is left open.
(2) Write a slave address to the S00 register.
A start condition is generated. Then, the bit counter becomes 000b, the SCL clock signal is output
for 1 byte, and the slave address is transmitted.

8. Sample Program

This sample program is provided for reference purposes only, and is not guaranteed to operate properly in all systems.
When incorporating it into a system, careful examination is recommended before using this sample program.
Furthermore, since its functionality as integral part of a system cannot be evaluated with this program alone, evaluation with the final system is indispensable.

8.1 Connection Example

Figure 8.1 shows the Sample Program Operating Environment.



Note
1. Pins SCLMM and SDAMM are N-channel open drain output.
When connecting, pull-up each pin.

Figure 8.1 Sample Program Operating Environment

8.2 Operation Conditions

Table 8.1 lists the Sample Program Operation Conditions

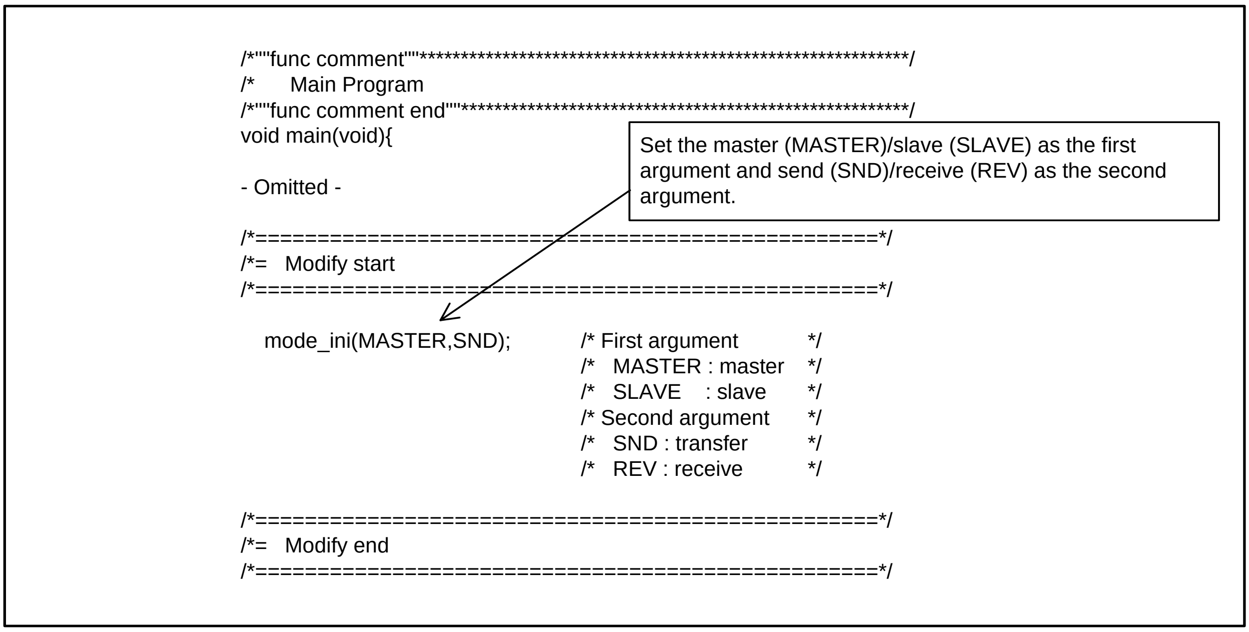
Table 8.1 Sample Program Operation Conditions

Item	Content
Peripheral function clock (fIIC)	24 MHz (XIN: 6 MHz; PLL clock: Divided-by-2, and then multiplied-by-8)
I^{2}C-bus system clock (fVIIC)	4 MHz (fIIC divided-by-6)
Bit rate	100 kbps (fVIIC divided-by-8 and further divided-by-5)
SCL mode	Standard clock mode
Data format	Addressing mode
Slave address compare	S0D0 register only
Stop condition detect interrupt	Enabled
Data receive interrupt	Enabled
Timeout detection function	Enabled

8.3 Sample Program Setting

Four communication modes can be used in the sample program: master transmission, master reception, slave reception, and slave transmission. When calling the “mode_ini” function, the communication modes can be selected by setting arguments.
Set the other slave address and own slave address in define declaration area in the sample program.

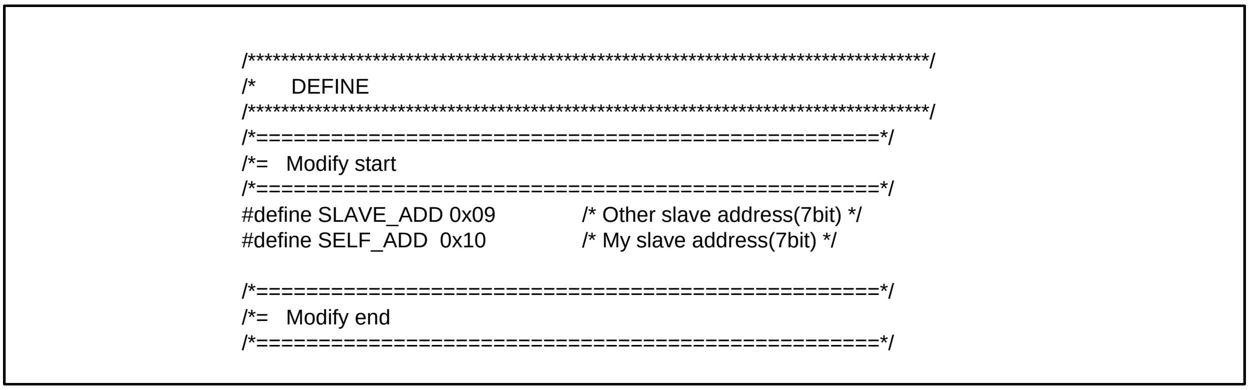
Figure 8.2 shows the Setting Example of Master Transmission. Figure 8.3 shows the Setting Example of Slave Address (0x09) and Own Slave Address (0x10).



```
/*""func comment""**********************************************************/
/*      Main Program
/*""func comment end""******************************************************/
void main(void){

- Omitted -

/*==================================================*/
/*=   Modify start
/*==================================================*/

    mode_ini(MASTER,SND);          /* First argument        */
                                   /*   MASTER : master     */
                                   /*   SLAVE    : slave    */
                                   /* Second argument       */
                                   /*   SND : transfer      */
                                   /*   REV : receive       */

/*==================================================*/
/*=   Modify end
/*==================================================*/
```

Set the master (MASTER)/slave (SLAVE) as the first argument and send (SND)/receive (REV) as the second argument.

Figure 8.2 Communication Mode Setting Example



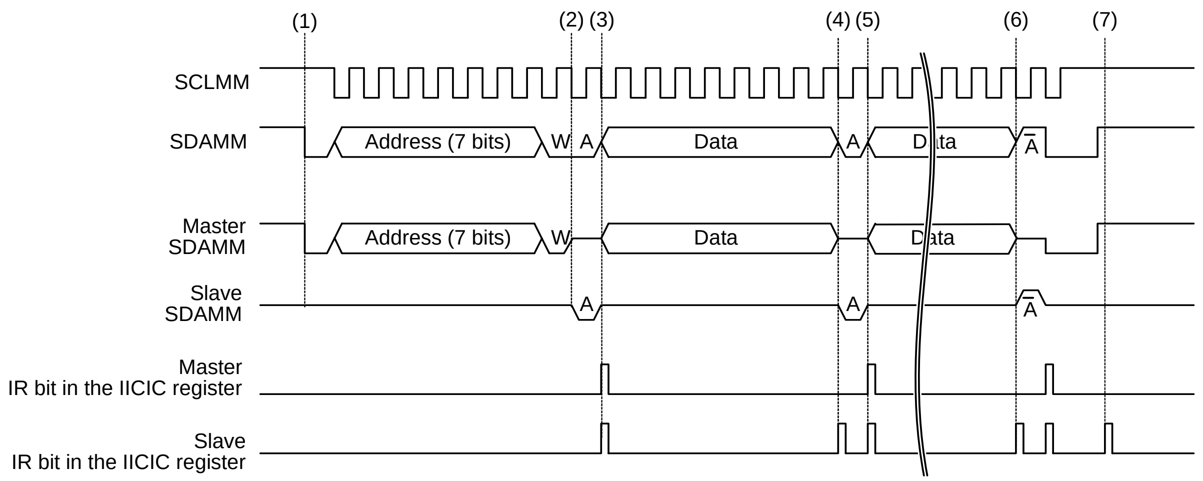
```
/**********************************************************************************/
/*      DEFINE
/**********************************************************************************/
/*==================================================*/
/*=   Modify start
/*==================================================*/
#define SLAVE_ADD 0x09             /* Other slave address(7bit) */
#define SELF_ADD  0x10             /* My slave address(7bit) */

/*==================================================*/
/*=   Modify end
/*==================================================*/
```

Figure 8.3 Slave Address Setting Example

8.4 Operation Example

8.4.1 Master Transmission and Slave Reception

Figure 8.4 shows the Master Transmission and Slave Reception Operation Example

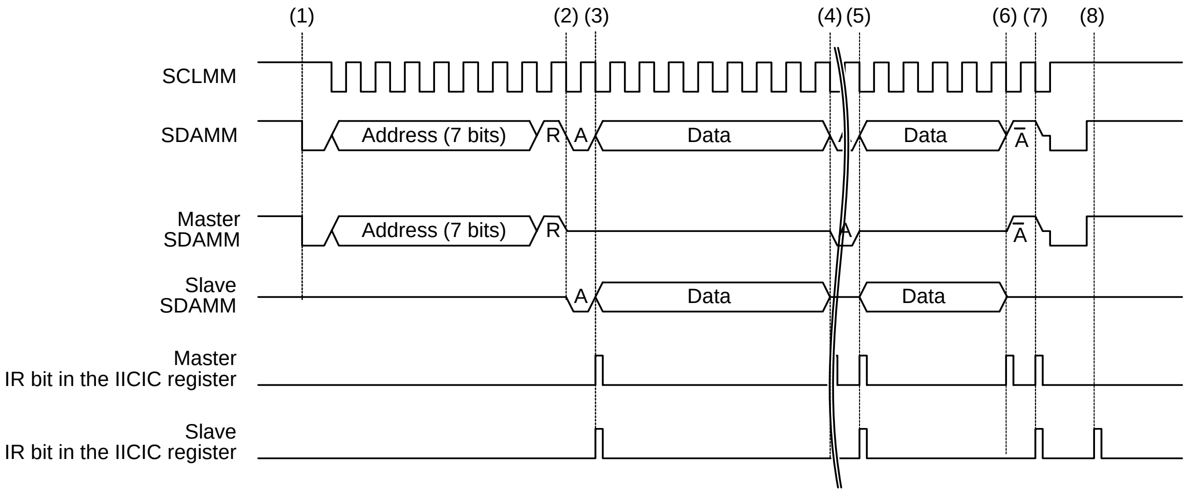


(1) Master: A start condition is generated after writing E0h to the S10 register and transmit data to the S00 register.
(2) Master: The slave address set to bits b7 to b1 in the S00 register and Write("0") set to b0 are output.
Slave: ACK is output when a match is found between the received slave address and the value in the S0Di register.
(3) Master: After ACK reception, the IR bit in the IICIC register becomes 1.
Slave: After ACK transmission, the IR bit becomes 1.
(4) Slave: After data reception, the IR bit becomes 1. During interrupt handling, set the ACKBIT bit to 0 and ACK is output.
(5) Master: After ACK reception, the IR bit becomes 1.
Slave: After ACK transmission, the IR bit becomes 1.
(6) Slave: After receiving 5 bytes, set the ACKBIT bit to 1 and NACK is output.
(7) Master: A stop condition is generated.
The IR bit does not become 1 when a stop condition is generated, by using the countermeasure described in technical update TN-16C-A176A/E.
Slave: When detecting the stop condition, the IR bit becomes 1.

Figure 8.4 Master Transmission and Slave Reception Operation Example

8.4.2 Master Reception and Slave Transmission

Figure 8.5 shows the Master Reception and Slave Transmission Operation



(1) Master: A start condition is generated after writing E0h to the S10 register and transmit data to the S00 register.

(2) Master: The slave address set to bits b7 to b1 in the S00 register and Read("1") set to b0 are output.
Slave: ACK is output when a match is found between the received slave address and the value in the S0Di register.
The TRX bit in the S10 register becomes 1 (transmit mode) (only when the ALS bit in the S1D0 register is 1 (addressing mode)).

(3) Master: After ACK reception, the IR bit in the IICIC register becomes 1.
Slave: After ACK transmission, the IR bit becomes 1.

(4) Slave: After data reception, the IR bit becomes 1. During interrupt handling, set the ACKBIT bit to 0 and ACK is output.

(5) Master: After ACK transmission, the IR bit becomes 1.
Slave: After ACK reception, the IR bit becomes 1.

(6) Slave: After receiving 5 bytes, set the ACKBIT bit to 1 and NACK is output.

(7) Slave: After receiving NACK, the TRX bit becomes 0 (receive mode) only when the ALS bit is 1.

(8) Master: A stop condition is generated.
The IR bit does not become 1 when a stop condition is generated, by using the countermeasure described in technical update TN-16C-A176A/E.
Slave: When detecting the stop condition, the IR bit becomes 1.

Figure 8.5 Master Reception and Slave Transmission Operation

8.5 Function Tables

Declaration	void iic_ini(unsigned char ini, unsigned char sub_address)	
Outline	I^{2}C-bus initialization function	
Argument	Argument name	Meaning
	ini	I^{2}C-bus function enabled/disabled
		ENABLED: I^{2}C-bus function enabled
		DISABLED: I^{2}C-bus function disabled
	sub_address	Slave address setting
Variable (global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_index	For the number of transfers
Returned value	None	
Function	Argument ini = When ENABLED (I^{2}C-bus function enabled), initialize the I^{2}C-bus before enabling interrupts. Argument ini = When DISABLED (I^{2}C-bus function disabled), disable the I^{2}C-bus interface and the I^{2}C-bus interrupt.	

Declaration	void mode_ini(unsigned char ms, unsigned char sr)	
Outline	Function for setting respective communication modes	
Argument	Argument name	Meaning
	ms	Select master or slave
		MASTER: Master SLAVE: Slave
	sr	Select transmission or reception
		SND: Transmission mode REV: Reception mode
Variable (global)	Variable name	Content
	iic_ram[]	Data storage alignment for master transmit
	iic_length	For transmit and receive size
Returned value	None	
Function	Set the respective communication modes.	

Declaration	unsigned char iic_master_start (unsigned char slave, unsigned char sr, unsigned char *buf, unsigned char len)	
Outline	Master start function	
Argument	Argument name	Meaning
	slave	Specified slave address (0x00 to 0x7f)
	sr	Select transmission or reception
		SND: Transmission mode REV: Reception mode
	*buf	Pointer for transmit buffer
	len	Transmit/receive data size (0x00 to 0xff)
Variable (global)	Variable name	Content
	iic_slave	Variable for storing slave address
	iic_length	For transmit and receive size
	iic_pointer	Pointer for transmission buffer
	iic_mode	For selecting communication mode
	iic_rw	READ/WRITE
Returned value	Type	Meaning
	unsigned char	Master start failure/start successful
		FALSE: Master start failure
		TRUE: Master start successful
Function	Transmit the start condition and slave address after master setting.	

Declaration	void master_transfer(void)	
Outline	Master transmit function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_length	For transmit and receive size
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	Detect arbitration lost, confirming ACK/NACK reception, and transmitting data.	

Declaration	void master_receive(void)	
Outline	Master receive function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_length	For transmit and receive size
	iic_pointer	Receive buffer pointer
Returned value	None	
Function	Detecting arbitration lost, transmitting ACK/NACK, and receiving data.	

Declaration	void slave_receive(void)	
Outline	Slave receive function	
Argument	None	
Variable (global)	Variable name	Content
	iic_length	For transmit and receive size
	iic_index	Number of transfers
	iic_pointer	Receive buffer pointer
Returned value	None	
Function	Receive data and transmit ACK/NACK.	

Declaration	void slave_transfer(void)	
Outline	Slave transmit function	
Argument	None	
Variable (global)	Variable name	Content
	iic_length	For transmit and receive size
	iic_index	Number of transfers
	iic_pointer	Transmit buffer pointer
Returned value	None	
Function	After receiving ACK/NACK, transmit data.	

Declaration	void idle_mode(void)	
Outline	Transmit and receive mode select function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting communication mode
Returned value	None	
Function	Select transmit mode or receive mode when receiving data.	

Declaration	unsigned char* select_buffer(unsigned char RW)	
Outline	Function for obtaining transmit and receive buffer addresses	
Argument	Variable name	Meaning
	RW	Select transmit and receive buffer
		0: Slave receive buffer 1: Slave transmit buffer
Variable (global)	None	
Returned value	Type	Meaning
	unsigned char*	Transmit and receive buffer address
Function	Obtain transmit and receive buffer addresses.	

Declaration	void receive_stop_condition(void)	
Outline	Stop condition reception state processing function	
Argument	None	
Variable (global)	Variable name	Content
	iic_mode	For selecting communication mode
	iic_index	Number of transfers
Returned value	None	
Function	Clear the stop condition detection interrupt request bit and initialize the communication mode.	

Declaration	void iic_master_end(unsigned char status)	
Outline	Master control completion function	
Argument	Argument name	Meaning
	status	Status after master control
		0x10: Master transmission completed
		0x11: Arbitration lost is detected during master transmission.
		0x12: NACK is received during master transmission
		0x20: Master reception completed
		0x21: Arbitration lost is detected during master reception.
		0x22: NACK is received during master reception
Variable (global)	None	
Returned value	None	
Function	Carry out the processing after master control is completed. This application note does not include any processing. Add if the need arises.	

Declaration	void iic_slave_end(unsigned char status)	
Outline	Slave control completion function	
Argument	Argument name	Meaning
	status	Status after slave control completed
		0x10: Slave transmission completed
Variable (global)	None	
Returned value	None	
Function	Carry out the processing after slave control is completed. This application note does not include any processing. Add if the need arises.	

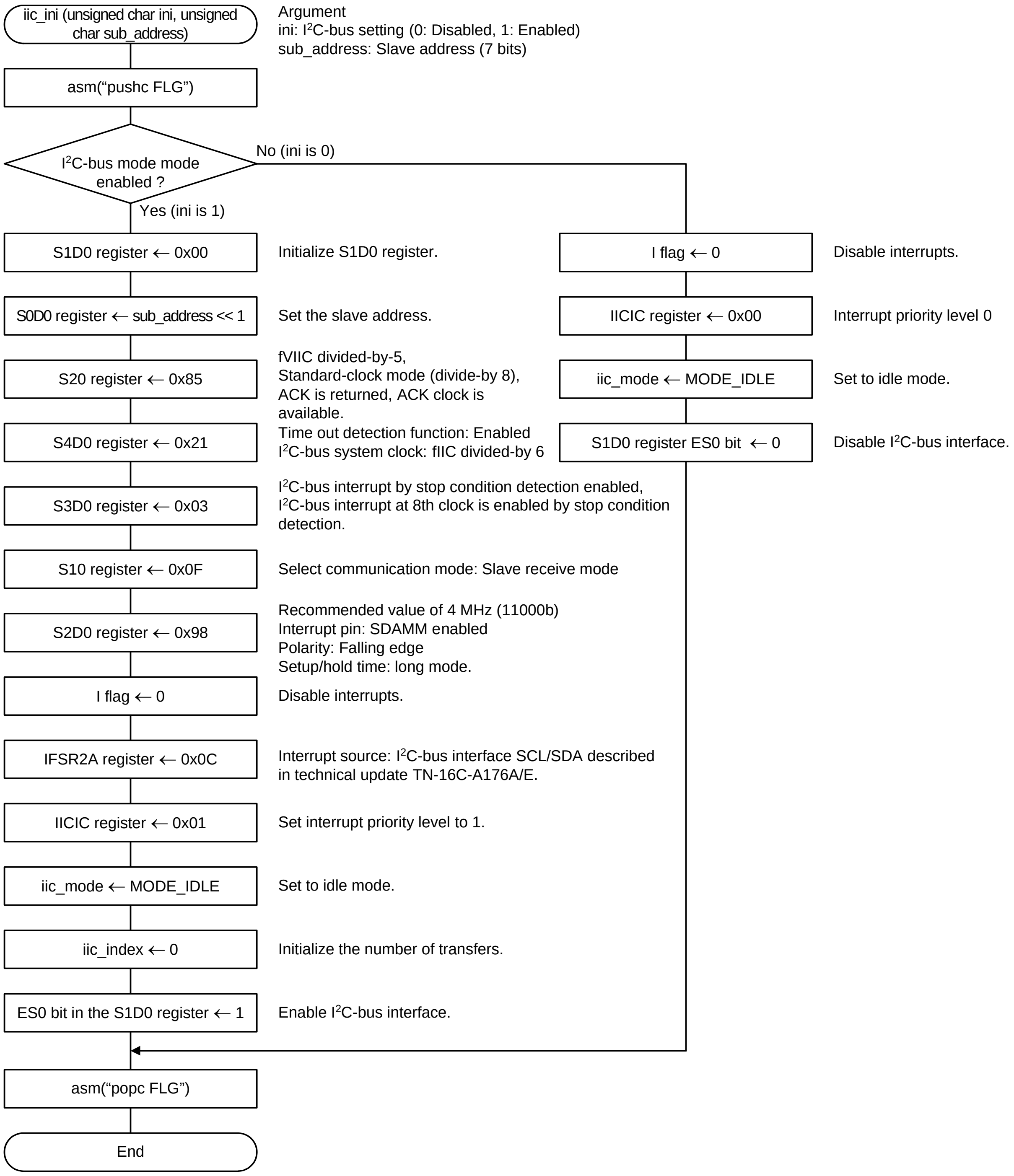
Declaration	void stop_condition(void)
Outline	Stop condition generation function
Argument	None
Variable (global)	None
Returned value	None
Function	A stop condition is generated using the countermeasure described in technical update TN-16C-176A/E.

Declaration	void soft_wait(unsigned int time)	
Outline	Software wait function	
Argument	Argument name	Meaning
	time	Wait time
		SETUP_TIME: Setup time for generating a stop condition WAIT_TIME: Wait time (approx. 5 µs)
Variable (global)	None	
Returned value	None	
Function	Wait time is generated.	

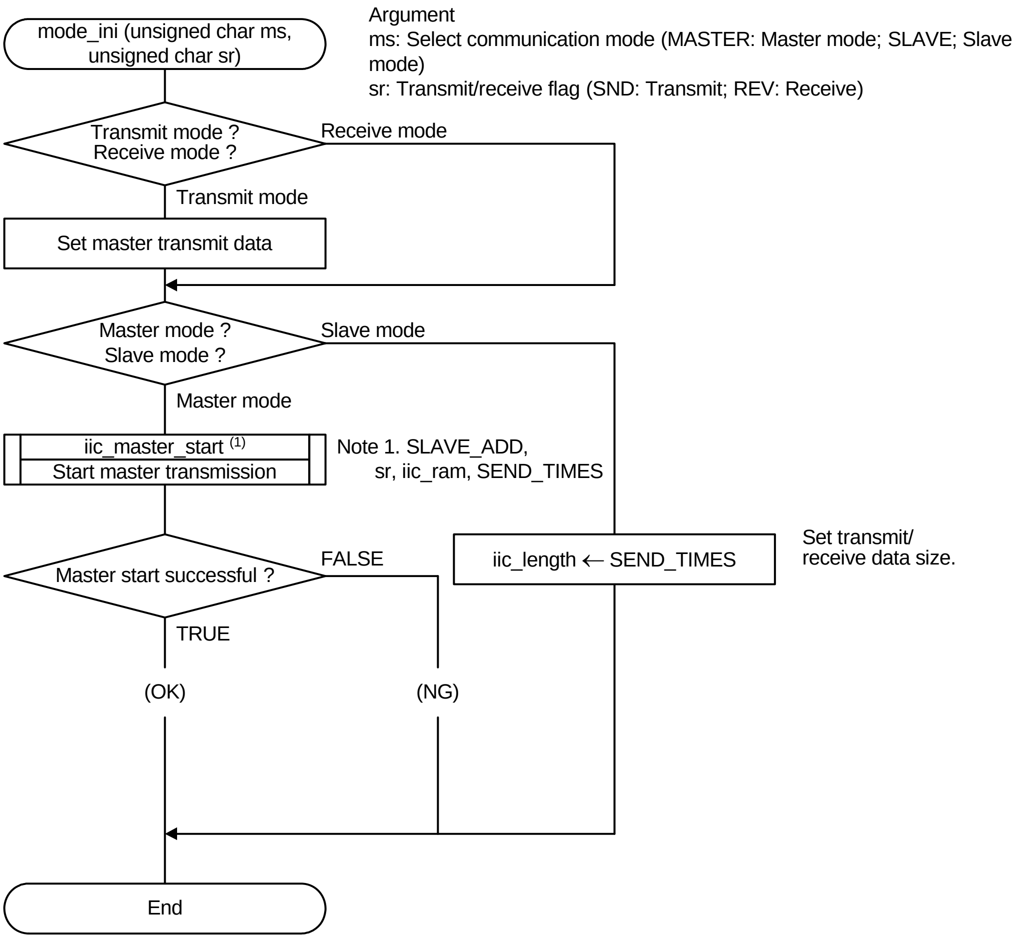
Declaration	void reset_mmi2c(void)
Outline	I^{2}C-bus interface reset function
Argument	None
Variable (global)	None
Returned value	None
Function	Set the SDAMM pin to high and reset the I^{2}C-bus interface.

8.6 Flowcharts

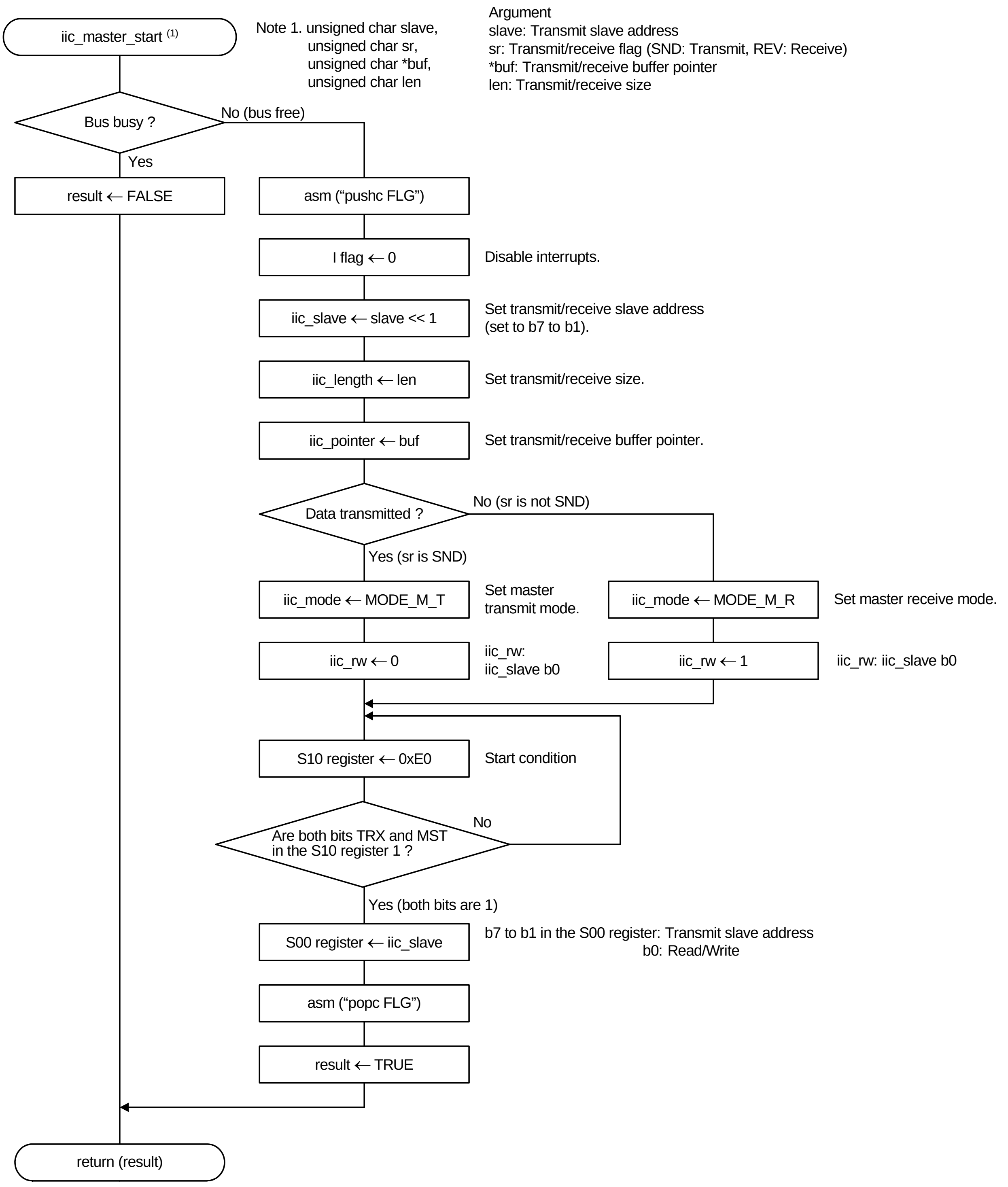
8.6.1 I^{2}C-bus Initialization Function


iic_ini (unsigned char ini, unsigned char sub_address)
Argument
ini: I2C-bus setting (0: Disabled, 1: Enabled)
sub_address: Slave address (7 bits)
asm("pushc FLG")
I2C-bus mode mode enabled ?
No (ini is 0)
Yes (ini is 1)
S1D0 register ← 0x00
Initialize S1D0 register.
S0D0 register ← sub_address << 1
Set the slave address.
S20 register ← 0x85
fVIIC divided-by-5,
Standard-clock mode (divide-by 8),
ACK is returned, ACK clock is available.
S4D0 register ← 0x21
Time out detection function: Enabled
I2C-bus system clock: fIIC divided-by 6
S3D0 register ← 0x03
I2C-bus interrupt by stop condition detection enabled,
I2C-bus interrupt at 8th clock is enabled by stop condition detection.
S10 register ← 0x0F
Select communication mode: Slave receive mode
S2D0 register ← 0x98
Recommended value of 4 MHz (11000b)
Interrupt pin: SDAMM enabled
Polarity: Falling edge
Setup/hold time: long mode.
I flag ← 0
Disable interrupts.
IFSR2A register ← 0x0C
Interrupt source: I2C-bus interface SCL/SDA described in technical update TN-16C-A176A/E.
IICIC register ← 0x01
Set interrupt priority level to 1.
iic_mode ← MODE_IDLE
Set to idle mode.
iic_index ← 0
Initialize the number of transfers.
ES0 bit in the S1D0 register ← 1
Enable I2C-bus interface.
I flag ← 0
Disable interrupts.
IICIC register ← 0x00
Interrupt priority level 0
iic_mode ← MODE_IDLE
Set to idle mode.
S1D0 register ES0 bit ← 0
Disable I2C-bus interface.
asm("popc FLG")
End

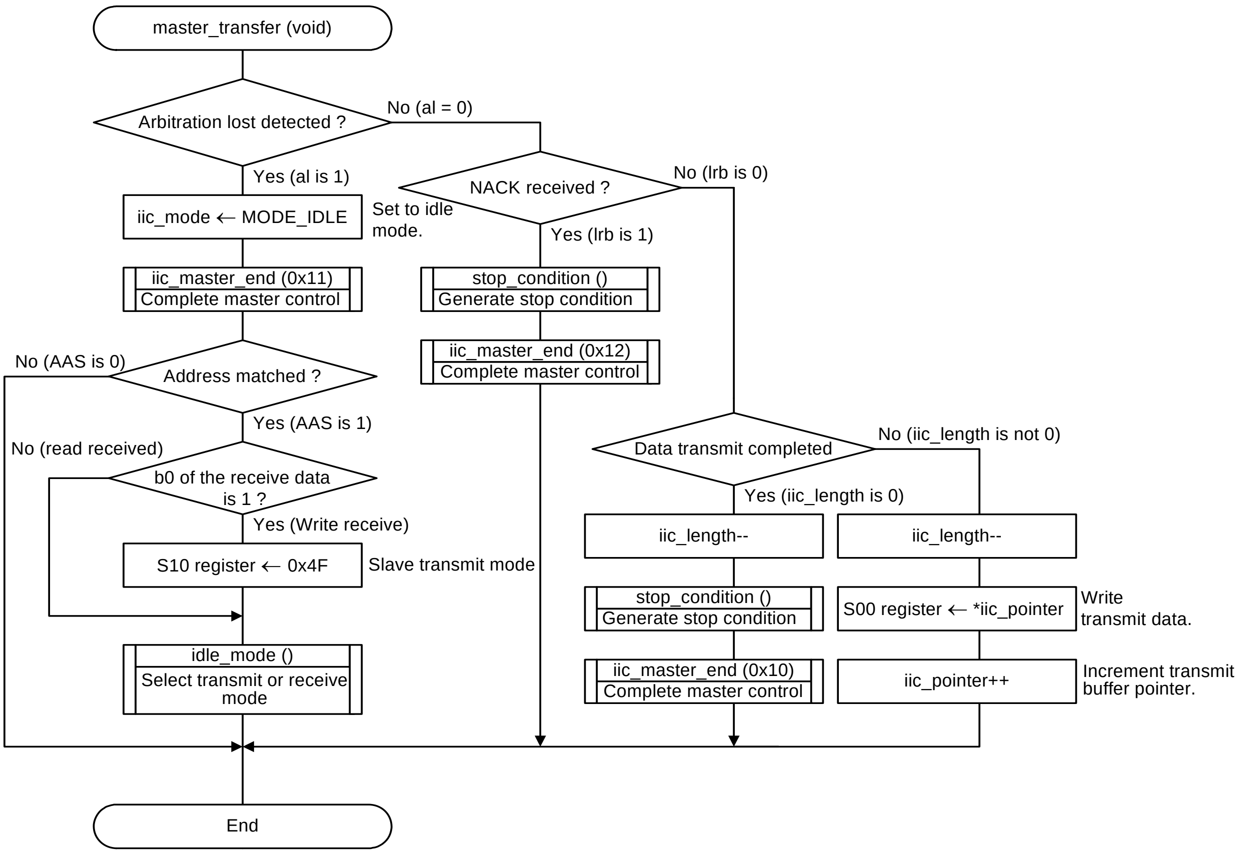
8.6.2 Function for Setting Respective Communication Modes


mode_ini (unsigned char ms, unsigned char sr)
Argument
ms: Select communication mode (MASTER: Master mode; SLAVE; Slave mode)
sr: Transmit/receive flag (SND: Transmit; REV: Receive)
Transmit mode ? Receive mode ?
Receive mode
Transmit mode
Set master transmit data
Master mode ? Slave mode ?
Slave mode
Master mode
iic_master_start (1)
Start master transmission
Note 1. SLAVE_ADD, sr, iic_ram, SEND_TIMES
iic_length ← SEND_TIMES
Set transmit/ receive data size.
Master start successful ?
FALSE
TRUE
(OK)
(NG)
End

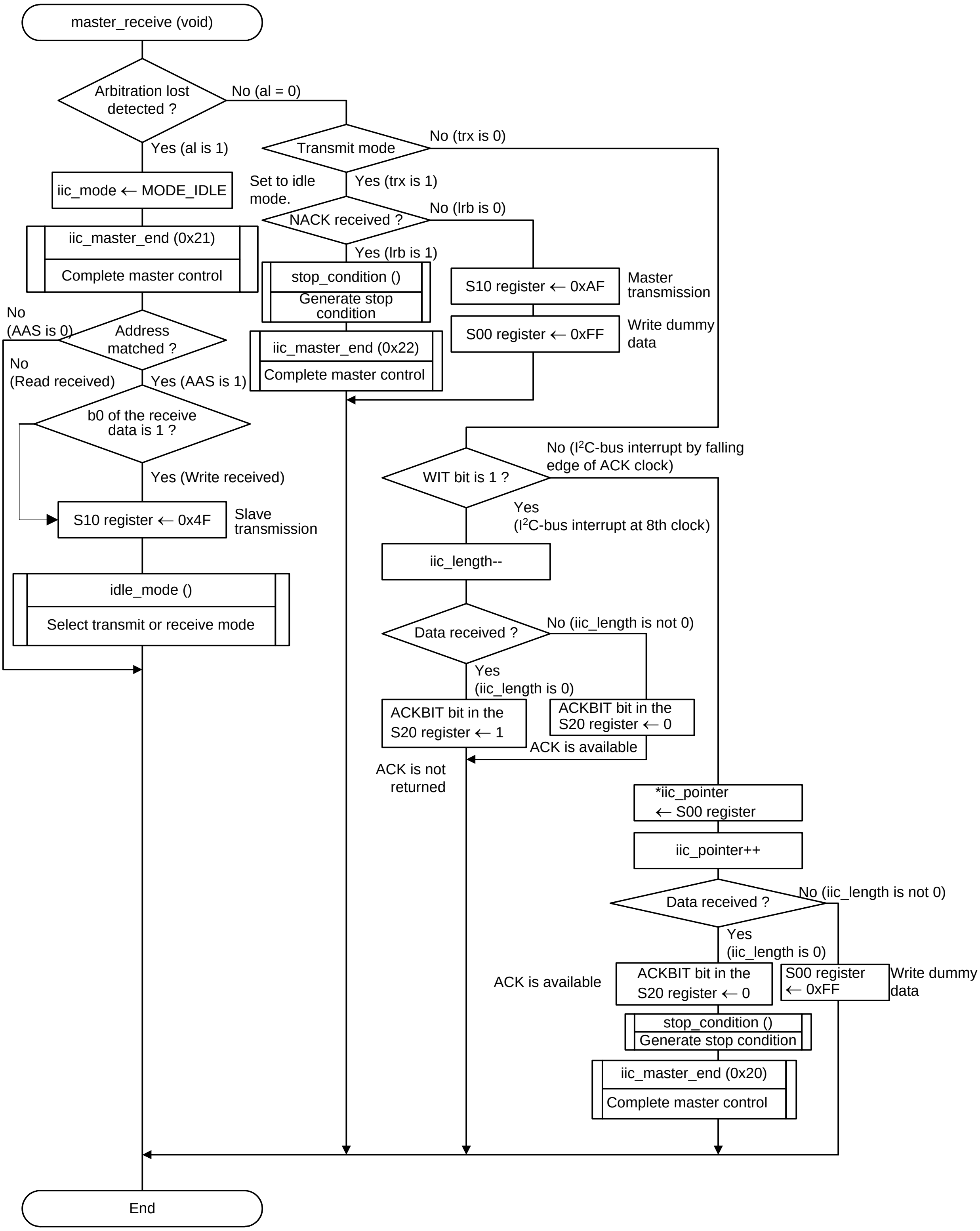
8.6.3 Master Start Function



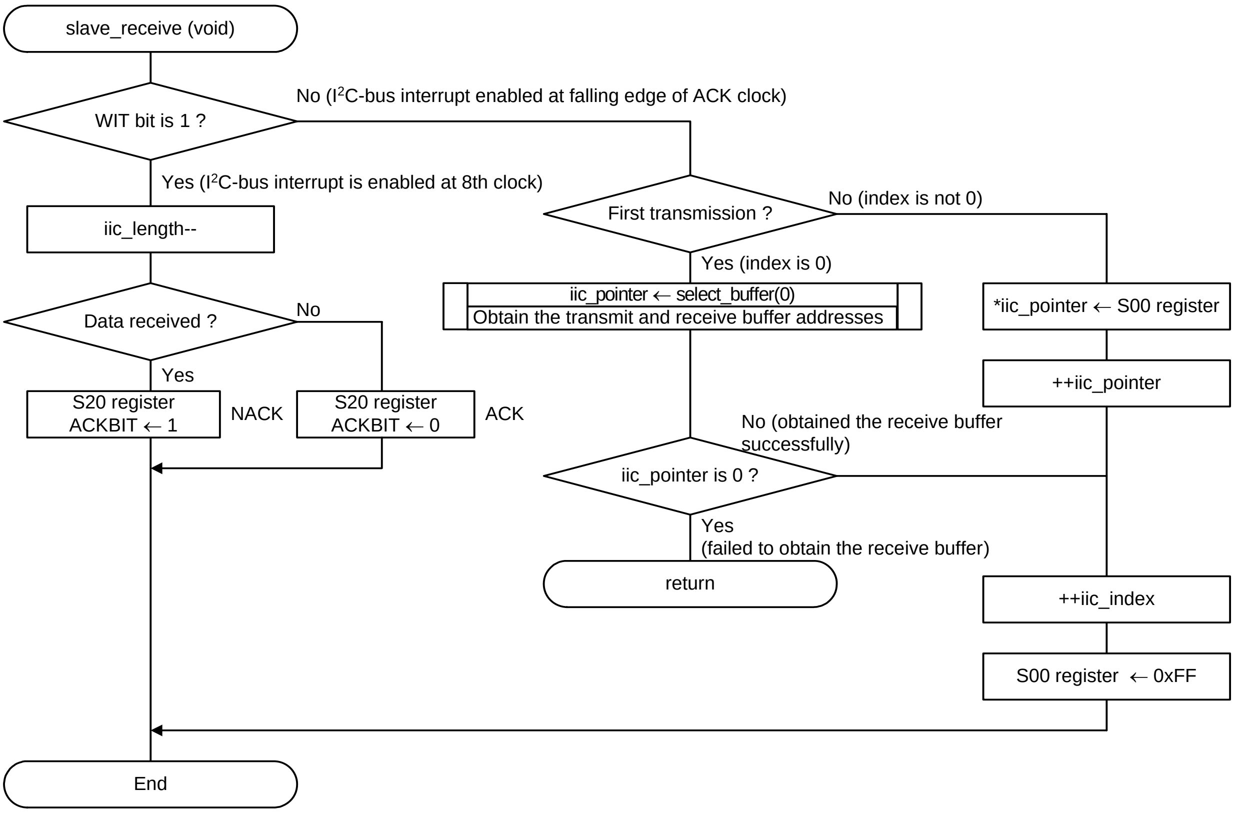
8.6.4 Master Transmit Function



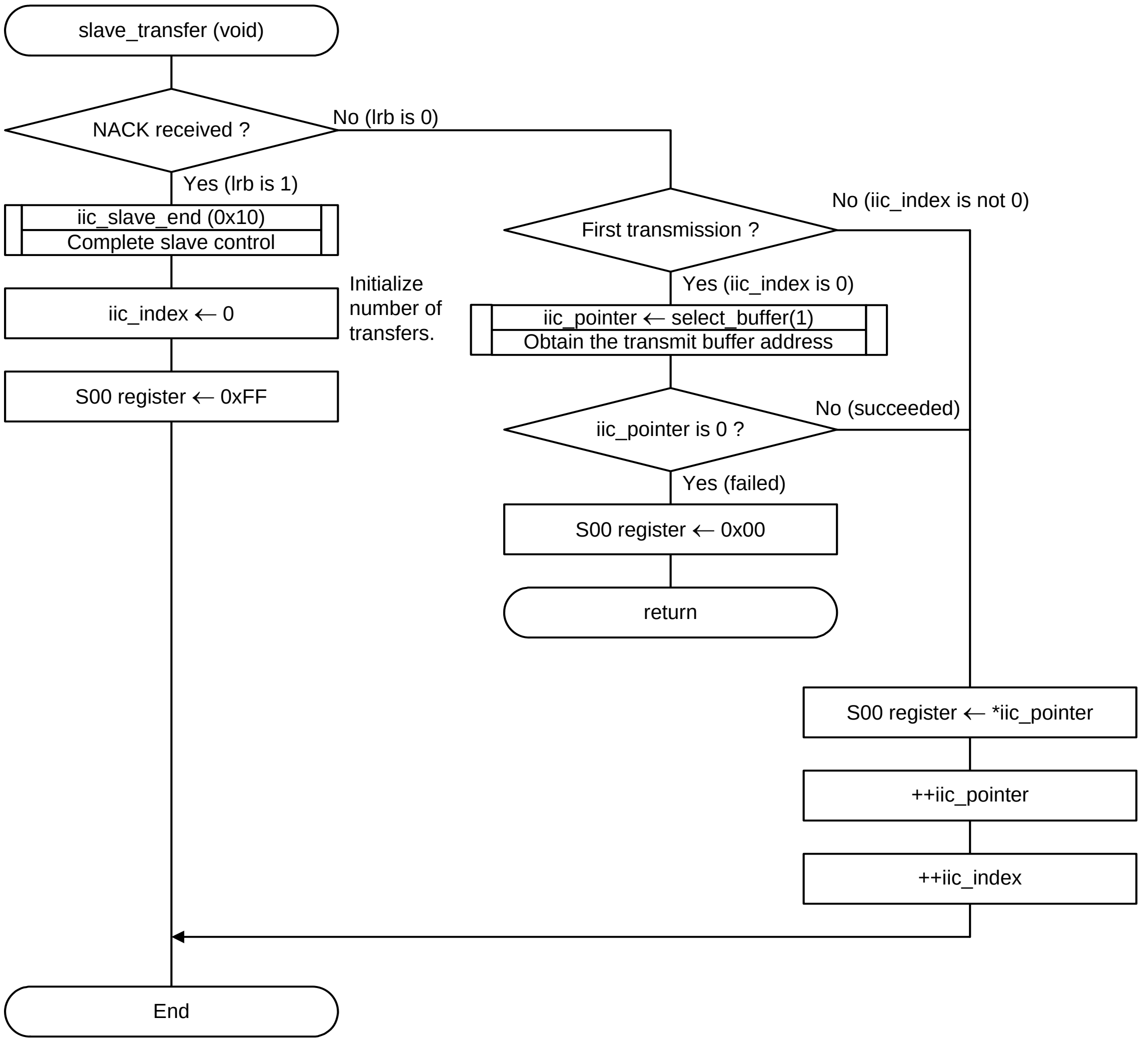
8.6.5 Master Receive Function



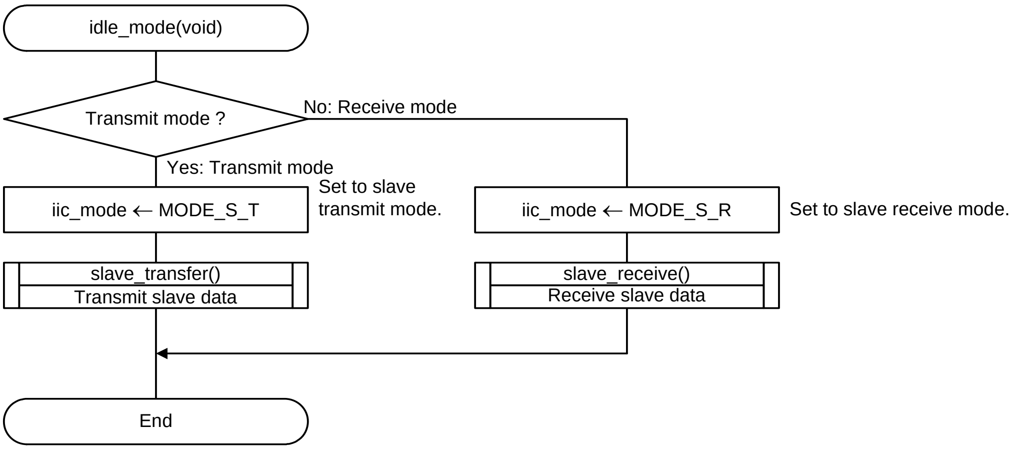
8.6.6 Slave Receive Function


slave_receive (void)
WIT bit is 1 ?
No (I²C-bus interrupt enabled at falling edge of ACK clock)
Yes (I²C-bus interrupt is enabled at 8th clock)
iic_length--
Data received ?
No
Yes
S20 register ACKBIT ← 1
NACK
S20 register ACKBIT ← 0
ACK
First transmission ?
No (index is not 0)
Yes (index is 0)
iic_pointer ← select_buffer(0)
Obtain the transmit and receive buffer addresses
*iic_pointer ← S00 register
++iic_pointer
No (obtained the receive buffer successfully)
iic_pointer is 0 ?
Yes
(failed to obtain the receive buffer)
return
++iic_index
S00 register ← 0xFF
End

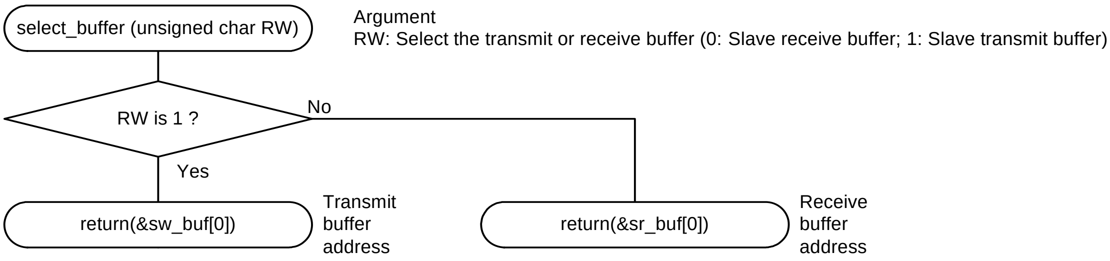
8.6.7 Slave Transmit Function



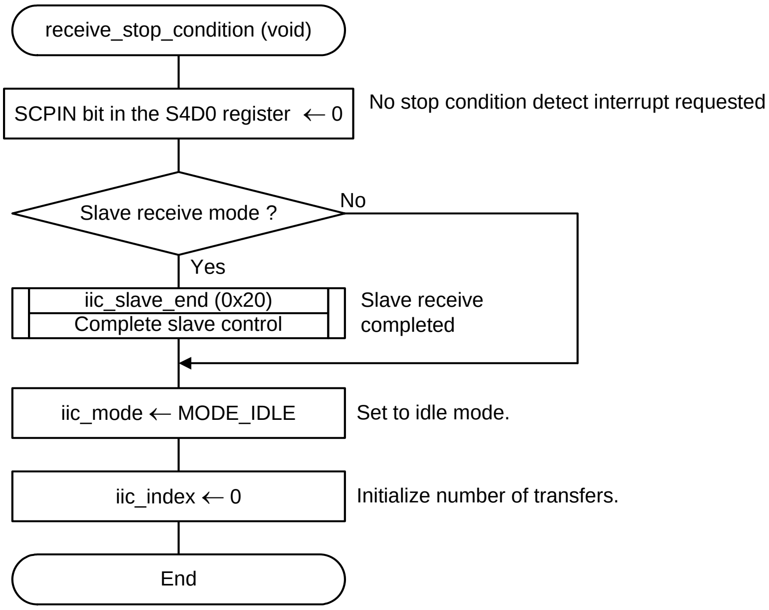
8.6.8 Transmit and Receive Mode Select Function



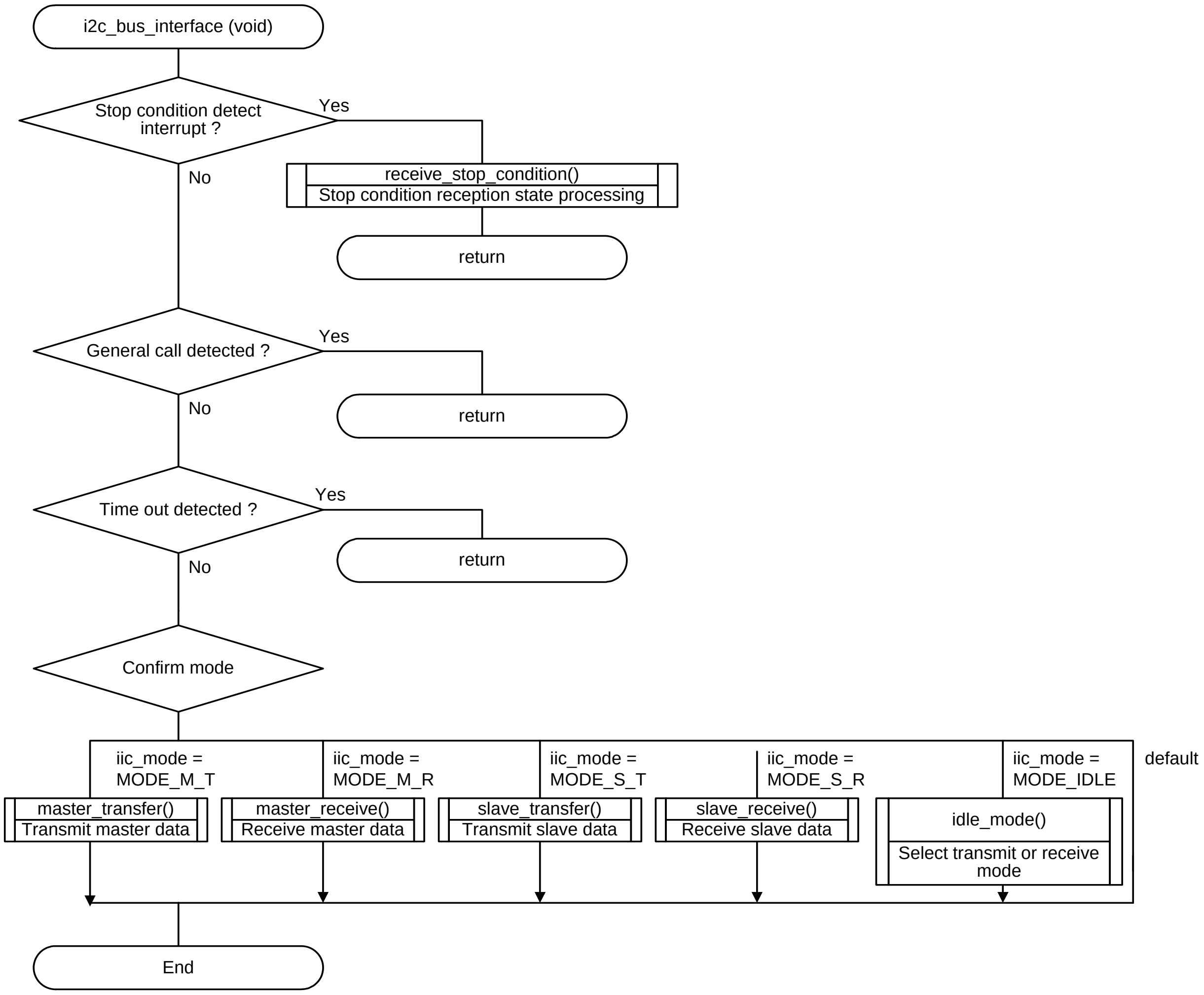
8.6.9 Function for Obtaining Transmit and Receive Buffer Addresses


select_buffer (unsigned char RW)
Argument
RW: Select the transmit or receive buffer (0: Slave receive buffer; 1: Slave transmit buffer)
RW is 1 ?
No
Yes
return(&sw_buf[0])
Transmit buffer address
return(&sr_buf[0])
Receive buffer address

8.6.10 Stop Condition Reception State Processing Function



8.6.11 I^{2}C-bus Interface Interrupt Handling



9. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the M16C Family page.

10. Reference Documents

Hardware Manuals
M16C/64A Group Hardware Manual
M16C/65 Group Hardware Manual
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	M16C/64A, M16C/65 Group Multi-Master I^{2}C-bus Interface

Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2009	–	First Edition issued
1.01	Dec 01, 2009	4	“4.1 Initial Settings” (3),(4) enabled → disabled

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