R32C/100 Series

Multi-channel PWM Output Using DMA Transfer

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1. Abstract

This document describes the setting procedure and operation example for multi-channel PWM output using DMA transfer.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

This application example describes how to output 16 PWM pulses from ports P0 to P2 using timer B0 and two channels of DMAC. Change the PWM output every time timer B0 (1) underflows.
Table 3.1 and Table 3.2 list the Clock Frequency Settings and DMAC Channel Settings, respectively.
Note:

1. Timer B0 setting: Timer mode, count source = f1 (25 MHz), cycle (change between 100 μs and 900 μs)

Table 3.1 Clock Frequency Settings

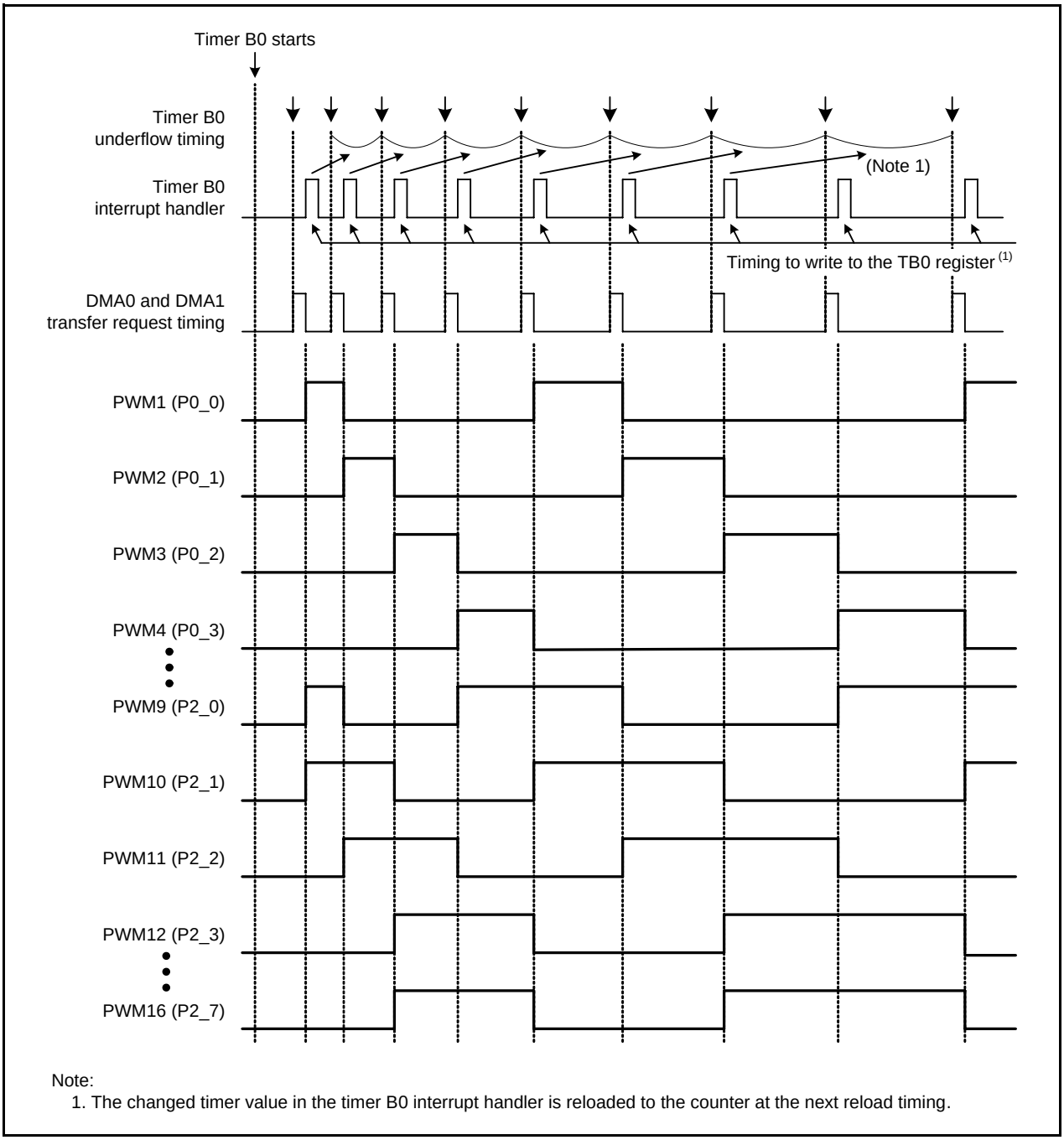
Clock	Frequency
Main clock	16 MHz
PLL clock	100 MHz
Base clock	50 MHz
CPU clock	50 MHz
Peripheral bus clock	25 MHz
Peripheral function clock source	25 MHz

Table 3.2 DMAC Channel Settings

Item	DMA0	DMA1
Transfer mode	Repeat transfer	
Transfer size	8 bits	
DMA request sources	Timer B0	
Update source address	Incrementing addressing	
Destination address	P0	P2
Update destination address	Non-incrementing addressing	
Number of transfers	4	
Transfer complete interrupt	Not used	

3.1 Operation

After setting ports P0 and P2 as output, timer B0 starts counting. Every time timer B0 underflows, a DMA transfer is generated, and a PWM pulse is output from ports P0 and P2.
Rewrite the TB0 register in the TB0 interrupt handler to change the PWM pulse output width.
Figure 3.1 shows the PWM Output Timing.



Note:
1. The changed timer value in the timer B0 interrupt handler is reloaded to the counter at the next reload timing.

Figure 3.1 PWM Output Timing

3.2 Notes

- DMA Transfer Priority
  When multiple DMA transfer requests are generated simultaneously, channel priority is as follows:
  DMA0 > DMA1 > DMA2 > DMA3

- Delay Time When Timer B0 Starts
  In the initial pulse output, the difference from when the ports are set and timer B0 starts is the delay time.

- Delay Time of Pulse Output
  The actual pulse output is delayed by the delay time of the number of DMA transfer cycles + DMA transfer delay cycles after a timer B0 interrupt request is generated.

3.3 Flowcharts

Figure 3.2 to Figure 3.5 show the Main Function, the DMAi Setting (i = 0, 1), the Timer B0 Setting Function, and the Timer B0 Interrupt Function, respectively.

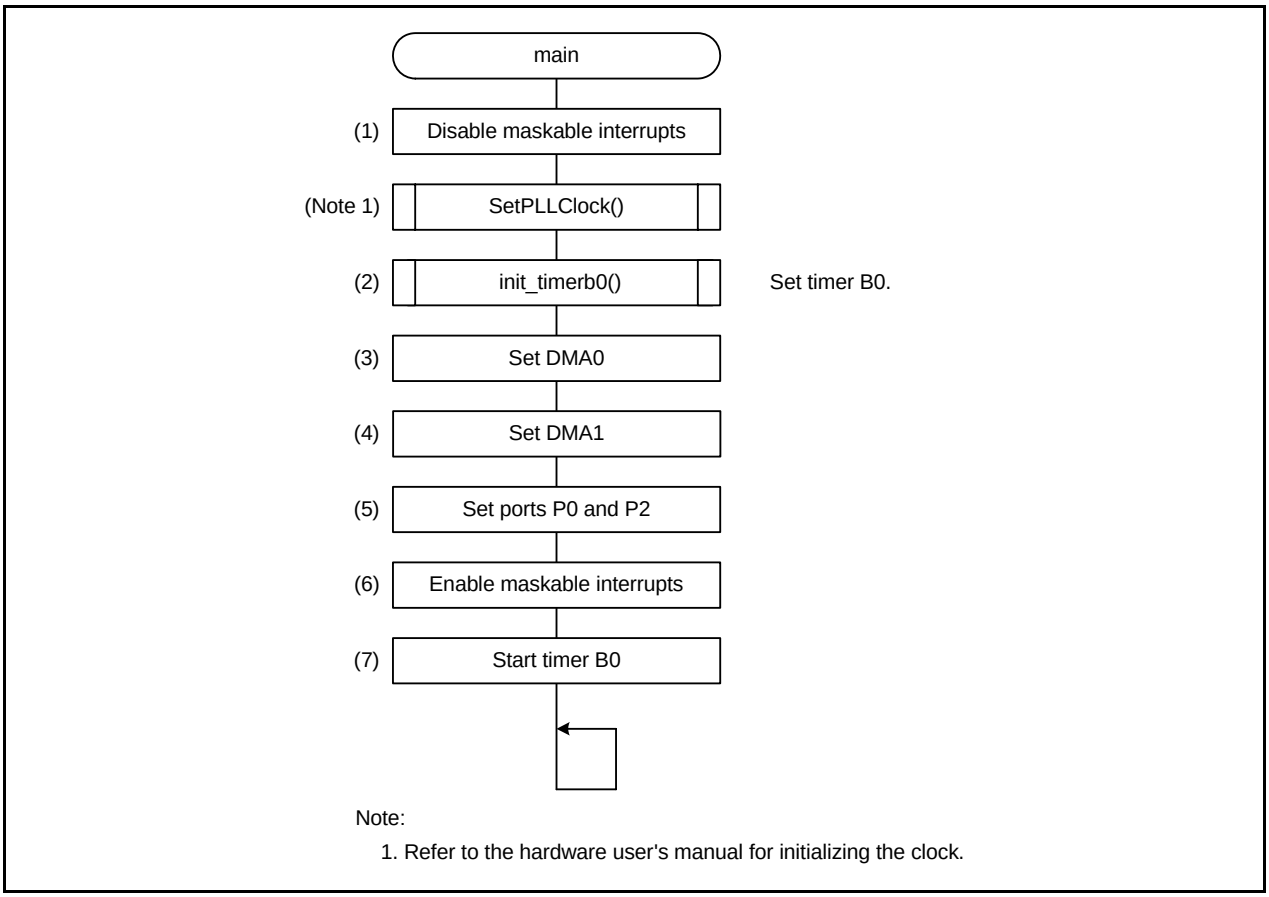
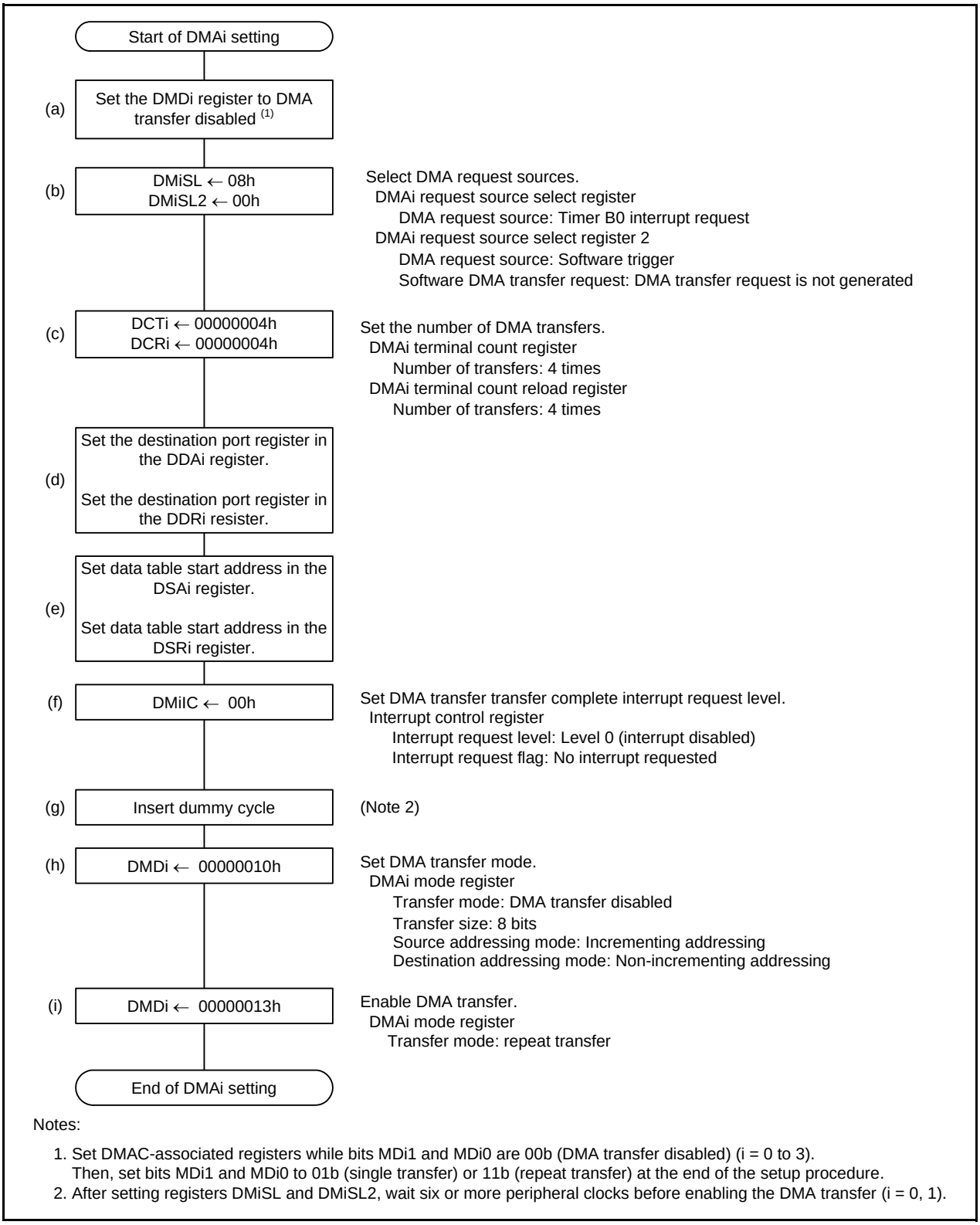


Figure 3.2 Main Function



Notes:

1. Set DMAC-associated registers while bits MDi1 and MDi0 are 00b (DMA transfer disabled) (i = 0 to 3). Then, set bits MDi1 and MDi0 to 01b (single transfer) or 11b (repeat transfer) at the end of the setup procedure.
2. After setting registers DMiSL and DMiSL2, wait six or more peripheral clocks before enabling the DMA transfer (i = 0, 1).

Figure 3.3 DMAi Setting (i = 0, 1)

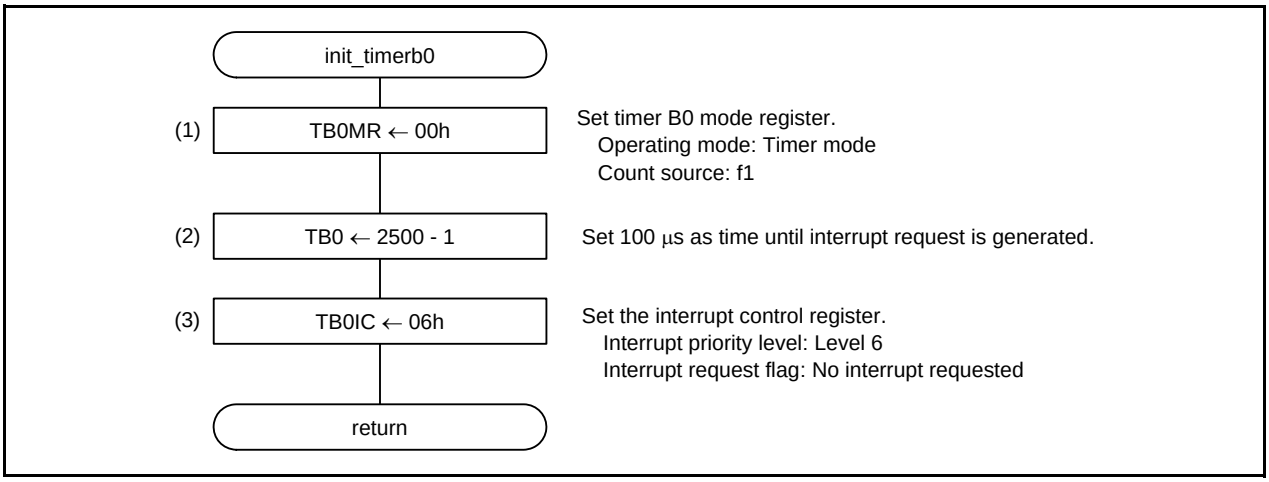
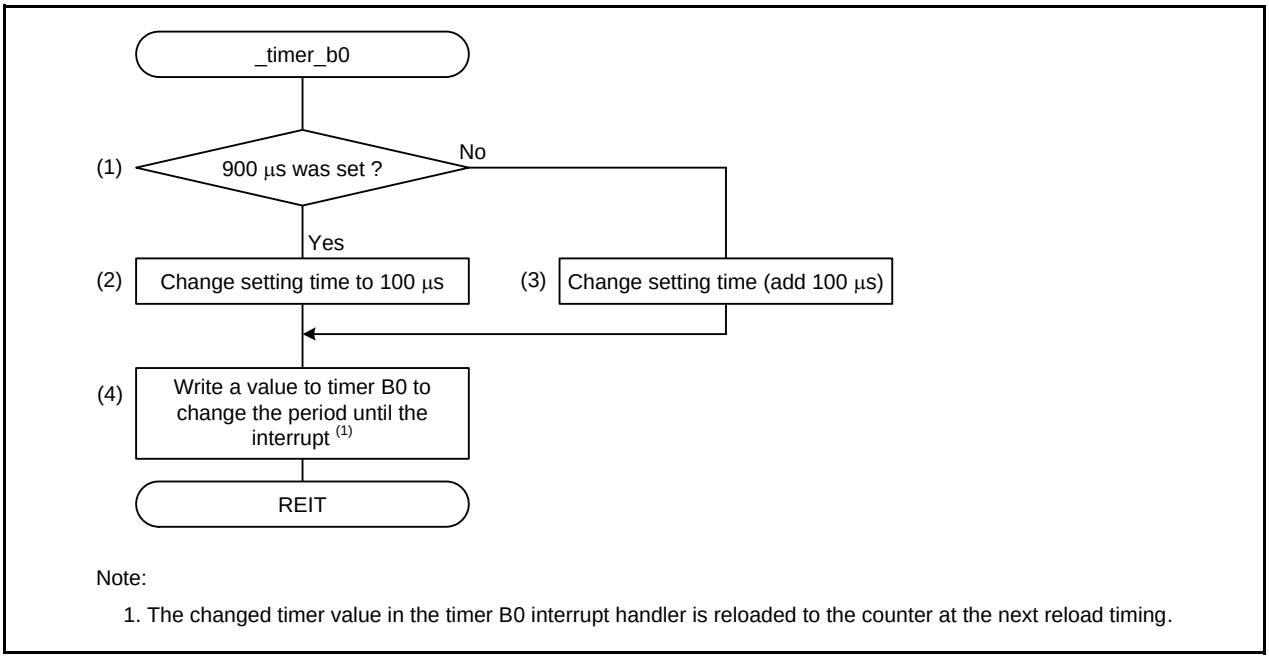


Figure 3.4 Timer B0 Setting Function



Note:

1. The changed timer value in the timer B0 interrupt handler is reloaded to the counter at the next reload timing.

Figure 3.5 Timer B0 Interrupt Function

4. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5. Reference Documents

User's Manuals
R32C/116 Group User's Manual: Hardware Rev.1.00
R32C/117 Group User's Manual: Hardware Rev.1.00
R32C/118 Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

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REVISION HISTORY	R32C/100 Series Multi-channel PWM Output Using DMA Transfer

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		Page	Summary
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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