RL78/L1C, RL78/L23

Migration Guide from RL78/L1C to RL78/L23

Introduction

This application note explains the functional differences between the RL78/L23 microcontroller and the RL78/L1C LCD microcontroller, as well as key considerations when replacing the RL78/L1C with the RL78/L23.

Please note that the RL78/L23 does not support USB functionality. Therefore, if you are using the USB function of the RL78/L1C, migration to the RL78/L23 cannot be performed.

Target Device

RL78/L1C, RL78/L23

For detailed information on peripheral functions and electrical characteristics, refer to the User's Manual: Hardware and Technical Updates.

Contents

1. Summary of Differences

The following provides an overview of the differences between the RL78/L1C and RL78/L23.

1.1 Functional Differences

Tables 1.1 to 1.3 show the functional differences between the RL78/L1C and RL78/L23. Due to modifications in certain functions of the RL78/L23, ROM code developed for the RL78/L1C is not compatible with the RL78/L23.

Important notes regarding the migration of each function are provided in Chapter 2.

Table 1.1 Functional summary differences (1/3)

Item	RL78/L1C	RL78/L23	Remarks
Power supply voltage	1.6 to 3.6V	1.6 to 5.5V	
Operating ambient temperature	-40 to 105℃	-40 to 105℃	
Package	80/85/100 pins	44/48/52/64/80/100 pins	
CPU core	S3 core	S3 core	
Operation clock	Max 24MHz TMKB is 48MHz	Max 32MHz TMKB is 64MHz	- Added MOCO (4MHz / 2MHz / 1MHz) - Changed low-speed OCO from 15kHz to 32.768kHz. Selectable as CPU clock source - Added frequency divider to high-speed system clock
Code flash	64 to 256KB (Block size: 1KB)	64 to 512KB (Block size: 2KB)	- Supported variable boot and dual-bank rewriting - Changed self-programming software to Renesas Flash Driver
Data flash	8KB (Block size: 1KB)	8KB (Block size: 256B)	- Changed self-programming software to Renesas Flash Driver
Port function	✓	Function enhanced	- Added output current control port - Added 40-mA output port
Flash operating mode	LV mode LS mode HS mode	LP mode LS mode HS mode	- Changed operating frequency and voltage range: LP mode: 1 to 2MHz, 1.6 to 5.5V LS mode: 1 to 24MHz, 1.8 to 5.5V HS mode: 1 to 32MHz, 1.8 to 5.5V
Switching the flash operating mode	-	Operation state control	- Operating mode changeable via software
Data transfer function	DTC 24ch	DTC 24ch	- Added DTC activation sources
Timer array unit	8ch	8ch	- Added input from ELCL - Changed f_{IL} input from ch1 to ch5
Realtime clock	1ch	1ch	- 500ms output added separately from INTRTC for LCD blinking
Interval timer	12bit 1ch	32bit 1ch +8bit 8 to 16ch	- Extended operation time and increased number of channels

Note : New peripheral functions, : Changed peripheral functions,
－ : There is no corresponding function

Table 1.2 Functional summary differences (2/3)

Item	RL78/L1C	RL78/L23	Remarks
16-bit timers KB20, KB21, KB22	3ch	3ch	- Added PWM output function for IH applications - Increased max frequency from 48 to 64MHz
Timer RJ	-	2ch	- New general-purpose timer added
External signal sampler	-	1unit	- Added function to generate sampling clock linked with 8-bit interval timer
Clock output/buzzer output controller	1ch	1ch	- Buzzer output using f_{IL} available
Watchdog timer (WDT)	1ch	1ch	- Overflow time change due to f_{IL} frequency update from 15 to 32.768kHz
A/D Converter	12bit 11 to 13ch	12bit 8 to 13ch	- Changed power supply from AVDD/AVSS to VDD/VSS - Scan mode removed - Added software trigger wait mode
D/A Converter	2ch	3ch	
Comparator	2ch	2ch	- Window mode removed - Added input path for D/A converter
Serial array unit	CSI: 4ch UART: 4ch Simplified I2C: 4ch	CSI: 5 to 8ch UART: 3 to 4ch Simplified I2C: 6 to 8ch	- Added UART loopback function
IICA(I2C)	1ch	2ch	- Added all address match function
UARTA	-	2~4ch	- Newly added UART operable with f_{SUB}
LCD controller	44 to 56segx4com 40 to 52segx8com	19 to 56segx4com 17 to 54segx6com 15 to 52segx8com	- Added VL2 reference (internal voltage boosting method) - Added VL4 reference method (capacitor split method) - 6com output supported - Blinking timing can be changed
Multiplier And Divider/ Multiply-Accumulate	CPU instruction	CPU instruction	
Event link controller (ELC)	✓	Function enhanced (Logic and event link controller)	- Signals output from peripheral functions can be routed to designated peripheral functions via the internal logic cell block, which allows signal modification.
Interrupt functions	External 9ch Internal 33 to 36ch	External 9ch Internal 47 to 52ch	- Changed interrupt sources due to functional differences - Increased the number of pins that also serve as INTP
Key interrupt function	8ch	2 to 8ch	
Standby function	✓	Function enhanced	- Added the ability to fast-start a high-speed on-chip oscillator - Added function to stop power supply to RAM
Reset function	✓	✓	- RTC and CMC registers are initialized only by POR reset

Note : New peripheral functions, : Changed peripheral functions,
－ : There is no corresponding function

Table 1.3 Functional summary differences (3/3)

Item	RL78/L1C	RL78/L23	Remarks
Voltage detector	1ch	2ch	- Removed interrupt & reset mode - Modified detection voltage - LVD1 settings configurable via register
Safety functions	✓	Function enhanced	- Added flash memory guard function - Added UART loopback function
Security functions encryption	Flash rewriting prohibit function, Flash shield window function	Function enhanced	- Added true random number generator, unique ID, and customer ID
SNOOZE mode sequencer	-	1unit	- Can operate in standby via sequencer independent from CPU
Capacitive sensing unit	-	16 to 36ch	- Capacitance measurement function of capacitance sensor
Regulator	1.8V and 2.1V	1.5V	- Changed REGC voltage
Option bytes	✓	Function enhanced	- WDT, LVD, and Flash operating mode functions, changeable boot/swap support
On-chip debugging	✓	✓	- Changed supported emulator - Added support for 2-wire OCD
BCD Correction Circuit	✓	✓	

Note : New peripheral functions, : Changed peripheral functions,
－ : There is no corresponding function

1.2 Pin function Differences

The RL78/L1C and RL78/L23 have different pin configurations.
Tables 1.4 to 1.7 show a comparison of the pin assignments between the RL78/L1C and RL78/L23 for the 80-pin and 100-pin packages. Refer to Tables 1.4 to 1.7 to verify the pin functions being used.

Table 1.4 Pin function Comparison of 80pin Products (1)

No	RL78/L1C	RL78/L23
1	P152/ANI2	P130/SEG28/TRJO1/(TxDA0)/(SO21)/(SO01)
2	P151/ANI1/AVREFM	P47/SEG27/(RxDA0)/(SI21)/(SDA21)/(SDA01)/(SI01)/(INTP1)
3	P150/ANI0/AVREFP	P46/SEG26/(SCK21)/(SCL21)/(SCL01)/(SCK01)
4	P130	P45/IVREF0/TxDA2/SCK30/SCL30/EXSDO0
5	P46/ANO1	P44/IVCMP0/RxDA2/SI30/SDA30/RxD3/EXSDO1/(TI04)/(TO04)/(INTP7) /(SCK11)/(SCL11)
6	P45/ANO0	P43/IVCMP1/SO30/TxD3/(TI05)/(TO05)/(INTP4)/(RxDA1)/(SI11)/(SDA11)
7	P44/IVREF0	P42/TI05/TO05/IVREF1/TRJO0/(INTP7)/(TxDA1)/(SCLA0)/(RxD0)/(TxD1)/ (SI00)/(SDA00)/(SO11)/(PCLBUZ1)
8	P43/(INTP7)/IVCMP0	P41/(TI07)/(TO07)/(INTP6)/(TxD0)/(SDAA0)/(SO00)/(RxD1)
9	P40/TOOL0/(TI00)/(TO00)	P40/TOOL0/(TI00)/(TO00)/(SCK00)/(SCL00)
10	RESET	RESET
11	P124/XT2/EXCLKS	P124/XT2/EXCLKS
12	P123/XT1	P123/XT1
13	P137/INTP0	P137/EI137/INTP0
14	P122/X2/EXCLK	P122/X2/EXCLK/EI122
15	P121/X1	P121/X1/VBAT0/EI121
16	REGC	REGC
17	VSS0	VSS
18	VDD0	VDD
19	P60/SCLA0/(TI01)/(TO01)	P60/SCLA0/CCD04/EO60/(TI01)/(TO01)/(INTP3)
20	P61/SDAA0/(TI02)/(TO02)	P61/SDAA0/CCD05/EO61/(TI02)/(TO02)/(INTP4)
21	P127/CAPH/(TI03)/(TO03)/(REMOOUT)	P62/SCLA1/CCD06/(TI03)/(TO03)/(REMOOUT)/(INTP5)
22	P126/CAPL/(TI04)/(TO04)	P63/SDAA1/CCD07/(TI04)/(TO04)/(INTP6)
23	VL1	P127/CAPH/TS00/(TI03)/(TO03)/(REMOOUT)
24	VL2	P126/CAPL/TS01/(TI04)/(TO04)/(INTP4)
25	VL4	P87/VL1/(TxD1)/(SO10)
26	P125/VL3/(TI06)/(TO06)	P86/VL2/(TI06)/(TO06)/(INTP3)/(RxD1)/(SI10)/(SDA10)/(PCLBUZ1)
27	P35/SO30/TxD3/SEG25	P85/VL4/(VCOUT0)/(INTP4)/(SCK10)/(SCL10)/(SCK30)/(SCL30)
28	P34/SI30/RxD3/SDA30/SEG24	P125/VL3/TS02/(TI06)/(TO06)/(VCOUT1)/(INTP7)/(RxD3)/(SI30)/(SDA30) /(PCLBUZ1)
29	P33/INTP4/SCK30/SCL30/SEG23	P35/SEG25/TS03/(VCOUT0)/(INTP4)/(SO30)/(TxD3)
30	P32/TI01/TO01/SEG22	P34/SEG24/TS04/(TI01)/(TO01)/(INTP0)/(RxD3)
31	P31/INTP3/RTC1HZ/SEG21	P31/INTP3/RTC1HZ/SEG21/TS07/(TI01)/(TO01)
32	P30/TI03/TO03/REMOOUT/SEG20	P30/TI03/TO03/SEG20/REMOOUT/TS08/(INTP3)/(RTC1HZ)
33	P77/KR0/TKBO01/SEG19	P77/KR7/SEG19/TS09/CCD00/TKBO01/SO20/TxD2/EI77/EO77/(TKBO21) /(TI07)/(TO07)/(INTP1)/(EXSDO0
34	P76/KR1/TKBO00/SEG18	P76/KR6/SEG18/TS10/CCD01/TKBO00/SI20/SDA20/RxD2/EI76/EO76/ (INTP2)/(RTC1HZ)/(EXSDO1)
35	P75/KR2/TKBO11/SEG17	P75/KR5/SEG17/TS11/CCD02/SCK20/SCL20/(TKBO11)/(TKBO01) /(TI03)/(TO03)/(REMOOUT)/(INTP0)
36	P74/KR3/TKBO10/SEG16	P74/KR4/SEG16/TS12/CCD03/TKBO11/(TKBO01)
37	P73/KR4/TKBO21/SEG15	P73/KR3/SEG15/TS13/TKBO10
38	P72/KR5/TKBO20/SEG14	P72/KR2/SEG14/TS14/TKBO21
39	P71/KR6/SEG13	P71/KR1/SEG13/TS15
40	P70/KR7/SEG12	P70/KR0/SEG12/TS16/TKBO20

Remarks: Locations where function pins have been deleted or moved are shown in red, and minor changes such as channel changes are shown in yellow.

Talbe1.5 Pin function Comparison of 80pin Products (2)

No	RL78/L1C	RL78/L23
41	P52/SEG6	P57/INTP6/SEG11/TSCAP/(TI03)/(TO03)/(REMOOUT)
42	P51/SEG5	P56/TI06/TO06/SEG10/TS17
43	P50/SEG4/INTP6	P55/INTP5/SEG9/TS18/(TI02)/(TO02)
44	COM7/SEG3	P54/TI02/TO02/SEG8/TS19/SCK01/SCL01/(INTP0)/(PCLBUZ0)
45	COM6/SEG2	P53/INTP2/SEG7/TS20/SI01/SDA01/(TI07)/(TO07)/(PCLBUZ0)
46	COM5/SEG1	P52/TI00/TO00/INTP1/SEG6/TS21/SO01/(PCLBUZ1)
47	COM4/SEG0	P51/SEG5/TS22/RxDA3/(INTP6)
48	COM3	P50/SEG4/TS23/TxDA3
49	COM2	P97/COM7/SEG3/TS24/(TI05)/(TO05)/(SCK01)/(SCL01)/(SCLA1)
50	COM1	P96/COM6/SEG2/TS25/(INTP5)/(SI01)/(SDA01)/(SDAA1)/(PCLBUZ0)
51	COM0	P95/COM5/SEG1/TS26/(TI02)/(TO02)/(INTP1)/(SO01)
52	P07/TI06/TO06/SEG55	P94/COM4/SEG0/TS27/(INTP2)/(SI01)/(SDA01)/(TI06)/(TO06)
53	P06/INTP5/SEG54	P93/COM3/TS28/(INTP3)/(SCK01)/(SCL01)
54	P05/TI02/TO02/SEG53	P92/COM2/TS29/(TI01)/(TO01)
55	P04/INTP2/SEG52	P91/COM1/TS30/(INTP2)
56	P03/TI00/TO00/INTP1/SEG51	P90/COM0/TS31/(TI00)/(TO00)/(INTP1)
57	P02/SO10/TxD1/(PCLBUZ0)/SEG50	P07/SO10/TxD1/SEG50/TS32/EI07/(PCLBUZ0)
58	P01/SI10/RxD1/SDA10/SEG49	P06/SI10/RxD1/SDA10/SEG49/TS33/EI06/(PCLBUZ1)
59	P00/SCK10/SCL10/SEG48	P05/SCK10/SCL10/SEG48/TS34/EO05
60	P12/TxD2/SO20/SEG42	P04/SEG47/VCOUT1/TS35/(INTP6)/(SO20)/(TxD2)/(PCLBUZ0)
61	P11/RxD2/SI20/SDA20/SEG41/VCOUT0	P03/SEG46/VCOUT0/TRJIO0/(RxD2)/(SI20)/(SDA20)/(SI31)/(SDA31)
62	P10/INTP7/PCLBUZ0/SCK20/SCL20/SEG40	P02/INTP7/PCLBUZ0/SEG45/(TKBO21)/(SCK20)/(SCL20) /(SCK31)/(SCL31)
63	P27/TI05/TO05/(INTP5)/PCLBUZ1/SEG39	P01/PCLBUZ1/SEG44/(TI05)/(TO05)/(TKBO11)/(INTP5)/(SO31)
64	P26/SO00/TxD0/TOOLTxD/SEG38	P00/SEG43/SO00/TxD0/TOOLTxD/EI00/EO00/EXSDI0/(TKBO01)/(TRJO0)
65	P25/SI00/RxD0/TOOLRxD/SDA00/SEG37	P17/SEG42/SI00/RxD0/TOOLRxD/SDA00/EI17/EO17/EXSDI1/(TKBO01) /(TRJIO0)
66	P24/SCK00/SCL00/SEG36	P16/SEG41/SCK00/SCL00/EI16/(VCOUT0)/(TKBO01)/(RTC1HZ)
67	P23/TI07/TO07/SEG35	P15/TI07/TO07/SEG40
68	P22/TI04/TO04/SEG34	P14/TI04/TO04/SEG39/ANI26
69	P21/ANI21/SEG33	P13/ANI25/SEG38
70	P20/ANI20/SEG32	P12/ANI24/SEG37/EI12/CLKA0/SO11/(VCOUT1)/(TKBO00)/(TRJO1) /(PCLBUZ1)
71	P143/ANI19/SEG31	P11/ANI23/SEG36/RxDA0/SI11/SDA11/(TKBO11)/(TRJIO1)/(INTP1)
72	P142/ANI18/SEG30	P10/ANI22/SEG35/TxDA0/SCK11/SCL11/(TKBO10)/(INTP0)
73	P141/ANI17/SEG29	P27/ANI21/SEG34/ANO1/EI27/RxDA1/SO21/(TKBO21)/(INTP4)/(TxD0) /(SO00)/(EXSDI1)
74	P140/ANI16/SEG28	P26/ANI20/SEG33/ANO0/EI26/TxDA1/SI21/SDA21/(TKBO20)/(INTP5) /(RxD0)/(SI00)/(SDA00)/(EXSDI0)
75	P82	P25/ANI19/SEG32/CLKA1
76	P83	P24/ANI18/SEG31
77	P156/ANI6	P23/ANI17/SEG30/TRJIO1
78	P155/ANI5	P22/ANI16/SEG29/SCK21/SCL21/(SCK00)/(SCL00)/(INTP7)
79	AVDD	P21/ANI0/AVREFP/VBAT1/EI21/(TO00)/(INTP6)/(PCLBUZ0)
80	AVSS	P20/ANI1/AVREFM/EI20/(TI00)/(INTP7)/(PCLBUZ1)

Remarks: Locations where function pins have been deleted or moved are shown in red, and minor changes such as channel changes are shown in yellow.

Talbe1.6 Pin function Comparison of 100pin Products (1)

No	RL78/L1C	RL78/L23
1	P153/ANI3	P140/SCK31/SCL31
2	P152/ANI2	P130/SEG28/TRJO1/(TxDA0)/(SO21)/(SO01)
3	P151/ANI1/AVREFM	P47/SEG27/SO31/(RxDA0)/(SI21)/(SDA21)/(SDA01)/(SI01)/(INTP1)
4	P150/ANI0/AVREFP	P46/SEG26/SI31/SDA31/(SCK21)/(SCL21)/(SCL01)/(SCK01)
5	P130	P45/IVREF0/TxDA2/SCK30/SCL30/EXSDO0
6	P46/ANO1	P44/IVCMP0/RxDA2/SI30/SDA30/RxD3/EXSDO1/(TI04)/(TO04)/(INTP7)
7	P45/ANO0	P43/IVCMP1/SO30/TxD3/(TI05)/(TO05)/(INTP4)/(RxDA1)/(SI11)/(SDA11)
8	P44/(SCK10)/(SCL10)/IVREF0	P42/TI05/TO05/IVREF1/TRJO0/(INTP7)/(TxDA1)/(SCLA0)/(RxD0)/(TxD1) /(SI00)/(SDA00)/(SO10)/(SO11)/(PCLBUZ1)
9	P43/(INTP7)/(SI10)/(RxD1)/(SDA10) /IVCMP0	P41/(TI07)/(TO07)/(INTP6)/(TxD0)/(RxDA3)/(SDAA0)/(SO00)/(SI10) /(SDA10)/(RxD1)
10	P42/TI05/TO05/(SO10)/(TxD1)/IVCMP1	P66/(TI05)/(TO05)/(INTP1)/(SCK10)/(SCL10)/(TxDA3)
11	P41/(TI07)/(TO07)/IVREF1	P67/(INTP2)/(TI01)/(TO01)
12	P40/TOOL0/(TI00)/(TO00)	P40/TOOL0/(TI00)/(TO00)/(SCK00)/(SCL00)
13	RESET	RESET
14	P124/XT2/EXCLKS	P124/XT2/EXCLKS
15	P123/XT1	P123/XT1
16	P137/INTP0	P137/INTP0/EI137
17	P122/X2/EXCLK	P122/X2/EXCLK/EI122
18	P121/X1	P121/X1/VBAT0/EI121
19	REGC	REGC
20	VSS0	VSS
21	VDD0	VDD
22	P60/SCLA0/(TI01)/(TO01)	P60/SCLA0/CCD04/EO60/(TI01)/(TO01)/(INTP3)
23	P61/SDAA0/(TI02)/(TO02)	P61/SDAA0/CCD05/EO61/(TI02)/(TO02)/(INTP4)
24	P127/CAPH/(TI03)/(TO03)/(REMOOUT)	P64/(INTP5)/(SDAA1)/(TI03)/(TO03)/(REMOOUT)
25	P126/CAPL/(TI04)/(TO04)	P65/(INTP0)/(SCLA1)/(TI05)/(TO05)
26	VL1	P62/SCLA1/CCD06/(TI03)/(TO03)/(REMOOUT)/(INTP5)
27	VL2	P63/SDAA1/CCD07/(TI04)/(TO04)/(INTP6)
28	VL4	P127/CAPH/TS00/(TI03)/(TO03)/(REMOOUT)
29	P125/VL3/(TI06)/(TO06)	P126/CAPL/TS01/(TI04)/(TO04)/(INTP4)
30	P37/SEG27	P87/VL1/(TxD1)/(SO10)
31	P36/SEG26	P86/VL2/(TI06)/(TO06)/(INTP3)/(RxD1)/(SI10)/(SDA10)/(PCLBUZ1)
32	P35/SO30/TxD3/SEG25	P85/VL4/(VCOUT0)/(INTP4)/(SCK10)/(SCL10)/(SCK30)/(SCL30)
33	P34/SI30/RxD3/SDA30/SEG24	P125/VL3/TS02/(TI06)/(TO06)/(VCOUT1)/(INTP7)/(RxD3)/(SI30)/(SDA30)
34	P33/INTP4/SCK30/SCL30/SEG23	P35/SEG25/TS03/(VCOUT0)/(INTP4)/(SO30)/(TxD3)
35	P32/TI01/TO01/SEG22	P34/SEG24/TS04/(TI01)/(TO01)/(INTP0)/(SI30)/(RxD3)/(SDA30)
36	P31/INTP3/RTC1HZ/SEG21	P33/INTP4/SEG23/TS05/(TI01)/(TO01)/(RTC1HZ)/(SCK30)/(SCL30)
37	P30/TI03/TO03/REMOOUT/SEG20	P32/TI01/TO01/SEG22/TS06/(TI03)/(TO03)/(REMOOUT)/(INTP3)
38	P77/KR0/TKBO01/SEG19	EVSS
39	P76/KR1/TKBO00/SEG18	P31/INTP3/RTC1HZ/SEG21/TS07/(TI01)/(TO01)
40	P75/KR2/TKBO11/SEG17	P30/TI03/TO03/SEG20/REMOOUT/TS08/(INTP3)/(RTC1HZ)
41	P74/KR3/TKBO10/SEG16	P77/KR7/SEG19/TS09/CCD00/TKBO01/SO20/TxD2/EI77/EO77/(TKBO21) /(TI07)/(TO07)/(INTP1)/(EXSDO0)
42	P73/KR4/TKBO21/SEG15	P76/KR6/SEG18/TS10/CCD01/TKBO00/SI20/SDA20/RxD2/EI76/EO76 /(INTP2)/(RTC1HZ)/(EXSDO1)
43	P72/KR5/TKBO20/SEG14	P75/KR5/SEG17/TS11/CCD02/SCK20/SCL20/(TKBO11)/(TKBO01)/(TI03) /(TO03)/(REMOOUT)/(INTP0)
44	P71/KR6/SEG13	P74/KR4/SEG16/TS12/CCD03/TKBO11/(TKBO01)
45	P70/KR7/SEG12	P73/KR3/SEG15/TS13/TKBO10
46	P57/SEG11	P72/KR2/SEG14/TS14/TKBO21
47	P56/SEG10	P71/KR1/SEG13/TS15
48	P55/SEG9	P70/KR0/SEG12/TS16/TKBO20
49	P54/SEG8	P84/(INTP0)/(TxDA0)/(SCLA1)
50	P53/SEG7	P83/(INTP1)/(RxDA0)/(SDAA1)

Remarks: Locations where function pins have been deleted or moved are shown in red, and minor changes such as channel changes are shown in yellow.

Talbe1.7 Pin function Comparison of 100pin Products (2)

No	RL78/L1C	RL78/L23
51	P52/SEG6	P57/INTP6/SEG11/TSCAP/(TI03)/(TO03)/(REMOOUT)
52	P51/SEG5	P56/TI06/TO06/SEG10/TS17
53	P50/SEG4/INTP6	P55/INTP5/SEG9/TS18/(TI02)/(TO02)
54	COM7/SEG3	P54/TI02/TO02/SEG8/TS19/SCK01/SCL01/(INTP0)/(PCLBUZ0)
55	COM6/SEG2	P53/INTP2/SEG7/TS20/SI01/SDA01/(TI07)/(TO07)/(PCLBUZ0)
56	COM5/SEG1	P52/TI00/TO00/INTP1/SEG6/TS21/SO01/(PCLBUZ1)
57	COM4/SEG0	P51/SEG5/TS22/RxDA3/(INTP6)
58	COM3	P50/SEG4/TS23/TxDA3
59	COM2	P97/COM7/SEG3/TS24/(TI05)/(TO05)/(SCK01)/(SCL01)/(SCLA1)
60	COM1	P96/COM6/SEG2/TS25/(INTP5)/(SI01)/(SDA01)/(SDAA1)/(PCLBUZ0)
61	COM0	P95/COM5/SEG1/TS26/(TI02)/(TO02)/(INTP1)/(SO01)
62	P07/TI06/TO06/SEG55	P94/COM4/SEG0/TS27/(INTP2)/(SI01)/(SDA01)/(TI06)/(TO06)
63	P06/INTP5/SEG54	P93/COM3/TS28/(INTP3)/(SCK01)/(SCL01)
64	P05/TI02/TO02/SEG53	P92/COM2/TS29/(TI01)/(TO01)
65	P04/INTP2/SEG52	P91/COM1/TS30/(INTP2)
66	P03/TI00/TO00/INTP1/SEG51	P90/COM0/TS31/(TI00)/(TO00)/(INTP1)
67	P02/SO10/TxD1/(PCLBUZ0)/SEG50	P82/(SCK10)/(SCL10)/(PCLBUZ0)
68	P01/SI10/RxD1/SDA10/SEG49	P81/(RxD1)/(SI10)/(SDA10)
69	P00/SCK10/SCL10/SEG48	P07/SO10/TxD1/SEG50/TS32/EI07/(PCLBUZ0)
70	P17/SEG47	P06/SI10/RxD1/SDA10/SEG49/TS33/EI06/(PCLBUZ1)
71	P16/SEG46	P05/SCK10/SCL10/SEG48/TS34/EO05
72	P15/SEG45	P04/SEG47/VCOUT1/TS35/(INTP6)/(SO20)/(TxD2)/(PCLBUZ0)
73	P14/SEG44	P80/(INTP2)/(SCK20)/(SCL20)
74	P13/SEG43	P147/(INTP2)/(TxDA3)/(RxD2)/(SI20)/(SDA20)
75	P12/TxD2/SO20/SEG42/VCOUT1	P146/(VCOUT1)/(TxD2)/(SO20)/(SO31)/(RxDA2)/(INTP7)
76	P11/RxD2/SI20/SDA20/SEG41/VCOUT0	P03/SEG46/VCOUT0/TRJIO0/(TxDA2)/(RxD2)/(SI20)/(SDA20)/(SI31) /(SDA31)
77	P10/INTP7/PCLBUZ0/SCK20/SCL20/SEG40	P02/INTP7/PCLBUZ0/SEG45/(TKBO21)/(SCK20)/(SCL20)/(SCK31) /(SCL31)
78	P27/(TI05)/(TO05)/(INTP5)/PCLBUZ1/SEG39	P01/PCLBUZ1/SEG44/(TI05)/(TO05)/(TKBO11)/(INTP5)/(SO31)
79	P26/SO00/TxD0/TOOLTxD/SEG38	P00/SEG43/SO00/TxD0/TOOLTxD/EI00/EO00/EXSDI0/(TKBO01)/(TRJO0)
80	P25/SI00/RxD0/TOOLRxD/SDA00/SEG37	P17/SEG42/SI00/RxD0/TOOLRxD/SDA00/EI17/EO17/EXSDI1/(TKBO01) /(TRJIO0)
81	P24/SCK00/SCL00/SEG36	P16/SEG41/SCK00/SCL00/EI16/(VCOUT0)/(TKBO01)/(RTC1HZ)
82	P23/TI07/TO07/SEG35	P15/TI07/TO07/SEG40
83	P22/TI04/TO04/SEG34	P14/TI04/TO04/SEG39/ANI26
84	P21/ANI21/SEG33	P13/ANI25/SEG38
85	P20/ANI20/SEG32	P12/ANI24/SEG37/EI12/CLKA0/SO11/(VCOUT1)/(TKBO00)/(TRJO1) /(PCLBUZ1)
86	P143/ANI19/SEG31	P11/ANI23/SEG36/RxDA0/SI11/SDA11/(TKBO11)/(TRJIO1)/(INTP1)
87	P142/ANI18/SEG30	P10/ANI22/SEG35/TxDA0/SCK11/SCL11/(TKBO10)/(INTP0)
88	P141/ANI17/SEG29	P145/SEG55/(INTP3)/(TxDA1)/(SDAA0)
89	P140/ANI16/SEG28	P144/SEG54/(INTP4)/(RxDA1)/(SCLA0)
90	VDD1	P27/ANI21/SEG34/ANO1/EI27/RxDA1/SO21/(TKBO21)/(INTP4)/(TxD0) /(SO00)/(EXSDI1)
91	VSS1	P26/ANI20/SEG33/ANO0/EI26/TxDA1/SI21/SDA21/(TKBO20)/(INTP5) /(RxD0)/(SI00)/(SDA00)/(EXSDI0)
92	P80	P25/ANI19/SEG32/CLKA1
93	P81	P24/ANI18/SEG31
94	P82	P143/SEG53/(INTP5)/(TxDA2)
95	P83	P142/SEG52/(INTP7)/(RxDA2)
96	P156/ANI6	P141/SEG51/(INTP6)/(RxDA3)
97	P155/ANI5	P23/ANI17/SEG30/TRJIO1
98	AVDD	P22/ANI16/SEG29/SCK21/SCL21/(SCK00)/(SCL00)/(INTP7)
99	AVSS	P21/ANI0/AVREFP/VBAT1/EI21/(TO00)/(INTP6)/(PCLBUZ0)
100	P154/ANI4	P20/ANI1/AVREFM/EI20/(TI00)/(INTP7)/(PCLBUZ1)

Remarks: Locations where function pins have been deleted or moved are shown in red, and minor changes such as channel changes are shown in yellow.

2. Migration Notes

This chapter describes important considerations when developing programs using functions that have been changed from the RL78/L1C. For peripheral function settings, it is recommended to use the code newly generated with the Smart Configurator (SC)Note. For information on new functions of the RL78/L23, please refer to the RL78/L23 User's Manual: Hardware.

Note: The Code Generator (CG), which is used as a development tool for the RL78/L1C, is not supported.

2.1 Port Functions

In the RL78/L23, the register used to switch between analog input and digital I/O functions has changed. Use the PMCAxx register.

In addition, new registers have been introduced for functions newly added to the RL78/L23. The default settings of these registers select digital I/O.

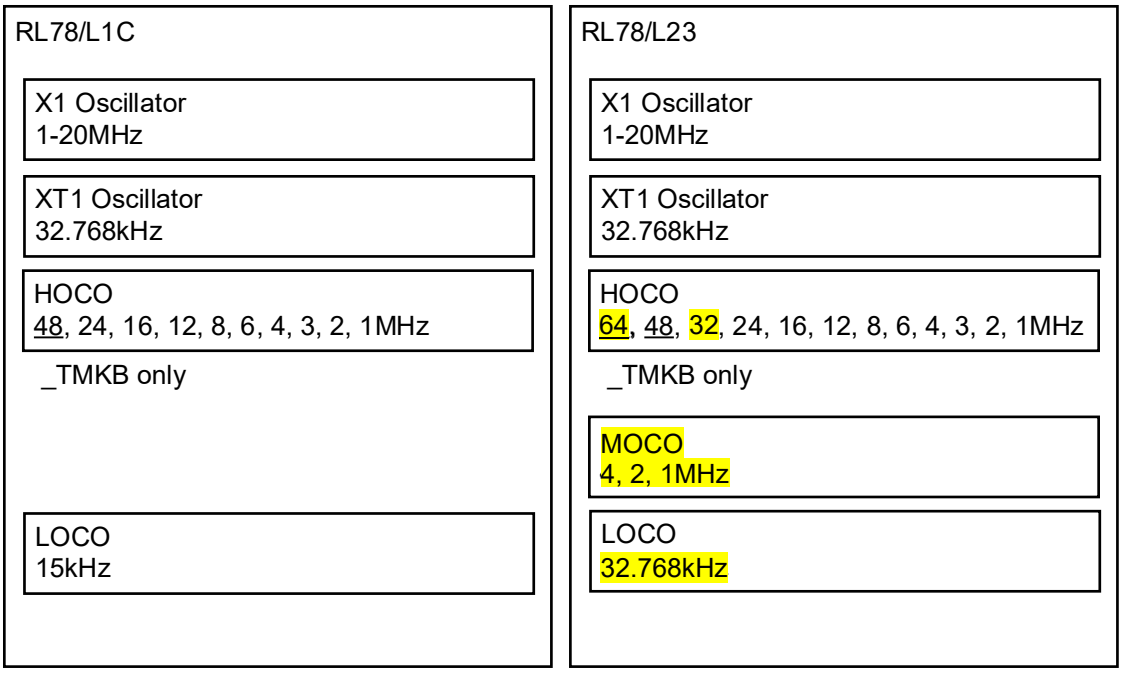
2.2 Clock Generator Circuit

Figure 2.1 shows the differences in the clock generation circuit. In the RL78/L23, the Low-Speed On-Chip Oscillator (LOCO) has been changed from 15 kHz to 32.768 kHz. It is also possible to select LOCO as the CPU clock source.

The maximum frequency of the High-Speed On-Chip Oscillator (HOCO) has been increased from 48 MHz to 64MHz. TMKB can be supplied with 64 MHz, and the CPU clock with 32MHz.

The high-speed system clock can be divided for use.

Figure 2.1 Clock Generation Circuit Differences



Remarks : Additional changes

In the RL78/L1C, the PERx register controlled both clock supply and reset for peripheral functions.

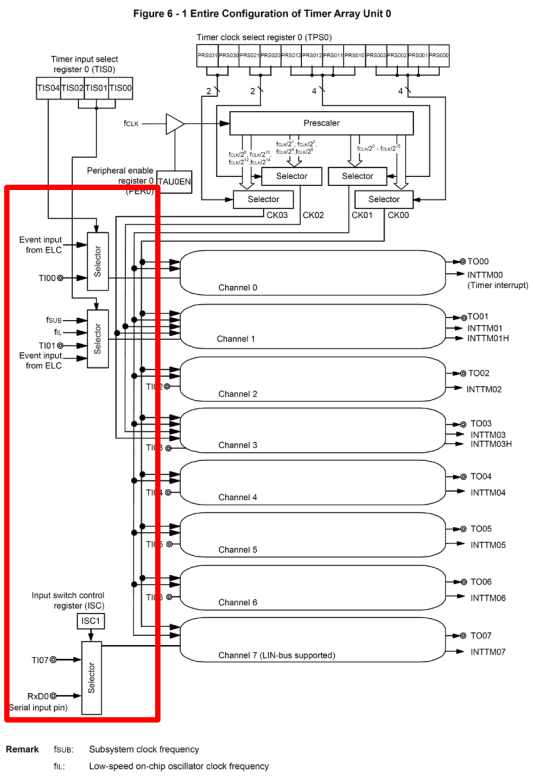
In contrast, in the RL78/L23, the PERx register is used only for clock supply control, while peripheral function resets are handled by the newly added PRRx register.

2.3 Timer Array Unit

Figure 2.2 shows the differences in the Timer Array Unit.
The basic functions are the same. In the RL78/L23, the input specification for channel 5 has been expanded, and the input specification for channel 1 has been modified.

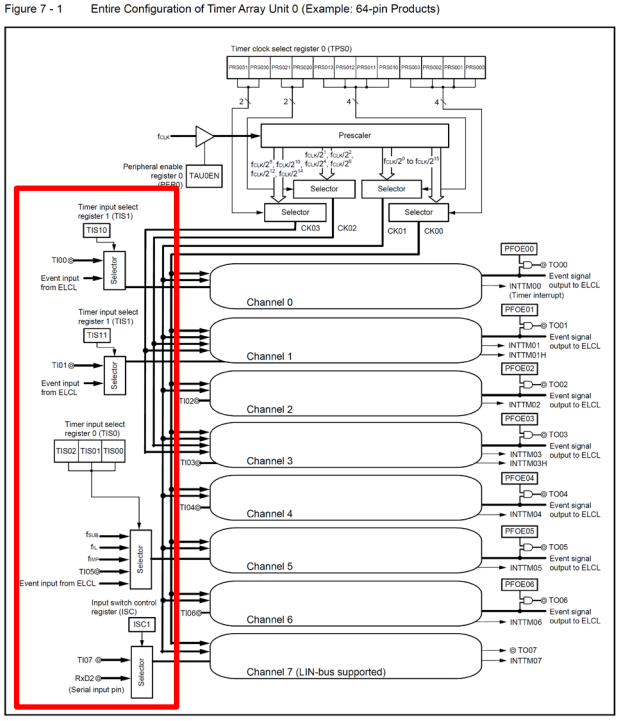
Figure 2.2 Timer Array Unit Difference

RL78/L1C



Remark fSUB: Subsystem clock frequency
fIL: Low-speed on-chip oscillator clock frequency

RL78/L23



Remark fSUB: Subsystem clock frequency
fIL: Low-speed on-chip oscillator clock frequency
fIMP: Middle-speed on-chip oscillator peripheral clock frequency

2.4 16-bit Timers KB20

For power and lighting control, the basic functions are the same as those of the RL78/L1C. The RL78/L23, in addition to supporting power and lighting control, can generate PWM output suitable for IH cooker control.

2.5 Realtime Clock

The basic functions are the same.

The RL78/L23 allows the 128 Hz clock generated from f_{RTC} to be selected as the operating clock. A 500ms signal generation function for LCD blinking display has also been added.

2.6 12-bit Interval Timer

The RL78/L23 includes 8-bit and 32-bit interval timers as alternatives to the 12-bit interval timer. The 8-bit and 32-bit interval timers can use the subsystem clock (32.768 kHz) as their operating clock.

2.7 Clock Output/Buzzer Output Controller

The basic functions are the same.

In the RL78/L23, LOCO can be selected as the clock source for the buzzer output.

2.8 Watchdog Timer

The basic functions are the same.

In the RL78/L23, the count clock has been changed from 15 kHz (Typ.) to 32.768 kHz (Typ.), which also results in changes to the overflow time and window open time specifications.

Table 2.1 Overflow Time Comparison

WDCS2-0 setting	Overflow time	
	RL78/L1C (f_{IL}=17.25 kHz (Max case))	RL78/L23 (f_{IL} =37.683kHz (Max case))
000	2^6/f_{IL} (3.71 ms)	2^7/f_{IL} (3.39 ms)
001	2^7/f_{IL} (7.42 ms)	2^8/f_{IL} (6.79 ms)
010	2^8/f_{IL} (14.84 ms)	2^9/f_{IL} (13.58 ms)
011	2^9/f_{IL} (29.68 ms)	2^10/f_{IL} (27.17 ms)
100	2^11/f_{IL} (118.72 ms)	2^12/f_{IL} (108.69 ms)
101	2^13/f_{IL} (474.89 ms)	2^14/f_{IL} (434.78 ms)
110	2^14/f_{IL} (949.79 ms)	2^15/f_{IL} (869.56 ms)
111	2^16/f_{IL} (3799.18 ms)	2^17/f_{IL} (3478.26 ms)

2.9 A/D Converter

The A/D converter of the RL78/L23 has the same 12-bit resolution as that of the RL78/L1C.

In the RL78/L23, the A/D converter power supply has been changed from AVDD/AVSS to VDD/VSS. Additionally, new hardware triggers have been added, including the A/D trigger signal from the 16-bit Timer KB4x and event input from the ELCL.

2.10 D/A Converter

The basic functions are the same.

2.11 Comparator

In the RL78/L23, the window mode has been removed.

Equivalent functionality can be achieved by using two comparator channels. Refer to the application note “RL78/G23 Setting the Window Comparator” for details.

The output of the D/A converter has also been added to the input path.

2.12 Serial Array Unit

There are no changes to the specifications of the RL78/L1C.

In the RL78/L23, a loopback function has been added for UART communication. Additional features, such as accepting output signals from the ELCL, have also been added.

2.13 Serial Interface IICA

There are no changes to the specifications of the RL78/L1C.

2.14 LCD Controller/Driver

In the RL78/L23, the VL2 reference method has been added for the internal voltage boost method, and the VL4 reference method has been added for the capacitor split method. Additionally, 6-time-division output is now supported. As a result, some register specifications have been changed. A new blinking display timing option of 0.5 seconds and a configurable ELCITL2 period have been added for LCD blinking control.

Furthermore, the relationship between port numbers and SEG output numbers has changed between the RL78/L1C and RL78/L23. The COM0-COM3 output pins are now shared with general-purpose ports. Please refer to Tables 2.2 and 2.3 for details.

Table 2.2 LCD display function ports (80 pins products)

Item	RL78/L1C								RL78/L23							
LCD Controllers / Driver	Segment signal outputs : 44 (40)Note Common signal outputs : 8								Segment signal outputs : 49 (45) Note Common signal outputs : 8							
Multiplexed I/O port	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	SEG 55	SEG 54	SEG 53	SEG 52	SEG 51	SEG 50	SEG 49	SEG 48	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43
P1						SEG 42	SEG 41	SEG 40	SEG 42	SEG 41	SEG 40	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35
P2	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29	–	–
P3	–	–	SEG 25	SEG 24	SEG 23	SEG 22	SEG 21	SEG 20	–	–	SEG 25	SEG 24	–	–	SEG 21	SEG 20
P4	–	–	–	–	–	–	–	–	SEG 27	SEG 26	–	–	–	–	–	–
P5	–	–	–	–	–	SEG 6	SEG 5	SEG 4	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4
P7	SEG 19	SEG 18	SEG 17	SEG 16	SEG 15	SEG 14	SEG 13	SEG 12	SEG 19	SEG 18	SEG 17	SEG 16	SEG 15	SEG 14	SEG 13	SEG 12
P9	–	–	–	–	–	–	–	–	SEG3/ COM7	SEG2/ COM6	SEG1/ COM5	SEG0/ COM4	COM3	COM2	COM1	COM0
P13	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 28
P14	–	–	–	–	SEG 31	SEG 30	SEG 29	SEG 28	–	–	–	–	–	–	–	–
Not multiplexed with I/O port																
COM0	–								–							
COM1	–								–							
COM2	–								–							
COM3	–								–							
COM4	SEG0								–							
COM5	SEG1								–							
COM6	SEG2								–							
COM7	SEG3								–							

Note : ( ) indicates the number of signal output pins when 8 com is used.
Remarks: ☐ :Change, ☐ : Delete, – : No corresponding register

Table 2.3 LCD display function ports (100 pins products)

Item	RL78/L1C								RL78/L23							
LCD Controllers / Driver	Segment signal outputs : 56 (52)Note Common signal outputs : 8								Segment signal outputs : 49 (45) Note Common signal outputs : 8							
Multiplexed I/O port	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	SEG 55	SEG 54	SEG 53	SEG 52	SEG 51	SEG 50	SEG 49	SEG 48	SEG 50	SEG 49	SEG 48	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43
P1	SEG 47	SEG 46	SEG 45	SEG 44	SEG 43	SEG 42	SEG 41	SEG 40	SEG 42	SEG 41	SEG 40	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35
P2	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29	–	–
P3	SEG 27	SEG 26	SEG 25	SEG 24	SEG 23	SEG 22	SEG 21	SEG 20	–	–	SEG 25	SEG 24	SEG 23	SEG 22	SEG 21	SEG 20
P4	–	–	–	–	–	–	–	–	SEG 27	SEG 26	–	–	–	–	–	–
P5	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4
P7	SEG 19	SEG 18	SEG 17	SEG 16	SEG 15	SEG 14	SEG 13	SEG 12	SEG 19	SEG 18	SEG 17	SEG 16	SEG 15	SEG 14	SEG 13	SEG 12
P9	–	–	–	–	–	–	–	–	SEG3/ COM7	SEG2/ COM6	SEG1/ COM5	SEG0/ COM4	COM3	COM2	COM1	COM0
P13	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 28
P14	–	–	–	–	SEG 31	SEG 30	SEG 29	SEG 28			SEG 55	SEG 54	SEG 53	SEG 52	SEG 51	
Not multiplexed with I/O port																
COM0	–								–							
COM1	–								–							
COM2	–								–							
COM3	–								–							
COM4	SEG0								–							
COM5	SEG1								–							
COM6	SEG2								–							
COM7	SEG3								–							

Note : ( ) indicates the number of signal output pins when 8 com is used.

Remarks: ▭ :Change, ▭ : Delete, – : No corresponding register

2.15 DTC

The basic functions are the same.
In the RL78/L23, additional DTC activation sources have been added to accommodate changes and additions to peripheral functions.

2.16 ELC

The RL78/L23 is equipped with the ELCL, an enhanced version of the traditional ELC. The enhancements include the following features.

To use the ELCL with the same functionality as the conventional ELC, select the “through” option in the logic cell.

- Event signals from peripheral functions can be linked through logic cells (through, AND, OR, EX-OR) to modify activation conditions.
- Event signals from peripheral functions can be routed through a selector to choose activation conditions for specific peripheral functions.
- Event signals can be input to a flip-flop, allowing signal connections to specified peripheral functions in sync with a clock.

2.17 Interrupt Functions

The basic mechanism of interrupts remains unchanged in the RL78/L23.

However, due to the significant expansion of peripheral functions, the interrupt sources, vector table, and registers corresponding to interrupt request sources have been extensively revised.

Therefore, when developing software, refer to the RL78/L23 User’s Manual to correctly handle flags associated with each interrupt source.

2.18 Key Interrupt Function

The basic functions are the same.

2.19 Standby Function

The RL78/L23 adds new functions including RAM shutdown and a setting for fast startup of the High-Speed On-Chip Oscillator upon exiting STOP mode or transitioning from SNOOZE mode.

2.20 Reset Function

In the RL78/L23, a register for initializing peripheral function SFRs has been added.

2.21 Voltage Detector

In the RL78/L23, the voltage detection circuit has been changed from a single LVD to two circuits: LVD0 and LVD1. LVD0 is configured via option bytes as before, while LVD1 can be configured using voltage detection level registers.

2.22 Safety Functions

The RL78/L23 adds several safety functions, including flash memory guard, invalid memory access detection control register (IAWCTL) guard function, and UART loopback functionality.

2.23 Regulator

In the RL78/L23, the regulator output voltage has been changed from (1.8V, 2.1V) to 1.5V.

No special precautions are required.

2.24 Option Bytes

The functions have been expanded and some specifications have been changed, please refer to the User's Manual: Hardware for details. When using boot swap, it is necessary to set an option byte for the boot swap destination address, but since the RL78/L23 can selectively set the boot swap area, the setting address changes according to the boot swap setting.

2.25 Flash Memory

In the RL78/L23, the self-programming software has been changed from the Code/Data Flash Library to the Renesas Flash Driver. For details, please refer to the documentation for the Renesas Flash Driver.

2.26 About the Instruction Set of the RL78/L23

Since the RL78/L23 uses the same S3 core as the RL78/L1C, there are no differences in the instruction set.

3. Documents for Reference

RL78/L1C User's Manual: Hardware (R01UH0409)

RL78/L23 User's Manual: Hardware (R01UH1082)

RL78 Family User's Manual: Software (R01US0015)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.27, 2025	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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(Rev.5.0-1 October 2020)

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