RH850/P1x-C Group

Migration Guide for RH850/P1x-C to RH850/U2C

Introduction

This document provides information on the differences between the RH850/U2C devices and the members of the RH850/P1x-C series. It is intended to support the migration of HW and SW from the RH850/P1x-C devices to the RH850/U2Cx devices.

This application note is derived from RH850/P1x-C Group User's Manual: Hardware and the RH850/U2C Group User's Manual: Hardware, please refer to their latest revisions for detailed information.

Target Device

RH850/U2C Group

- RH850/U2C2
- RH850/U2C4
- RH850/U2C8

Contents

1. Feature overview

This chapter describes the feature differences between the RH850/U2C group devices and the RH850/P1x-C group devices.
The functional details are described in the hardware User's Manuals as referred to in the chapter of the reference documents.

1.1 Feature Overview RH850/U2C2 versus RH850/P1M-C(2MB)

Table 1.1 Feature overview comparison between RH850/U2C2 and RH850/P1M-C(2MB) (1/4)

Function			**RH850/U2C2**		**RH850/P1M-C**		
Number of Pins			**144**	**100**	**292**	**156**	**144**
CPU	Main Core		RH850/G4KH		RH850/G3M		
	FPU		Single precision (32 bit) Double precision (64 bit)		Single precision (32 bit) Double precision (64 bit)		
	MPU	Regions	24		16		
	Frequency	MHz	320		120,160,240		
Memory	Code Flash	MB	2		2		
	Data Flash	KB	128		64		
	Data Flash (HSM)	KB	64		32		
	Local RAM	KB	128		128		
	Cluster RAM	KB	160		-		
	Global RAM	KB	-		320		
	Retention RAM	KB	32		-		
	I-cache RAM	KB	8/core(2way)		16/core		
	Trace RAM	KB	-		-		
DMA Controller		Unit	2		2		
		Channel	16 x 2		8 x 2		
DTS Controller		Unit	1		1		
		Channel	128		128		
OTA update			Yes		-		

Table 1.1 Feature overview comparison between RH850/U2C2 and RH850/P1M-C(2MB) (2/4)

Function					RH850/U2C2		RH850/P1M-C		
Number of Pins					144	100	292	156	144
Oscillator	Main Oscillator		MHz		8/16/20/24		16/20/24		
	Internal Low-speed Oscillator		KHz		32.768		-		
	Internal high-speed Oscillator		MHz		200		-		
	Internal Oscillator		MHz		-		16		
	PLL	PLL0			Yes		Yes		
		PLL1			-		-		
	Sub Clock		KHz		32.768		-		
I/O Port					117	77	99	59	81
Low-power Sampler	LPS		Unit		1		-		
SFMA			Unit		1		-		
MMCA			Unit		-		-		
Clocked Serial Interface	MSPI		Unit		8	6	-		
	CSIH				-		4		
LIN Interface (RLIN2)			Unit		-		-		
LIN/UART Interface (RLIN3)			Unit		16	16	14	2	
I2C Bus Interface (RIIC)			Unit		-		-		
I3C Bus Interface (RI3C)			Unit		3		-		
CANFD Interface (RS-CANFD)			Unit		1		1		
			Channel		6	4	3		
CANXL Interface			Unit		1		-		
Ethernet	AVB (ETNA)		Unit		-		1		
	TSN (ETND) (MII/RMII/SGMII)		Unit	1/1/0	1/1/0	-		-	
	10base-T1S (ETNF) (T1S/RMII)		Unit	1/1	1/1	-		-	
Single Edge Nibble Transmission (RSENT)			Unit		8		6	4	6
Peripheral Sensor Interface 5 (PSI5)			Unit		2		-		
Clock Extension Peripheral Interface (CXPI)			Unit		2	2	-		
FlexRay Interface (FLXA)			Unit		-		2		
I2S Interface (SSIF)			Unit		2		-		

Table 1.1 Feature overview comparison between RH850/U2C2 and RH850/P1M-C(2MB) (3/4)

Function				RH850/U2C2		RH850/P1M-C		
Number of Pins				144	100	292	156	144
Window Watchdog Timer		WDTA	Unit	-		1		
		WDTB		2		-		
OS Timer (OSTM)		Unit		1		-		
System Timer (STM)		Unit		-		1		
Timer Array Unit D (TAU D)		Unit		3		-		
		Channel		16 x 3		-		
Timer Array Unit J (TAU J)		Unit		4		-		
		Channel		4 x 4		-		
Motor Control Timer (TSG3)		Unit		2		-		
Generic Timer Module (GTM)		Unit		1		1		
Time Protection Timer (TPTM)		Timer sets		1		-		
Long-Term System Counter (LTSC)		Unit		1		-		
Timer Option (TAPA)		Unit		4		-		
Real-time Clock (RTCA)		Unit		1		-		
Encoder Timer (ENCA)		Unit		1		-		
Peripheral Interconnect (PIC)		PIC1	Unit	1		-		
		PIC2		3		1		
PWM Output/Diagnostic (PWM-Diag)		Channel		64	48	-		
SAR-ADC		Unit		2		2		
	ADCF0	Physical Channels		-		12	8	10
	ADCF1	Physical Channels		-		12	8	10
	ADCA1/K1	high accuracy ports		16	15	-		
		Low accuracy ports		8	6	-		
	ADCKA	high accuracy ports		12	4	-		
		Low accuracy ports		14	10	-		
Temperature Sensor		Unit		1		1		

Table 1.1 Feature overview comparison between RH850/U2C2 and RH850/P1M-C(2MB) (4/4)

Function				**RH850/U2C2**		**RH850/P1M-C**		
Number of Pins				**144**	**100**	**292**	**156**	**144**
Functional Safety	ASIL Level			D		D		
	Data CRC	Function B (DCRB)	Channel	-		4		
		Function K (KCRC)		8		-		
	Error Control Module (ECM)		Unit	1		1		
	Core Voltage Monitor (CVM)			-		Yes		
	Voltage Monitor (VMON)			Yes		-		
	Clock Monitor (CLMA)			Yes		Yes		
	Power-On Clear (POC)			Yes		Yes		
	Error Correction Coding			Yes		Yes		
	Error injection for self-diagnosis of several safety mechanisms			Yes		Yes		
	LBIST			Yes		Yes		
	MBIST			Yes		Yes		
	Low-Voltage Indicator (LVI)			-		-		
Hardware Security Module (HSM)				ICUMHB		ICUMC		
Debug	On-Chip debug (OCD)			Yes		Yes		
	Single Wire Debug (SWD)			-		-		
	Low Pin Debug (LPD4)			Yes		Yes		
	Nexus-JTAG			Yes		Yes		
	Trace I/F (Aurora)			-		-		
Boundary SCAN				Yes		Yes		
External Interrupts	Maskable			40		10	9	9
	Non-maskable (NMI)			1		1		

1.2 Feature Overview RH850/U2C4 versus RH850/P1H-C(4MB)

Table 1.2 Feature overview comparison between RH850/U2C4 and RH850/P1H-C(4MB) (1/4)

Function			**RH850/U2C4**			**RH850/P1H-C(4MB)**	
Number of Pins			**292**	**144**	**100**	**292**	**156**
CPU	Main Core		RH850/G4KH			RH850/G3M	
	FPU		Single precision (32 bit) Double precision (64 bit)			Single precision (32 bit) Double precision (64 bit)	
	MPU	Regions	24			16	
	Frequency	MHz	320			160,240	
Memory	Code Flash	MB	4			4	
	Data Flash	KB	256			128	
	Data Flash (HSM)	KB	64			32	
	Local RAM	KB	PE1: 128 PE2: 128			PE1:64 PE2:64	
	Cluster RAM	KB	448			-	
	Global RAM	KB	-			960	
	Retention RAM	KB	32			-	
	I-cache RAM	KB	8/core(2way)			16/core	
	Trace RAM	KB	-			-	
DMA Controller		Unit	2			2	
		Channel	16 x 2			8 x 2	
DTS Controller		Unit	1			1	
		Channel	128			128	
OTA update			Yes			-	

Table 1.2 Feature overview comparison between RH850/U2C4 and RH850/P1H-C(4MB) (2/4)

Function					RH850/U2C4			RH850/P1H-C(4MB)	
Number of Pins					292	144	100	292	156
Oscillator	Main Oscillator		MHz		8/16/20/24			16/20/24	
	Internal Low-speed Oscillator		KHz		32.768			-	
	Internal high-speed Oscillator		MHz		200			-	
	Internal Oscillator		MHz		-			16	
	PLL	PLL0			Yes			Yes	
		PLL1			-			-	
	Sub Clock		KHz		32.768			-	
I/O Port					190	117	77	137	66
Low-power Sampler	LPS	Unit			1			-	
SFMA		Unit			1			-	
MMCA		Unit			1			-	
Clocked Serial Interface	MSPI	Unit			8			-	
	CSIH				-			4	
LIN Interface (RLIN2)		Unit			-			-	
LIN/UART Interface (RLIN3)		Unit			16	16	14	4	2
I2C Bus Interface (RIIC)		Unit			-			-	
I3C Bus Interface (RI3C)		Unit			3			-	
CANFD Interface (RS-CANFD)		Unit			1			1	
		Channel			6	6	4	3	
CANXL Interface		Unit			2			-	
Ethernet	AVB (ETNA)	Unit			-			1	1
	TSN (ETND) (MII/RMII/SGMII)	Unit	1/1/0	1/1/0	0/1/0			-	
	10base-T1S (ETNF) (T1S/RMII)	Unit	1/1	1/1	1/0			-	
Single Edge Nibble Transmission (RSENT)		Unit			8			8	4
Peripheral Sensor Interface 5 (PSI5)		Unit			2			-	
Clock Extension Peripheral Interface (CXPI)		Unit			4	2	2	-	
FlexRay Interface (FLXA)		Unit			1[2ch]			2	1
I2S Interface (SSIF)		Unit			2			-	

Table 1.2 Feature overview comparison between RH850/U2C4 and RH850/P1H-C(4MB) (3/4)

Function				RH850/U2C4			RH850/P1H-C(4MB)	
Number of Pins				292	144	100	292	156
Window Watchdog Timer		WDTA	Unit	-			2	
		WDTB		3			-	
OS Timer (OSTM)		Unit		2			-	
System Timer (STM)		Unit		-			2	
Timer Array Unit D (TAU D)		Unit		3			-	
		Channel		16 x 3			-	
Timer Array Unit J (TAU J)		Unit		4			-	
		Channel		4 x 4			-	
Motor Control Timer (TSG3)		Unit		2			-	
Generic Timer Module (GTM)		Unit		1			1	
Time Protection Timer (TPTM)		Timer sets		2			-	
Long-Term System Counter (LTSC)		Unit		1			-	
Timer Option (TAPA)		Unit		4			-	
Real-time Clock (RTCA)		Unit		1			-	
Encoder Timer (ENCA)		Unit		1			-	
Peripheral Interconnect (PIC)		PIC1	Unit	1			-	
		PIC2		3			1	
PWM Output/Diagnostic (PWM-Diag)		Channel		96	64	48	-	
SAR-ADC		Unit		2			2	
	ADCF0	Physical Channels		-			16	8
	ADCF1	Physical Channels		-			16	8
	ADCA1/K1	high accuracy ports		20	16	15	-	
		Low accuracy ports		14	8	6	-	
	ADCKA	high accuracy ports		20	12	4	-	
		Low accuracy ports		14	14	10	-	
Temperature Sensor		Unit		1			1	

Table 1.2 Feature overview comparison between RH850/U2C4 and RH850/P1H-C(4MB) (4/4)

Function				RH850/U2C4			RH850/P1H-C(4MB)	
Number of Pins				292	144	100	292	156
Functional Safety	ASIL Level			D			D	
	Data CRC	Function B (DCRB)	Channel	-			8	
		Function K (KCRC)		8			-	
	Error Control Module (ECM)		Unit	1			2	
	Core Voltage Monitor (CVM)			-			Yes	
	Voltage Monitor (VMON)			Yes			-	
	Clock Monitor (CLMA)			Yes			Yes	
	Power-On Clear (POC)			Yes			Yes	
	Error Correction Coding			Yes			Yes	
	Error injection for self-diagnosis of several safety mechanisms			Yes			Yes	
	LBIST			Yes			Yes	
	MBIST			Yes			Yes	
	Low-Voltage Indicator (LVI)			-			-	
hardware Security Module				ICUMHB			ICUMC	
Debug	On-Chip debug (OCD)			Yes			Yes	
	Single Wire Debug (SWD)			-			-	
	Low Pin Debug (LPD4)			Yes			Yes	
	Nexus-JTAG			Yes			Yes	
	Trace I/F (Aurora)			-			-	
Boundary SCAN				Yes			Yes	
External Interrupts	Maskable			40			12	
	Non-maskable (NMI)			1			1	

1.3 Feature Overview RH850/U2C8 versus RH850/P1H-C(8MB)

Table 1.3 Feature overview comparison between RH850/U2C8 and RH850/P1H-C(8MB) (1/4)

Function			**RH850/U2C8**	**RH850/P1H-C(8MB)**
Number of Pins			**292**	**292**
CPU	Main Core		RH850/G4KH	RH850/G3M
	FPU		Single precision (32 bit) Double precision (64 bit)	Single precision (32 bit) Double precision (64 bit)
	MPU	Regions	24	16
	Frequency	MHz	320	160,240
Memory	Code Flash	MB	8	8
	Data Flash	KB	384	192
	Data Flash (HSM)	KB	64	32
	Local RAM	KB	PE1: 128 PE2: 128	PE1:64 PE2:64
	Cluster RAM	KB	1248	-
	Global RAM	KB	-	960
	Retention RAM	KB	32	-
	I-cache RAM	KB	8/core(2way)	16/core
	Trace RAM	KB	-	-
DMA Controller		Unit	2	2
		Channel	16 x 2	8 x 2
DTS Controller		Unit	1	1
		Channel	128	128
OTA update			Yes	-

Table 1.3 Feature overview comparison between RH850/U2C8 and RH850/P1H-C(8MB) (2/4)

Function				RH850/U2C8	RH850/P1H-C(8MB)
Number of Pins				**292**	**292**
Oscillator	Main Oscillator		MHz	8/16/20/24	16/20/24
	Internal Low-speed Oscillator		KHz	32.768	-
	Internal high-speed Oscillator		MHz	200	-
	Internal Oscillator		MHz	-	16
	PLL	PLL0		Yes	Yes
		PLL1		-	-
	Sub Clock		KHz	32.768	-
I/O Port				181	130
Low-power Sampler	LPS	Unit		1	-
SFMA		Unit		1	-
MMCA		Unit		1	-
Clocked Serial Interface	MSPI	Unit		10	-
	CSIH			-	4
LIN Interface (RLIN2)		Unit		-	-
LIN/UART Interface (RLIN3)		Unit		20	4
I2C Bus Interface (RIIC)		Unit		-	-
I3C Bus Interface (RI3C)		Unit		4	-
CANFD Interface (RS-CANFD)		Unit		2	1
		Channel		14	3
CANXL Interface		Unit		2	-
Ethernet	AVB (ETNA)	Unit		-	2
	TSN (ETND0) (MII/RMII/SGMII)	Unit		1/1/0	-
	TSN (ETND1) (MII/RMII/SGMII)	Unit		0/0/1	
	10base-T1S (ETNF) (T1S/RMII)	Unit		1/1	-
Single Edge Nibble Transmission (RSENT)		Unit		8	8
Peripheral Sensor Interface 5 (PSI5)		Unit		2	-
Peripheral Sensor Interface 5 S (PSI5S)		Unit		1	-
Clock Extension Peripheral Interface (CXPI)		Unit		4	-
FlexRay Interface (FLXA)		Unit		1[2ch]	4
I2S Interface (SSIF)		Unit		2	-

Table 1.3 Feature overview comparison between RH850/U2C8 and RH850/P1H-C(8MB) (3/4)

Function				RH850/U2C8	RH850/P1H-C(8MB)
Number of Pins				**292**	**292**
Window Watchdog Timer		WDTA	Unit	-	2
		WDTB		3	-
OS Timer (OSTM)		Unit		2	-
System Timer (STM)		Unit		-	2
Timer Array Unit D (TAU D)		Unit		3	-
		Channel		16 x 3	-
Timer Array Unit J (TAU J)		Unit		4	-
		Channel		4 x 4	-
Motor Control Timer (TSG3)		Unit		2	-
Generic Timer Module (GTM)		Unit		1	1
Time Protection Timer (TPTM)		Timer sets		2	-
Long-Term System Counter (LTSC)		Unit		1	-
Timer Option (TAPA)		Unit		4	-
Real-time Clock (RTCA)		Unit		1	-
Encoder Timer (ENCA)		Unit		1	-
Peripheral Interconnect (PIC)		PIC1	Unit	1	-
		PIC2		3	1
PWM Output/Diagnostic (PWM-Diag)		Channel		96	-
SAR-ADC		Unit		2	2
	ADCF0	Physical Channels		-	20
	ADCF1	Physical Channels		-	20
	ADCA1/K1	high accuracy ports		20	-
		Low accuracy ports		14	-
	ADCKA	high accuracy ports		20	-
		Low accuracy ports		14	-
Temperature Sensor		Unit		1	1

Table 1.3 Feature overview comparison between RH850/U2C8 and RH850/P1H-C(8MB) (4/4)

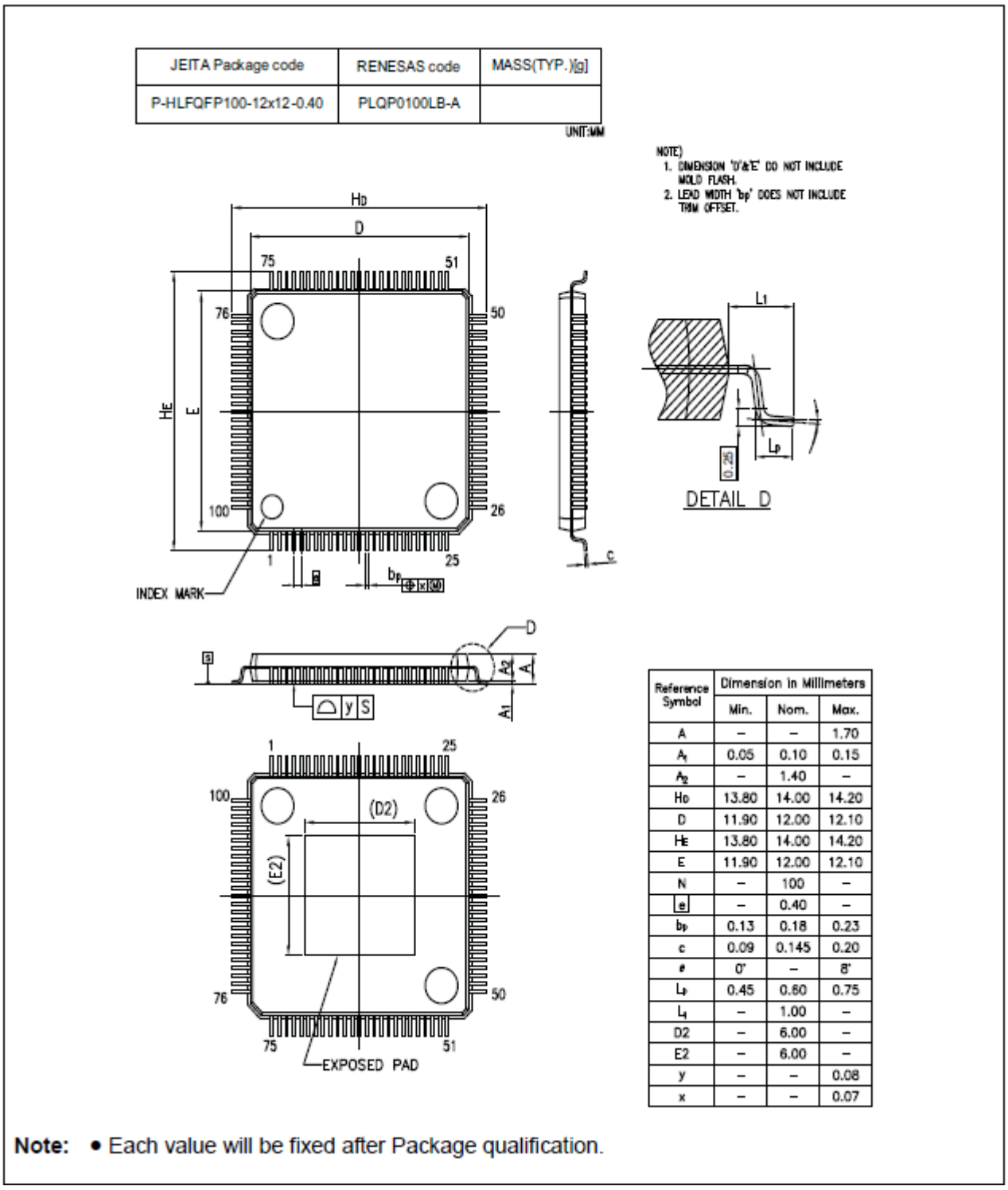
Function				RH850/U2C8	RH850/P1H-C(8MB)
Number of Pins				**292**	**292**
Functional Safety	ASIL Level			D	D
	Data CRC	Function B (DCRB)	Channel	-	8
		Function K (KCRC)		8	-
	Error Control Module (ECM)		Unit	1	2
	Core Voltage Monitor (CVM)			-	Yes
	Voltage Monitor (VMON)			Yes	-
	Clock Monitor (CLMA)			Yes	Yes
	Power-On Clear (POC)			Yes	Yes
	Error Correction Coding			Yes	Yes
	Error injection for self-diagnosis of several safety mechanisms			Yes	Yes
	LBIST			Yes	Yes
	MBIST			Yes	Yes
	Low-Voltage Indicator (LVI)			-	-
hardware Security Module				ICUMHB	ICUMC
Debug	On-Chip debug (OCD)			Yes	Yes
	Single Wire Debug (SWD)			-	-
	Low Pin Debug (LPD4)			Yes	Yes
	Nexus-JTAG			Yes	Yes
	Trace I/F (Aurora)			-	-
Boundary SCAN				Yes	Yes
External Interrupts	Maskable			40	12
	Non-maskable (NMI)			1	1

Note: U2C2, U2C4, U2C8 and P1M-C, P1H-C(4MB), P1H-C(8MB) were used as examples in this document, for more details refer to **RH850/P1x-C Group User's Manual: Hardware** or **RH850/U2C Group User's Manual: Hardware**

2. Package and pinout

2.1 Package

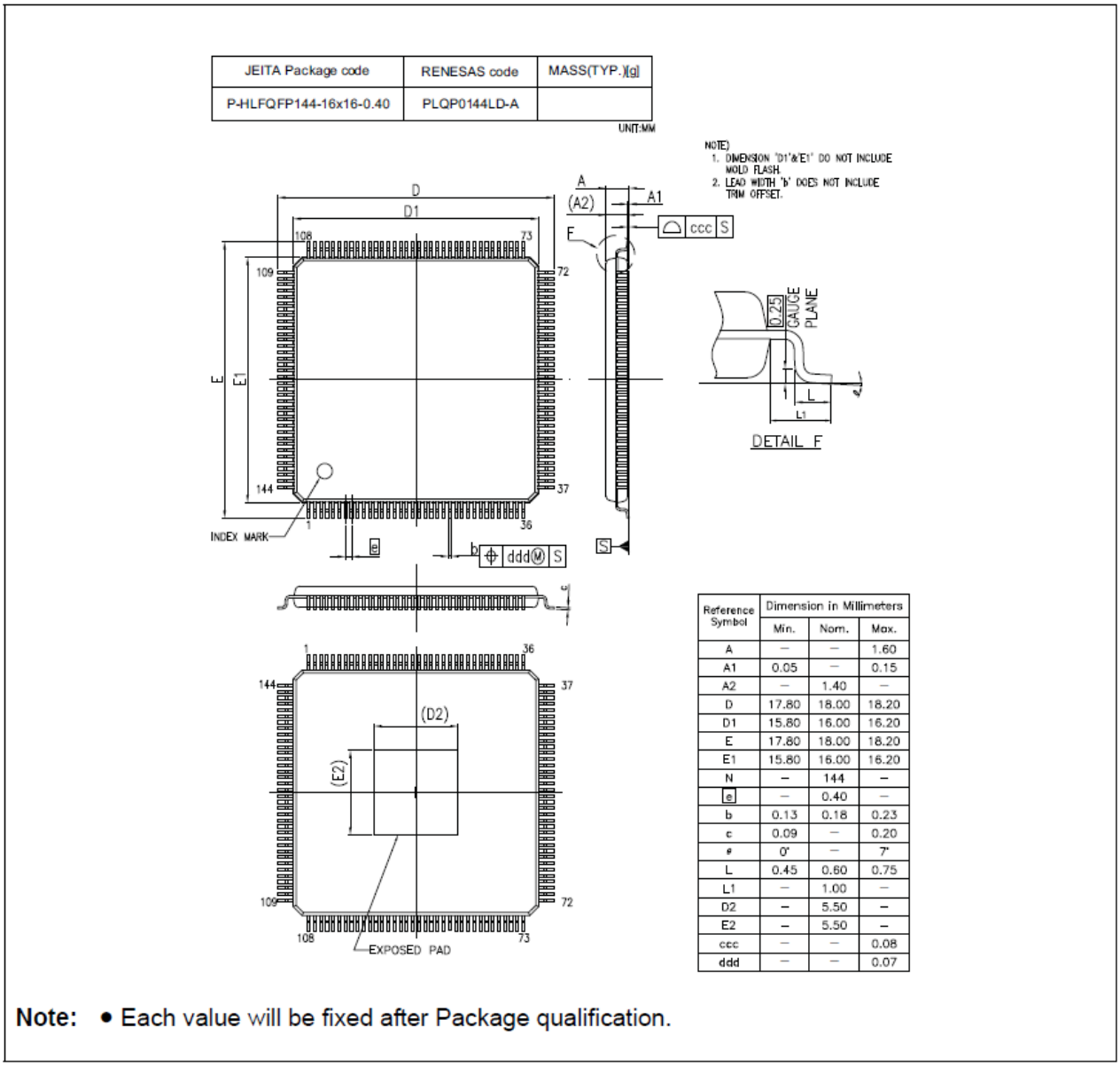
The 100 pin (12x12 mm) and 144 pin (16x16 mm) packages of U2C4 and U2C2 have the same dimensions.
The 144 pin (16x16 mm) package of U2CX and P1X-C have the same dimensions.



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.70
A_1	0.05	0.10	0.15
A_2	–	1.40	–
HD	13.80	14.00	14.20
D	11.90	12.00	12.10
HE	13.80	14.00	14.20
E	11.90	12.00	12.10
N	–	100	–
e	–	0.40	–
bp	0.13	0.18	0.23
c	0.09	0.145	0.20
θ	0°	–	8°
Lp	0.45	0.60	0.75
L1	–	1.00	–
D2	–	6.00	–
E2	–	6.00	–
y	–	–	0.08
x	–	–	0.07

Note: • Each value will be fixed after Package qualification.

Figure 2.1 HLQFP100 (0.4 mm ball pitch) outline for U2C4 and U2C2



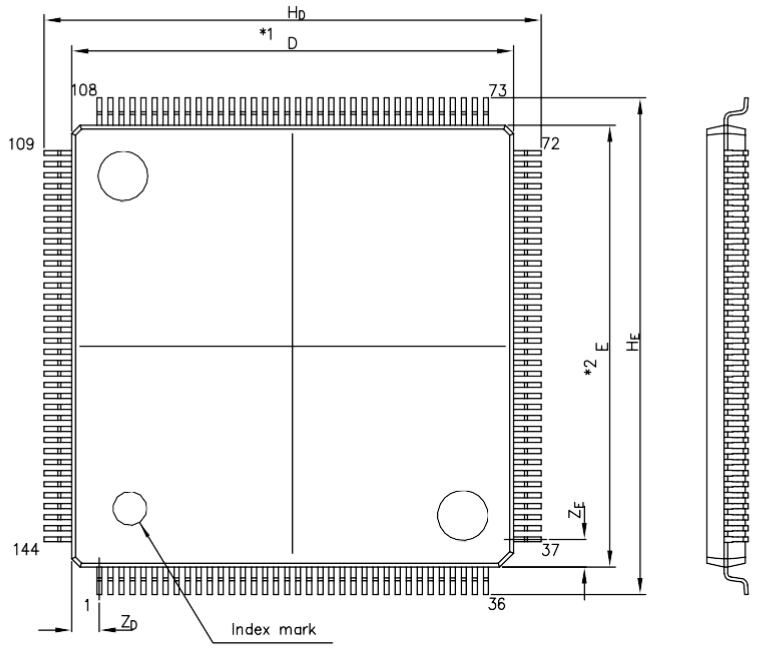
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	–	1.40	–
D	17.80	18.00	18.20
D1	15.80	16.00	16.20
E	17.80	18.00	18.20
E1	15.80	16.00	16.20
N	–	144	–
e	–	0.40	–
b	0.13	0.18	0.23
c	0.09	–	0.20
θ	0°	–	7°
L	0.45	0.60	0.75
L1	–	1.00	–
D2	–	5.50	–
E2	–	5.50	–
ccc	–	–	0.08
ddd	–	–	0.07

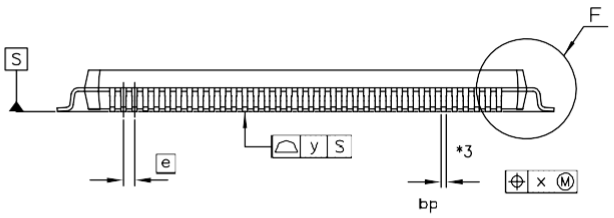
Note: • Each value will be fixed after Package qualification.

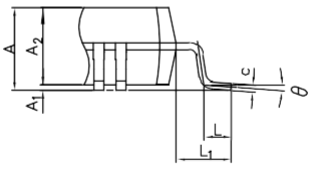
Figure 2.2 HLQFP144 (0.4 mm ball pitch) outline for U2C4 and U2C2

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-16x16-0.40	PLQP0144LB-A	——	0.9g

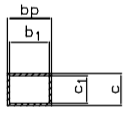
Unit: mm







Detail F



Terminal cross section

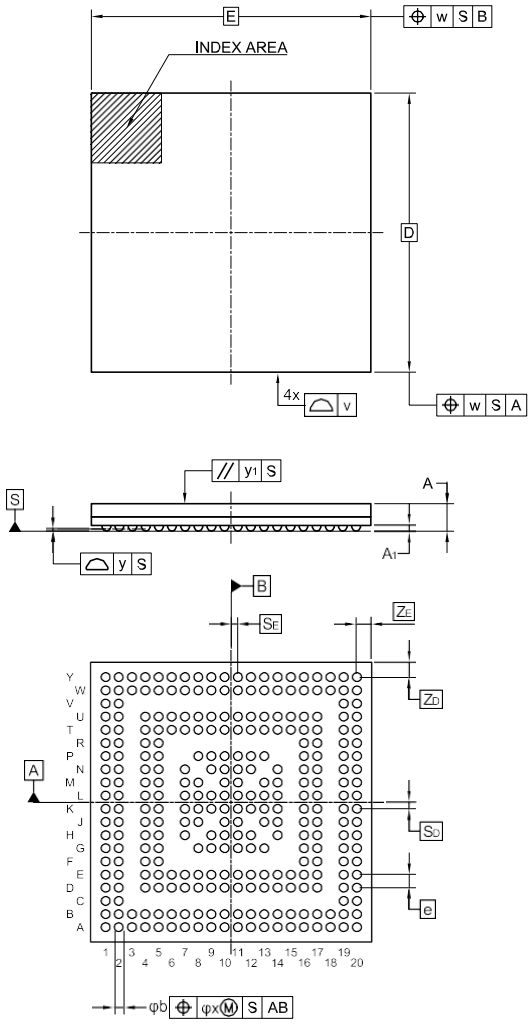
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A2	——	1.4	——
HD	17.8	18.0	18.2
HE	17.8	18.0	18.2
A	——	——	1.7
A1	0.05	0.10	0.15
bp	0.13	0.18	0.23
b1	——	0.16	——
c	0.09	0.145	0.20
c1	——	0.125	——
θ	0°	——	8°
e	——	0.4	——
x	——	——	0.07
y	——	——	0.08
ZD	——	1.0	——
ZE	——	1.0	——
L	0.35	0.5	0.65
L1	——	1.0	——

Figure 2.3 LQFP144 outline of P1M-C

U2C8 and U2C4 share the same dimensions for FBGA 292 with 17 mm x 17 mm and 0.8 ball pitch which is the same with the FBGA 292 of P1x-C.

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA292-17X17-0.80	PRBG0292GC-A	T292F1-80-GNP	0.9



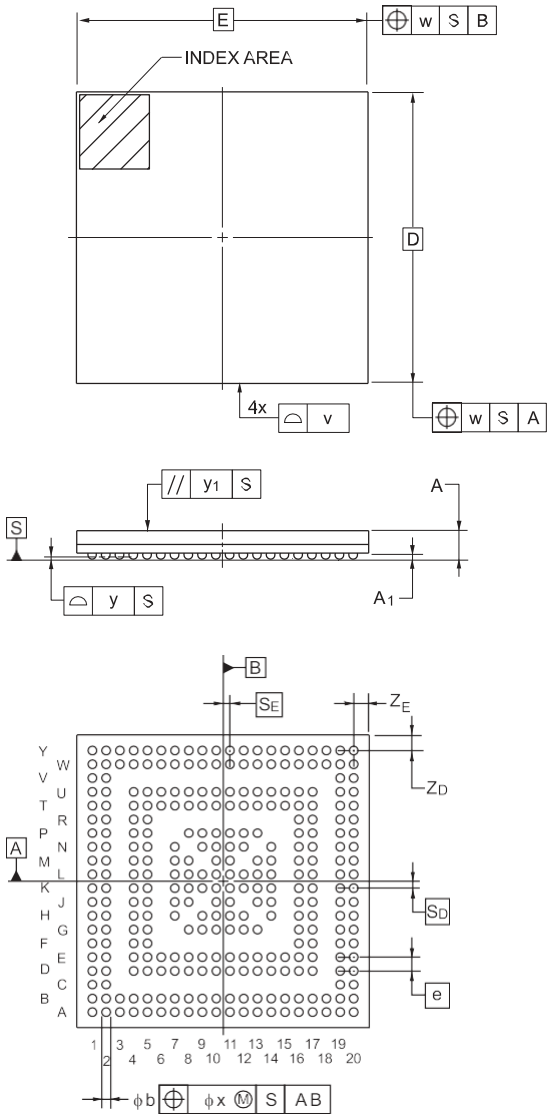
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	–	17.00	–
E	–	17.00	–
A	–	–	1.90
A_1	0.30	0.35	0.40
e	–	0.80	–
b	0.50	0.55	0.60
x	–	–	0.12
y	–	–	0.10
y_1	–	–	0.20
Z_D	–	0.90	–
Z_E	–	0.90	–
v	–	–	0.15
w	–	–	0.20
S_D	–	0.40	–
S_E	–	0.40	–

Note: INDEX AREA is on the corner near a ball A1 (Top view side).

Figure 2.4 FBGA292 outline of U2C4 and U2C8

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ.) [g]
P-FBGA292-17x17-0.80	PRBG0292GC-A	T292F1-80-GNP	—

Unit: mm

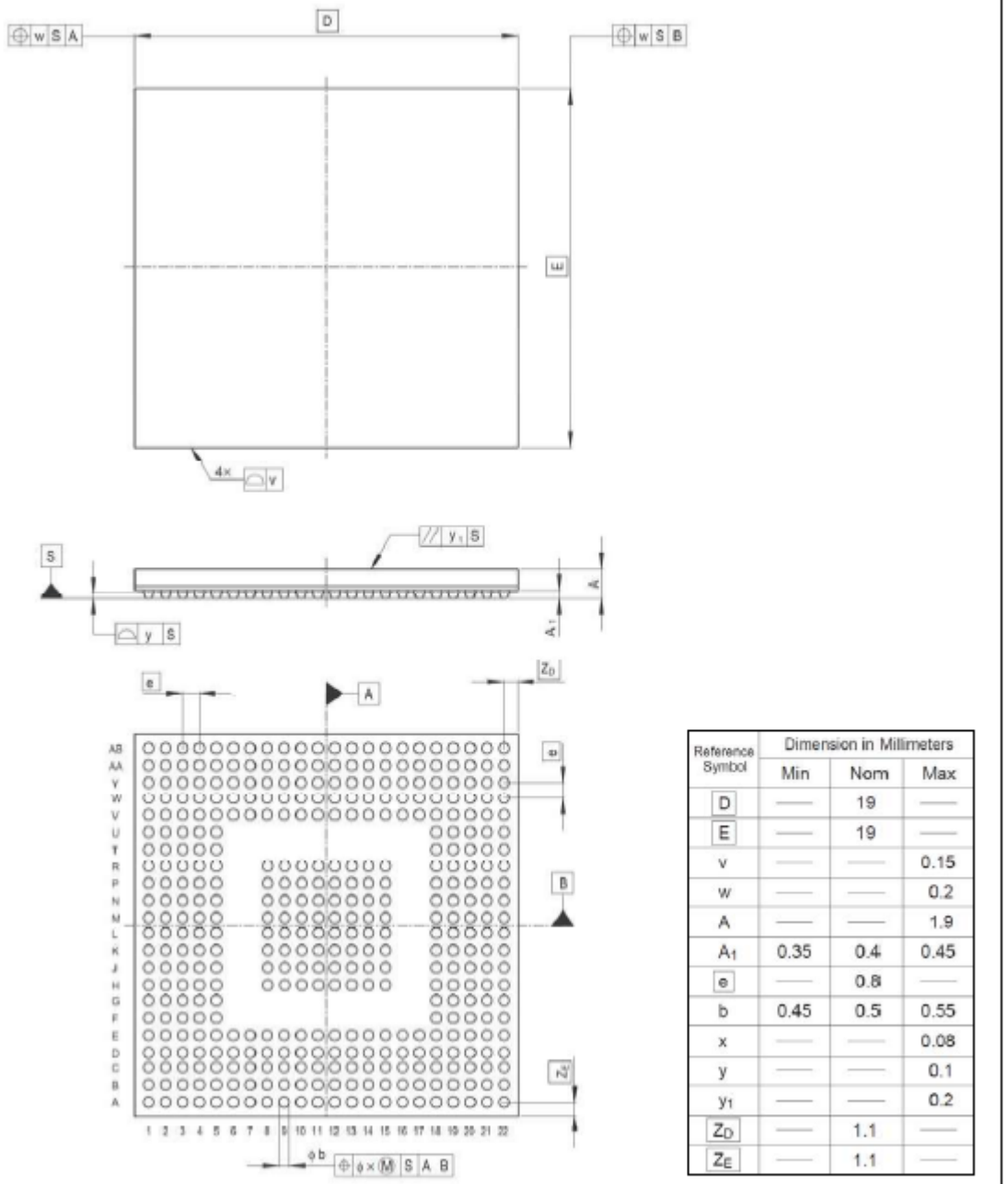


Reference symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	17.00	—
E	—	17.00	—
A	—	—	1.90
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.50	0.55	0.60
x	—	—	0.12
y	—	—	0.10
y_1	—	—	0.20
Z_D	—	0.90	—
Z_E	—	0.90	—
v	—	—	0.15
w	—	—	0.20
So	—	0.40	—
Se	—	0.40	—

Figure 2.5 FBGA292 pin outline for P1H-C(4MB), P1H-C(8MB)

U2C8-EVA FBGA 404 shares the same dimensions with P1x-C FBGA 404 of 19 mm x 19 mm with 0.8 ball pitch.

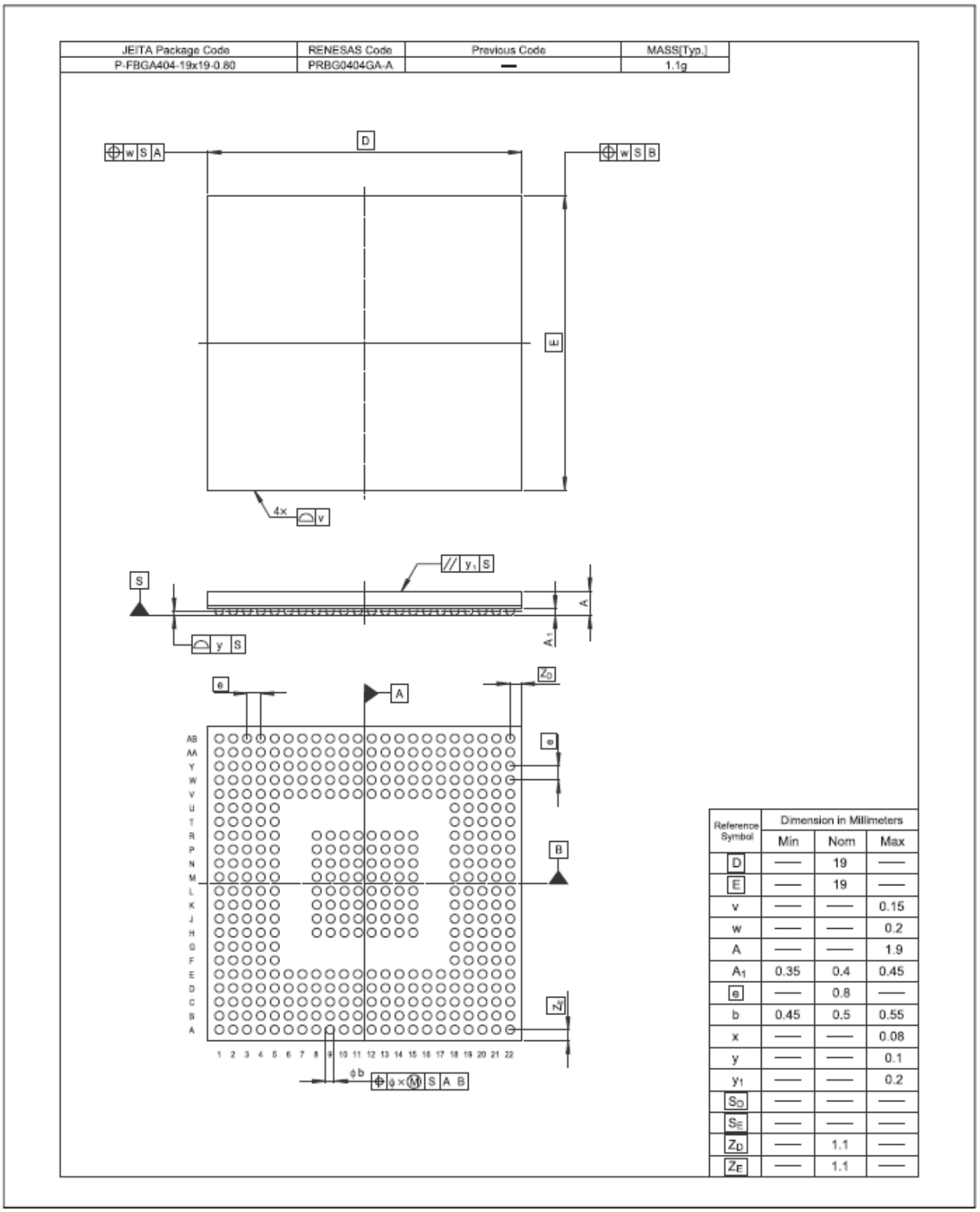
JEITA Package Code	RENESAS Code	Previous Code	MASS(TYP.)[g]
P-FBGA404-19x19-0.80	PRBG0404GA-A	-	1.1



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	19	—
E	—	19	—
v	—	—	0.15
w	—	—	0.2
A	—	—	1.9
A_1	0.35	0.4	0.45
e	—	0.8	—
b	0.45	0.5	0.55
x	—	—	0.08
y	—	—	0.1
y_1	—	—	0.2
Z_D	—	1.1	—
Z_E	—	1.1	—

Note: • INDEX AREA is on the corner near a ball A1 (Top view side).

Figure 2.6 FBGA404 pin outline for U2C8-EVA

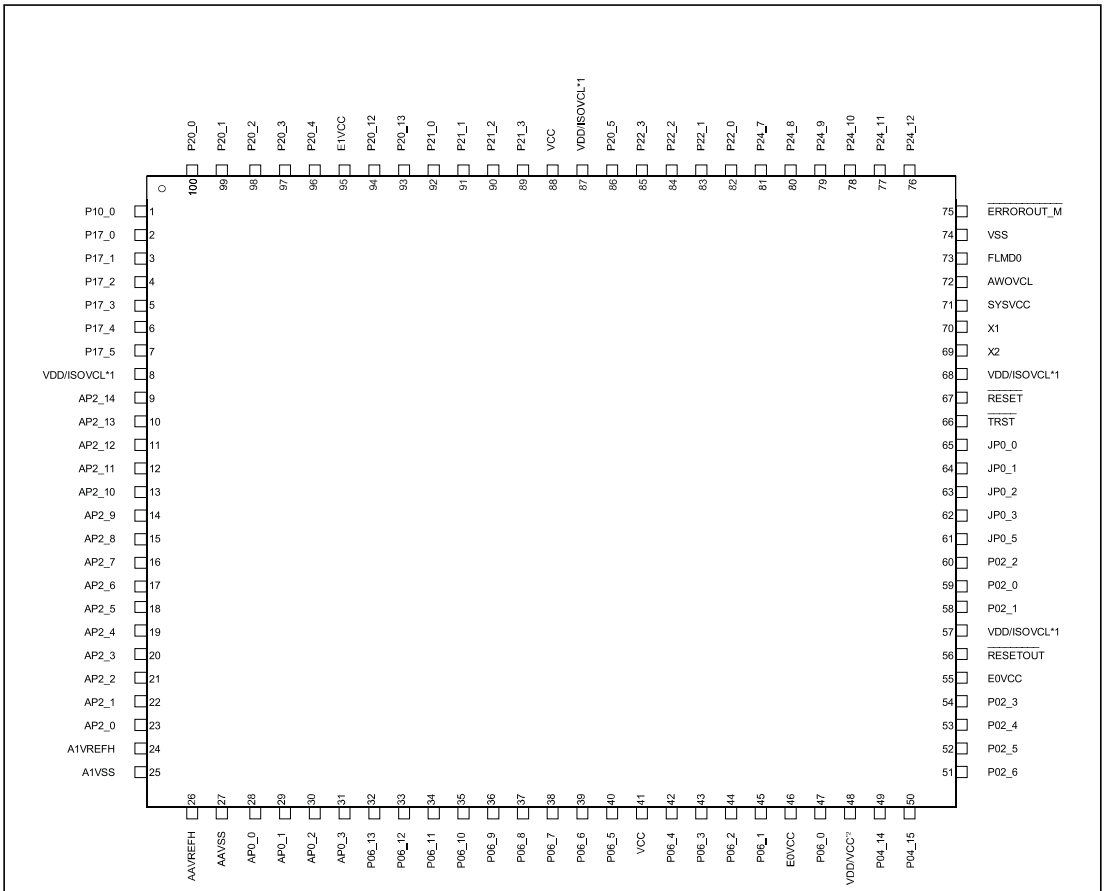


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	19	—
E	—	19	—
v	—	—	0.15
w	—	—	0.2
A	—	—	1.9
A_1	0.35	0.4	0.45
e	—	0.8	—
b	0.45	0.5	0.55
x	—	—	0.08
y	—	—	0.1
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	1.1	—
Z_E	—	1.1	—

Figure 2.7 FBGA404 pin outline for P1H-CE

2.2 Pinout comparison

Both U2C2 and U2C4 have an option for a package of 100 pins (HLQFP100) which can be seen in figure 2.8 below. This 100 pins package is not available in P1x-C.



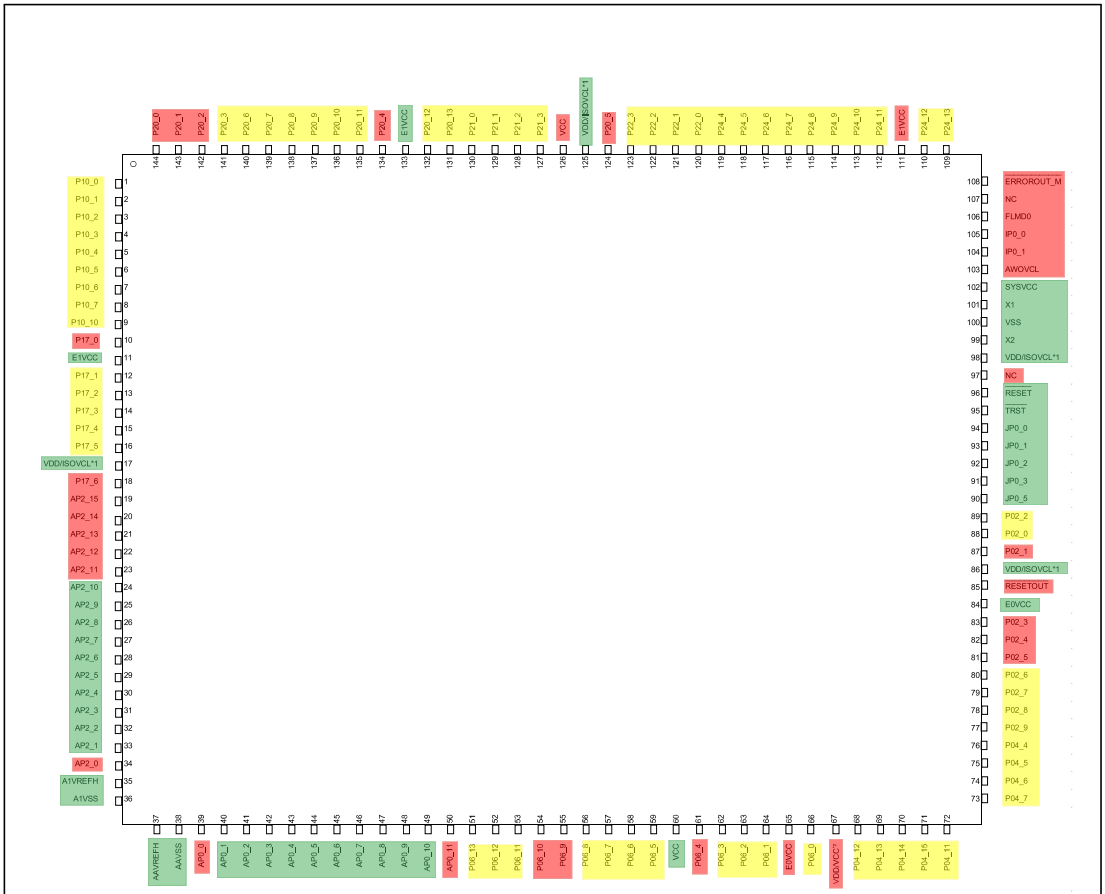
Note 1. VDD on U2C4 DPS package. ISOVCL on U2C4 eVR package and U2C2.

Note 2. VDD on U2C4 DPS package. VCC on U2C4 eVR package and U2C2.

Note: The Exposed Pad shall be connected to VSS.

Figure 2.8 Pin Connection Diagram RH850/U2C4, U2C2 (HLQFP100)

Both U2C2 and U2C4 have an option for a package of 144 pins (HLQFP144) which can be seen in figure 2.9 below. This 144-pin package is available for P1x-C group for P1M-C microcontroller. The differences between those 2 packages are shown in the figure below.



Note 1. VDD on U2C4 DPS package. ISOVCL on U2C4 eVR package and U2C2.
Note 2. VDD on U2C4 DPS package. VCC on U2C4 eVR package and U2C2.

Note: The Exposed Pad shall be connected to VSS.

Figure 2.9 Pin Connection Diagram RH850/U2C4, U2C2 (HLQFP144)

Note:

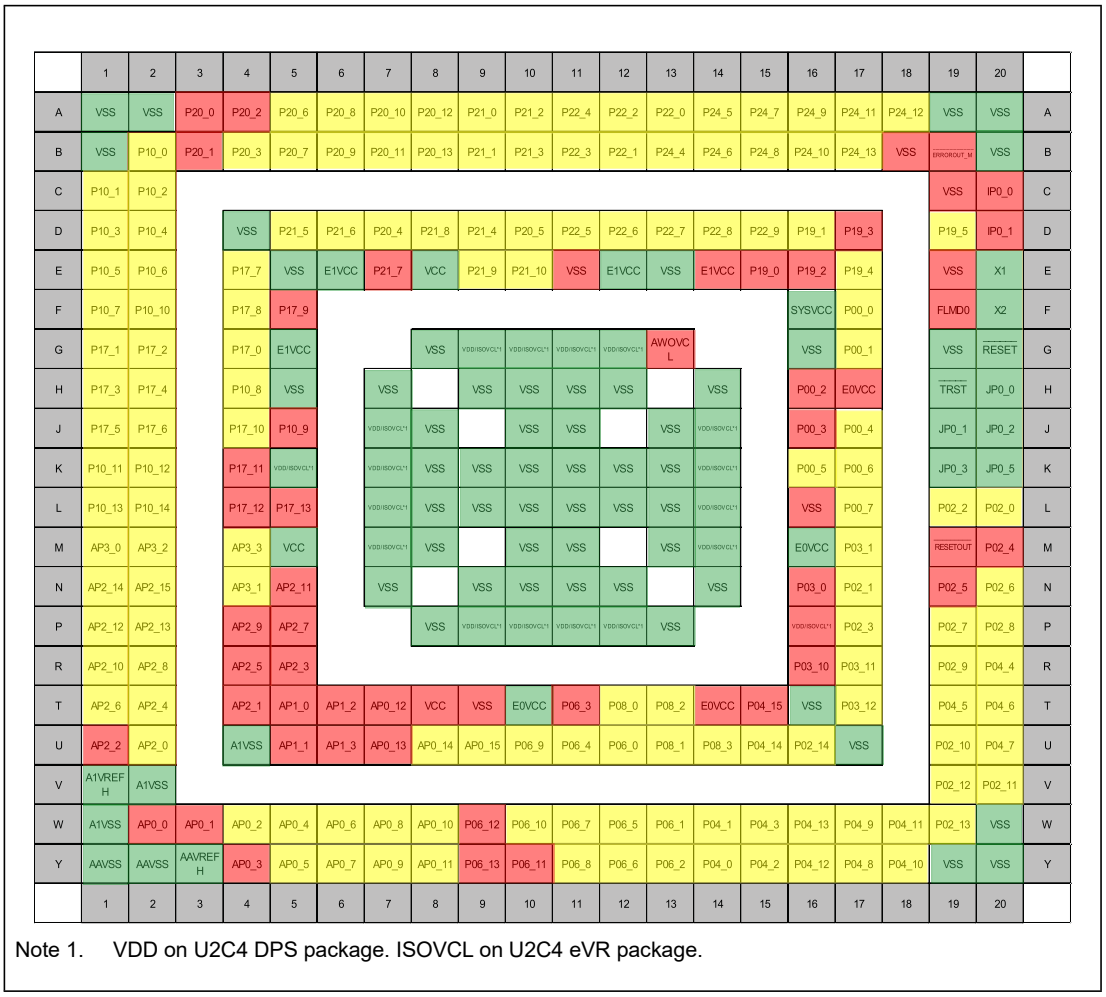
Pins of U2C4 or U2C2 do not have same functionality as pins of P1M-C

Pins of U2C4 or U2C2 have similar functionality as pins of P1M-C, with differences in alternate functions

Pins of U2C4 or U2C2 have the same functionality as pins of P1M-C

Note: Pins JP0_n (n = 0, 1, 2, 3, 5) of U2C have more alternative functions.

U2C4 devices have an option for a package of 292 pins (BGA292) which can be seen in figure 2.10 below. This 292 pins package is available for P1x-C group for P1H-C (4MB) microcontroller. The differences between those 2 packages are shown in the figure below.



Note 1. VDD on U2C4 DPS package. ISOVCL on U2C4 eVR package.

Figure 2.10 Pin Connection Diagram RH850/U2C4 (BGA292)

Note:

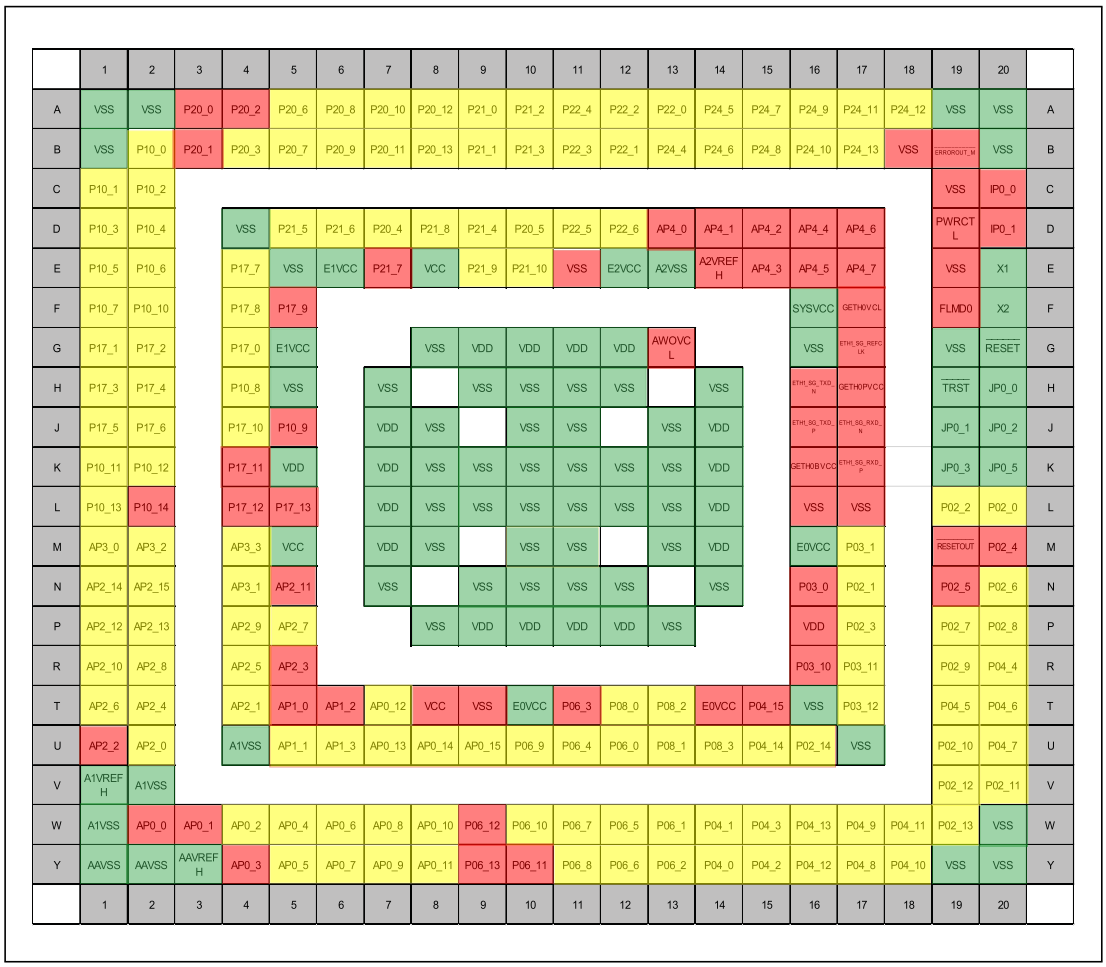
Pins of U2C4 do not have same functionality as pins of P1H-C(4MB)

Pins of U2C4 have similar functionality as pins of P1H-C(4MB), with differences in alternate functions

Pins of U2C4 have the same functionality as pins of P1H-C(4MB)

Note: Pins JP0_n (n = 0, 1, 2, 3, 5) of U2C have more alternative functions.

U2C8 devices have an option for a package of 292 pins (BGA292) which can be seen in figure 2.11 below. This 292 pins package is available for P1x-C group for P1H-C (8MB) microcontroller. The differences between those 2 packages are shown in the figure below.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	P20_0	P20_2	P20_6	P20_8	P20_10	P20_12	P21_0	P21_2	P22_4	P22_2	P22_0	P24_5	P24_7	P24_9	P24_11	P24_12	VSS	VSS	A
B	VSS	P10_0	P20_1	P20_3	P20_7	P20_9	P20_11	P20_13	P21_1	P21_3	P22_3	P22_1	P24_4	P24_6	P24_8	P24_10	P24_13	VSS	ERROROUT_M	VSS	B
C	P10_1	P10_2																	VSS	IP0_0	C
D	P10_3	P10_4		VSS	P21_5	P21_6	P20_4	P21_8	P21_4	P20_5	P22_5	P22_6	AP4_0	AP4_1	AP4_2	AP4_4	AP4_6		PWRCTL	IP0_1	D
E	P10_5	P10_6		P17_7	VSS	E1VCC	P21_7	VCC	P21_9	P21_10	VSS	E2VCC	A2VSS	A2VREFH	AP4_3	AP4_5	AP4_7		VSS	X1	E
F	P10_7	P10_10		P17_8	P17_9											SYSVCC	GETH0VCL		FLMD0	X2	F
G	P17_1	P17_2		P17_0	E1VCC			VSS	VDD	VDD	VDD	VDD	AWOVCL			VSS	ETH1_SG_REFCLK		VSS	RESET	G
H	P17_3	P17_4		P10_8	VSS		VSS		VSS	VSS	VSS	VSS		VSS		ETH1_SG_TXD_N	GETH0PVCC		TRST	JP0_0	H
J	P17_5	P17_6		P17_10	P10_9		VDD	VSS		VSS	VSS		VSS	VDD		ETH1_SG_TXD_P	ETH1_SG_RXD_N		JP0_1	JP0_2	J
K	P10_11	P10_12		P17_11	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GETH0BVCC	ETH1_SG_RXD_P		JP0_3	JP0_5	K
L	P10_13	P10_14		P17_12	P17_13		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	VSS		P02_2	P02_0	L
M	AP3_0	AP3_2		AP3_3	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P03_1		RESETOUT	P02_4	M
N	AP2_14	AP2_15		AP3_1	AP2_11		VSS		VSS	VSS	VSS	VSS		VSS		P03_0	P02_1		P02_5	P02_6	N
P	AP2_12	AP2_13		AP2_9	AP2_7			VSS	VDD	VDD	VDD	VDD	VSS			VDD	P02_3		P02_7	P02_8	P
R	AP2_10	AP2_8		AP2_5	AP2_3											P03_10	P03_11		P02_9	P04_4	R
T	AP2_6	AP2_4		AP2_1	AP1_0	AP1_2	AP0_12	VCC	VSS	E0VCC	P06_3	P08_0	P08_2	E0VCC	P04_15	VSS	P03_12		P04_5	P04_6	T
U	AP2_2	AP2_0		A1VSS	AP1_1	AP1_3	AP0_13	AP0_14	AP0_15	P06_9	P06_4	P06_0	P08_1	P08_3	P04_14	P02_14	VSS		P02_10	P04_7	U
V	A1VREFH	A1VSS																	P02_12	P02_11	V
W	A1VSS	AP0_0	AP0_1	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P06_12	P06_10	P06_7	P06_5	P06_1	P04_1	P04_3	P04_13	P04_9	P04_11	P02_13	VSS	W
Y	AAVSS	AAVSS	AAVREFH	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P06_13	P06_11	P06_8	P06_6	P06_2	P04_0	P04_2	P04_12	P04_8	P04_10	VSS	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 2.11 Pin Connection Diagram RH850/U2C8 (BGA292)

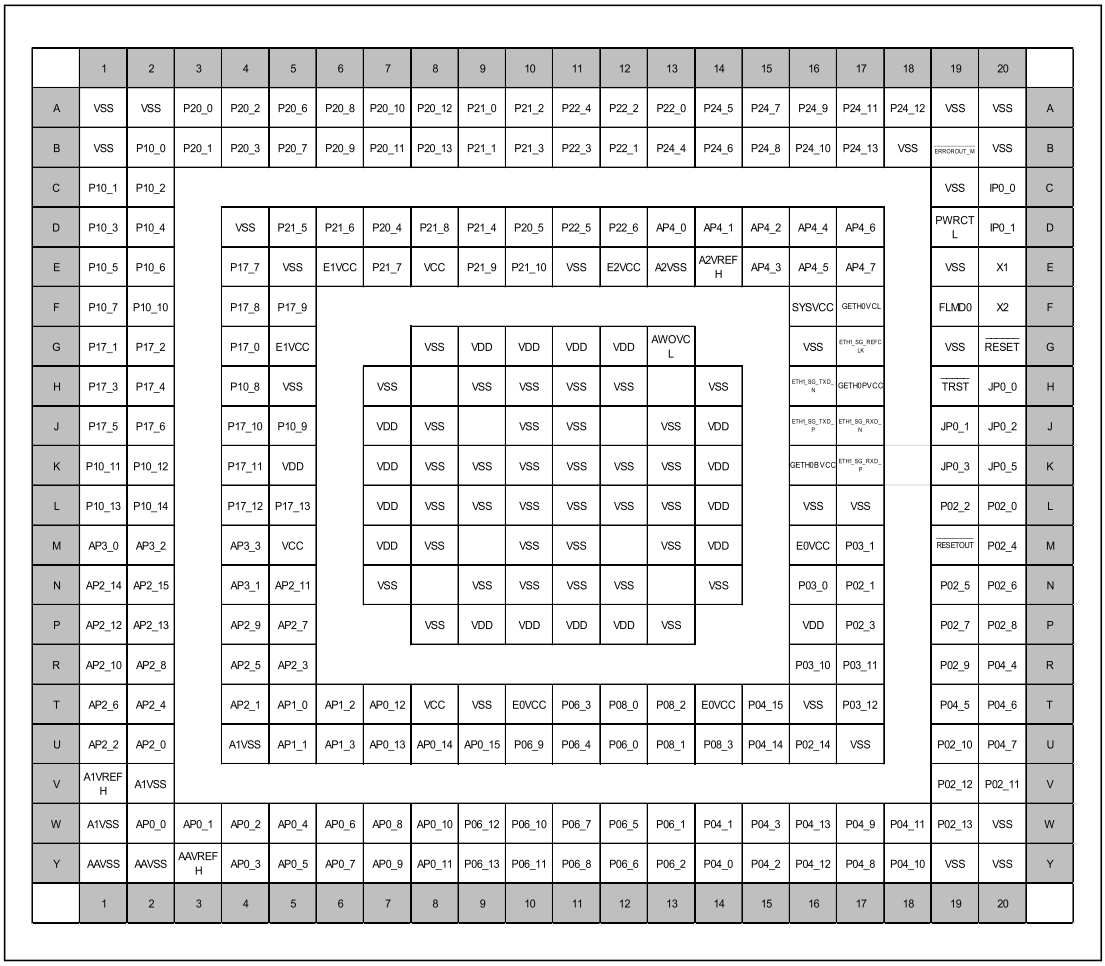
Note:

Pins of U2C8 do not have same functionality as pins of P1H-C(8MB)

Pins of U2C8 have similar functionality as pins of P1H-C(8MB), with differences in alternate functions

Pins of U2C8 have the same functionality as pins of P1H-C(8MB)

Note: Pins JP0_n (n = 0, 1, 2, 3, 5) of U2C have more alternative functions.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	P20_0	P20_2	P20_6	P20_8	P20_10	P20_12	P21_0	P21_2	P22_4	P22_2	P22_0	P24_5	P24_7	P24_9	P24_11	P24_12	VSS	VSS	A
B	VSS	P10_0	P20_1	P20_3	P20_7	P20_9	P20_11	P20_13	P21_1	P21_3	P22_3	P22_1	P24_4	P24_6	P24_8	P24_10	P24_13	VSS	ERROROUT_M	VSS	B
C	P10_1	P10_2																	VSS	IP0_0	C
D	P10_3	P10_4		VSS	P21_5	P21_6	P20_4	P21_8	P21_4	P20_5	P22_5	P22_6	AP4_0	AP4_1	AP4_2	AP4_4	AP4_6		PWRCTL	IP0_1	D
E	P10_5	P10_6		P17_7	VSS	E1VCC	P21_7	VCC	P21_9	P21_10	VSS	E2VCC	A2VSS	A2VREFH	AP4_3	AP4_5	AP4_7		VSS	X1	E
F	P10_7	P10_10		P17_8	P17_9											SYSVCC	GETH0VCL		FLMD0	X2	F
G	P17_1	P17_2		P17_0	E1VCC			VSS	VDD	VDD	VDD	VDD	AWOVCL			VSS	ETH1_SG_REFCLK		VSS	RESET	G
H	P17_3	P17_4		P10_8	VSS		VSS		VSS	VSS	VSS	VSS		VSS		ETH1_SG_TXD_N	GETH0PVCC		TRST	JP0_0	H
J	P17_5	P17_6		P17_10	P10_9		VDD	VSS		VSS	VSS		VSS	VDD		ETH1_SG_TXD_P	ETH1_SG_RXD_N		JP0_1	JP0_2	J
K	P10_11	P10_12		P17_11	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GETH0BVCC	ETH1_SG_RXD_P		JP0_3	JP0_5	K
L	P10_13	P10_14		P17_12	P17_13		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	VSS		P02_2	P02_0	L
M	AP3_0	AP3_2		AP3_3	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P03_1		RESETOUT	P02_4	M
N	AP2_14	AP2_15		AP3_1	AP2_11		VSS		VSS	VSS	VSS	VSS		VSS		P03_0	P02_1		P02_5	P02_6	N
P	AP2_12	AP2_13		AP2_9	AP2_7			VSS	VDD	VDD	VDD	VDD	VSS			VDD	P02_3		P02_7	P02_8	P
R	AP2_10	AP2_8		AP2_5	AP2_3											P03_10	P03_11		P02_9	P04_4	R
T	AP2_6	AP2_4		AP2_1	AP1_0	AP1_2	AP0_12	VCC	VSS	E0VCC	P06_3	P08_0	P08_2	E0VCC	P04_15	VSS	P03_12		P04_5	P04_6	T
U	AP2_2	AP2_0		A1VSS	AP1_1	AP1_3	AP0_13	AP0_14	AP0_15	P06_9	P06_4	P06_0	P08_1	P08_3	P04_14	P02_14	VSS		P02_10	P04_7	U
V	A1VREFH	A1VSS																	P02_12	P02_11	V
W	A1VSS	AP0_0	AP0_1	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P06_12	P06_10	P06_7	P06_5	P06_1	P04_1	P04_3	P04_13	P04_9	P04_11	P02_13	VSS	W
Y	AAVSS	AAVSS	AAVREFH	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P06_13	P06_11	P06_8	P06_6	P06_2	P04_0	P04_2	P04_12	P04_8	P04_10	VSS	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 2.12 Pin Connection Diagram RH850/U2C8-EVA (BGA404)

2.3 PORT Overview

2.3.1 General Features

RH850/U2C ports provide more advanced access protection, configuration options, and safe state features while RH850/P1x-C (P1H-C 4MB) ports are more straightforward general-purpose I/O without explicit access protection categories or advanced safe state functions.

Both families support high pin-count packages and configurable I/O, but U2C is tailored for applications requiring enhanced security, networking, and lower standby current.

Figures 2.13 and 2.14 show the block diagram of the port control functions of RH850/U2C and RH850/P1x-C. For smaller devices or other members in the device series, please refer to Hardware User's Manual for details.

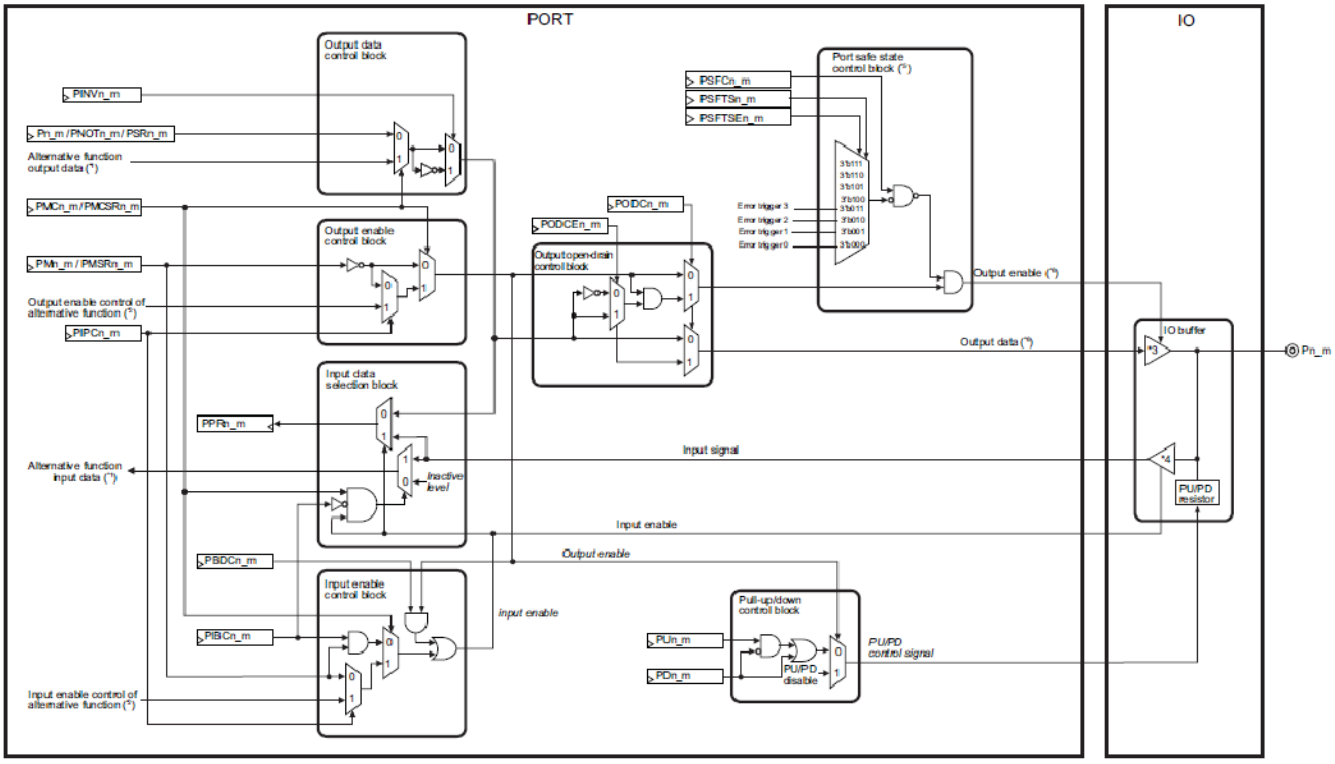


Figure 2.13 Block diagram of the port control function in U2C

Note 1. Alternative function signal selected by PFCn_m, PFCEn_m, PFCAEn_m and PFCEAEn_m.

Note 2. Only functions exist in RH850/U2C Group User's Manual: Hardware **Table 2.28, Alternative functions require "Direct I/O Control" (Must Set PIPCn_m=1)** are supported this configuration.

Note 3. The output drive strength can be set by PDSCn_m and PUCCn_m.

Note 4. The input buffer type can be set by PISn_m and PISAn_m.

Note 5. Details of Port Safe State function are described in RH850/U2C Group User's Manual: Hardware **Section 2.4.2, Port Safe State Function**.

Note 6. P17_0, P17_1, P20_0 and P20_1 are target pins for ICUM select function which requires additional higher priority control. For details, refer to RH850/U2C Group User's Manual: Hardware **Section 2.4.3, ICUM Select Function**.

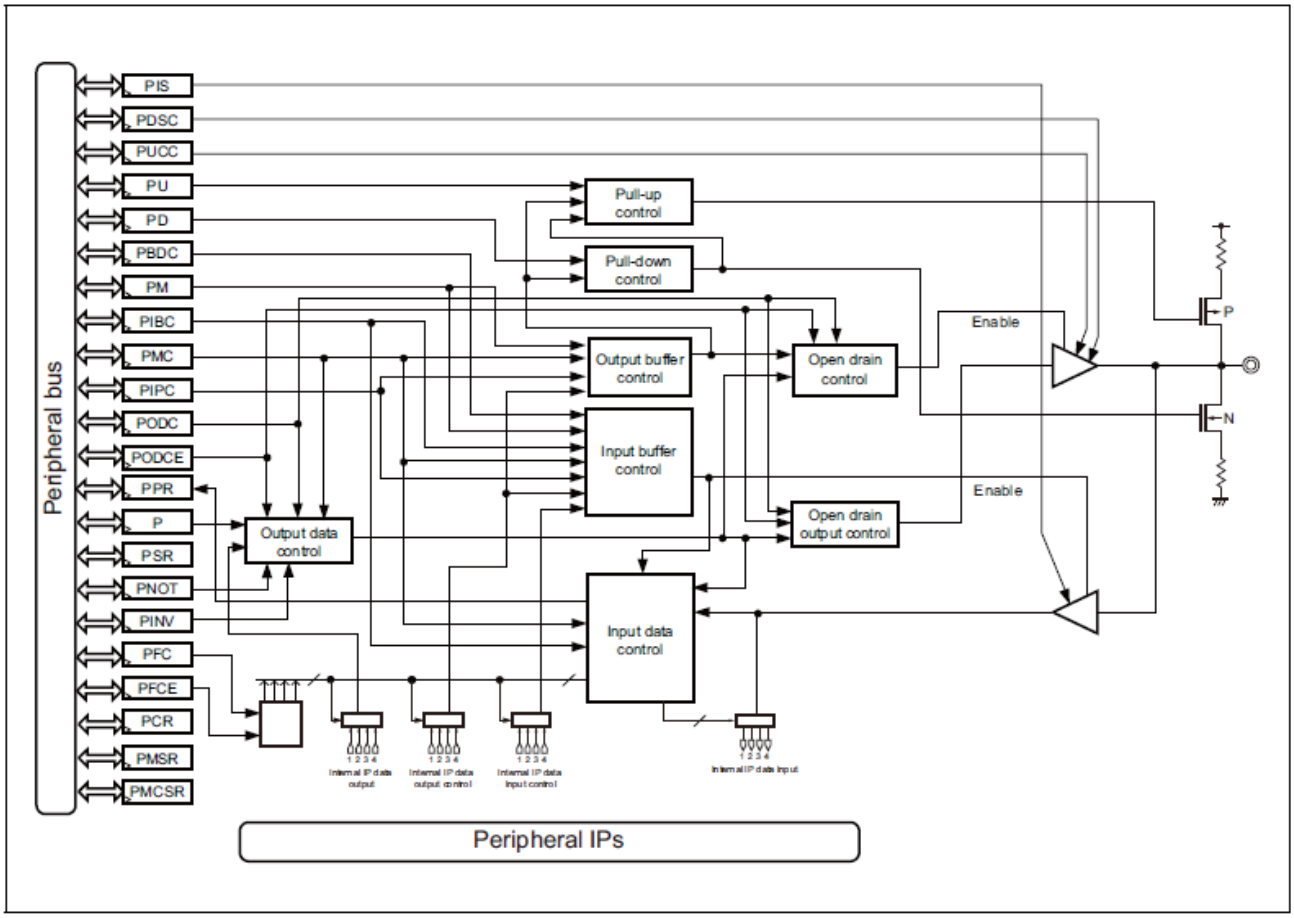


Figure 2.14 Block diagram of the port control function in P1x-C

Besides, there are also implementation differences in terms of:

- I/O Port Numbers
- Clock connections
- Base address

Please refer to the related User manual chapters for details.

2.3.2 I/O Port Numbers

The unit and/or channel number is different between RH850/U2C and RH850/P1x-C. For details, please refer to RH850/U2C Group User's Manual: Hardware **Appendix "E02_01_List_of_Pin_Assignment.xlsx"** and RH850/P1x-C Group User's Manual: Hardware **Section 2.1.1 Pin List and Function assignment**

2.3.3 Clock Supply

Table 2.1 shows the difference between the supplied clock of the PIN function on the RH850/U2C devices and the RH850/P1x-C devices.

Table 2.1 Clock Supply of the PIN function on U2C and P1x-C Devices

Unit Name	RH850/U2C	RH850/P1x-C
Register_access_clock	CLK_LSB	CLK_LSB

2.3.4 Register Base Address

Table 2.2 shows the differences between the register base address of the PIN function on the RH850/U2C devices and the RH850/P1x-C devices.

Table 2.2 Register Base Address of the PIN function on U2C and P1x-C Devices

Base Address Name	RH850/U2C	RH850/P1x-C
<PORT_base>	FFD9 0000$_H$	FFC1 0000$_H$
<JPORT_base>	FFDA 0000$_H$	FFC2 0000$_H$

3. CPU System

RH850/G4KH Core is implemented in RH850/U2C devices, while RH850/G3M processor is implemented in RH850/P1x-C devices.

Table 3.1 provides information of the General Features of the CPU system.

Table 3.1 Features of CPU System

Item	Features	
	RH850/U2C	**RH850/P1x-C**
Processor	RH850G4KH	RH850/G3M
Architecture profile	High performance 32-bit architecture for embedded control	Advanced 32-bit architecture for embedded control
FPU	Supports single precision (32-bits) and double precision (64-bits). Supports IEEE754-compliant data types and exceptions.	Supports single precision (32 bits) and double precision (64 bits). Supports data types and exceptions conforming to IEEE754.
DSP	-	-
External Coprocessor interface	-	-
MPU	24 areas settable	16 areas settable
Wake-up Interrupt Controller	Supported.	Supported.
Debug watchpoints and breakpoints	A maximum of 12 breakpoints can be specified. Asynchronous Break function is supported.	A maximum of 12 breakpoints can be specified.
Cross Trigger Interface (CTI)	-	-
Level of Instrumentation trace	This microcontroller provides several trace functions including branch PC trace and data trace for each CPU, and DMA data trace.	This product provides several trace functions including branch PC trace of the CPU, data trace, and DMA data trace.
Embedded Trace Macrocell (ETM)	-	-
Macro Trace Buffer (MTB)	-	-
Cache	I-Cache	I-Cache
SBIST	-	-

Figure 3.1 shows the block configuration diagram of RH850/P1H-CE.

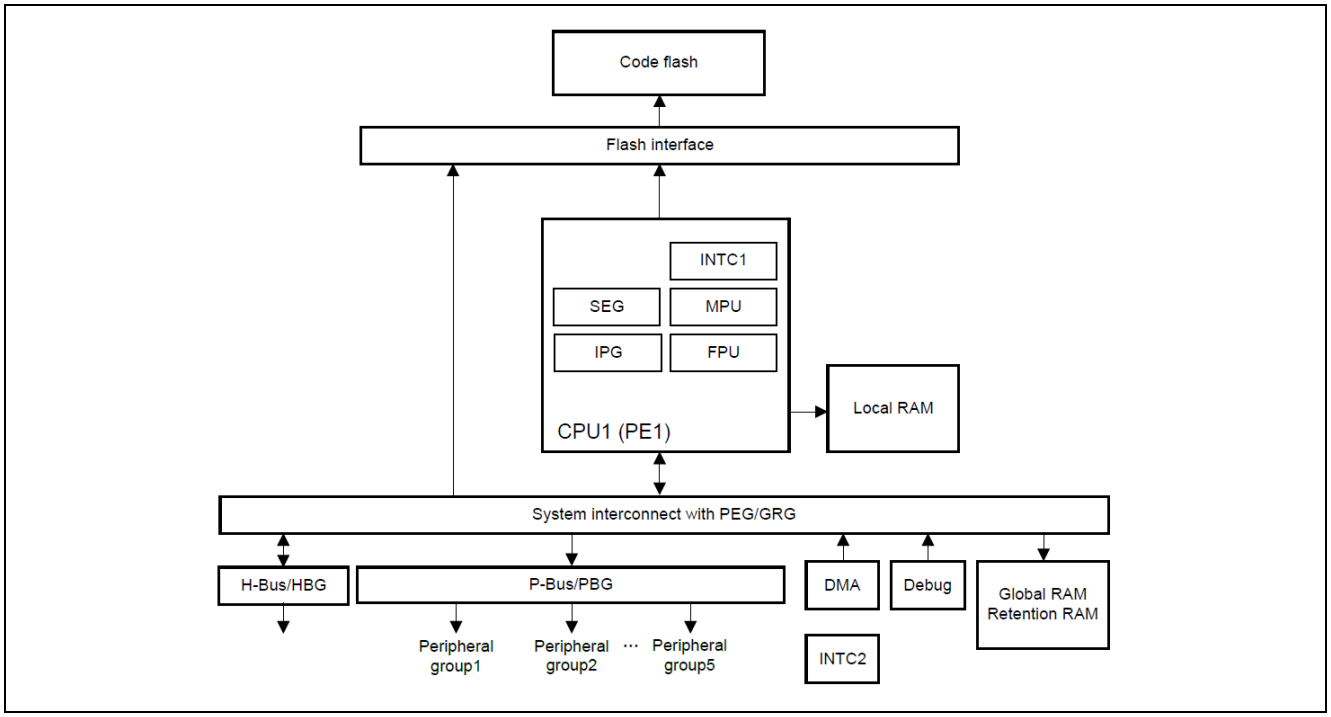


Figure 3.1 Block Diagram of the RH850/P1H-CE

For the block diagram of the CPU system in U2C see Figure 4.1

4. Bus Architecture

The U2C4 architecture has a multi-core RH850 automotive MCU bus system, built around a crossbar bus matrix that connects CPU cores, Flash/RAM, DMA, and peripheral groups (timers, ADC, CAN, Ethernet, etc.). It is optimized for real-time, safety-critical automotive applications, supporting high data throughput and parallelism.

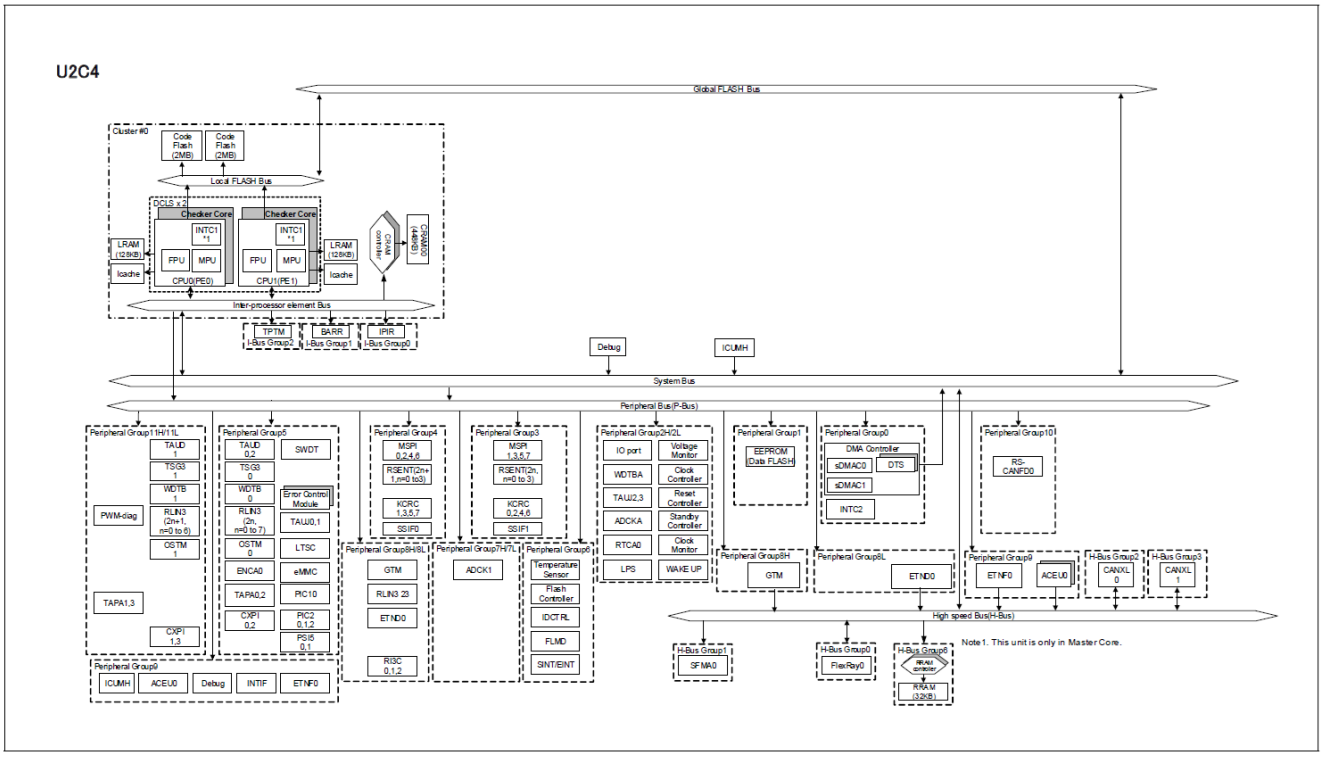


Figure 4.1 Internal Block Diagram (U2C4)

This RH850/P1x-C MCU uses a shared bus matrix that connects multiple CPU cores, memories, and peripherals, enabling parallel access for real-time automotive tasks.

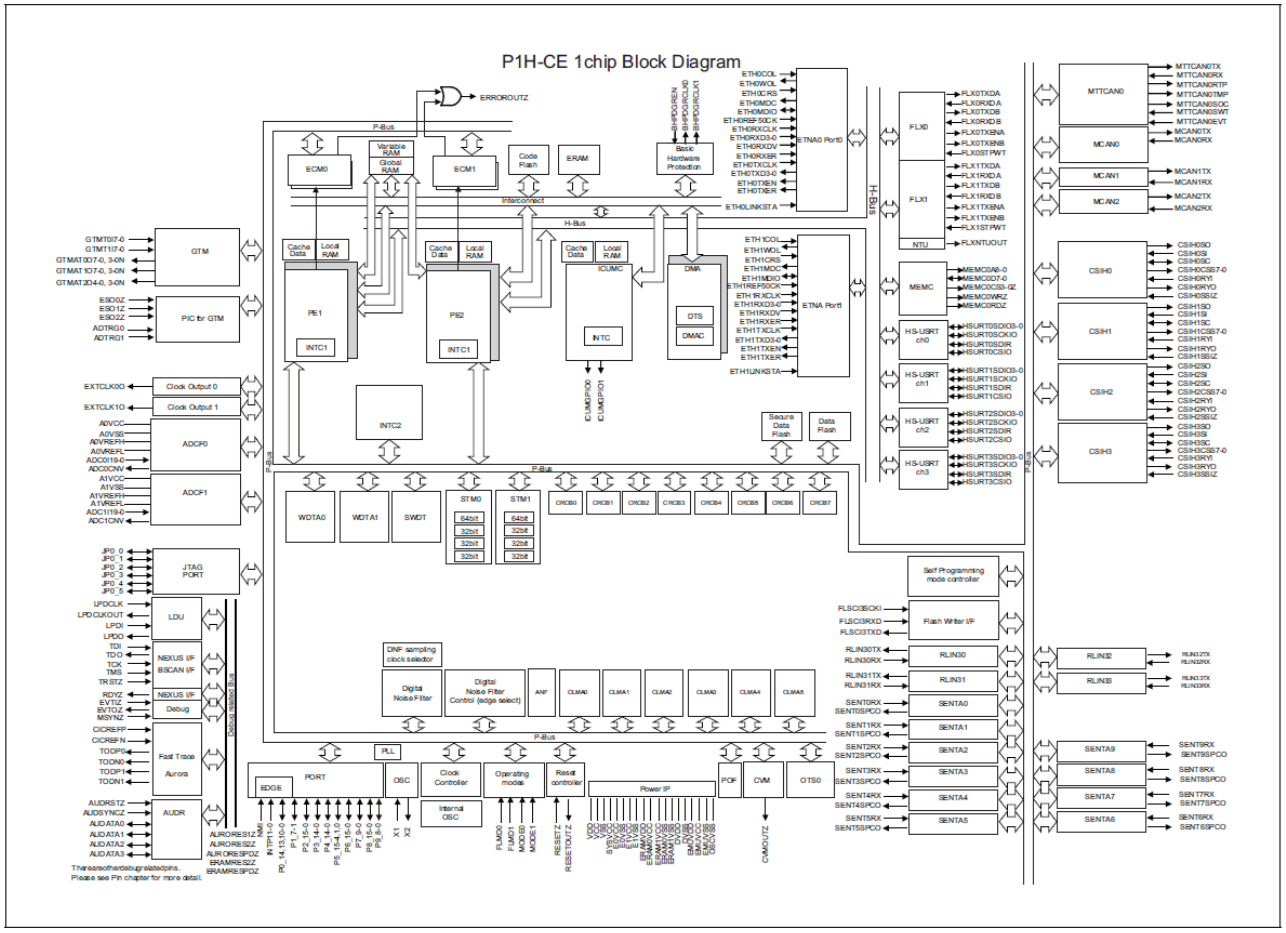


Figure 4.2 RH850/P1x-C chip block diagram (P1H-CE)

5. Address Space

The Table 5.1 shows the general overview of memory distribution in U2C and P1x-C devices.

Table 5.1 Memory distribution in U2C and P1x-C

Device	RH850/U2C			RH850/P1x-C		
	U2C2	U2C4	U2C8	P1M-C(2MB)	P1H-C(4MB)	P1H-C(8MB)
Code Flash [MB]	2	4	8	2	4	8
Data Flash [KB]	128 + 64(HSM)	256 + 64(HSM)	384 + 64(HSM)	64 + 32(HSM)	128 + 32(HSM)	192 + 32(HSM)
Local RAM [KB]	128/core	128/core	128/core	128(one core)	64/core	64/core
Retention RAM [KB]	32	32	32	-	-	-

Tables 5.2, 5.3 and Figure 5.1 shows address space for U2C and P1x-C Devices.

Table 5.2 Address space (Single Map Mode) - U2C (1/2)

Start Address	End Address	Area	Availability of Area √: Available, —: Not available				Access from(*4)		
			U2C8-EVA	U2C8	U2C4	U2C2	CPU	DMA modules	H-Bus modules
0000 0000$_H$	000F FFFF$_H$	Code flash (User Area 0) (Bank A)	√	√	√	√			
0010 0000$_H$	001F FFFF$_H$		√	√	√	—			
0020 0000$_H$	002F FFFF$_H$		√	√	—	—			
0030 0000$_H$	003F FFFF$_H$		√	√	—	—			
0040 0000$_H$	004F FFFF$_H$	Code flash (User Area 1) (Bank B)	√	√	√	√			
0050 0000$_H$	005F FFFF$_H$		√	√	√	—			
0060 0000$_H$	006F FFFF$_H$		√	√	—	—			
0070 0000$_H$	007F FFFF$_H$		√	√	—	—			
0080 0000$_H$	03FF FFFF$_H$	Reserved	—	—	—	—			
0400 0000$_H$	07FF FFFF$_H$	Code flash (Non-overlay area)*1	√	√	√	√			
0800 0000$_H$	0800 FFFF$_H$	Code flash (User Boot Area 0) (Bank A)	√	√	√	√			
0801 0000$_H$	0802 FFFF$_H$	Reserved	—	—	—	—			
0803 0000$_H$	0803 7FFF$_H$	Code flash (Product Info Area 0) (Bank A)	√	√	√	√			
0803 8000$_H$	0804 FFFF$_H$	Reserved	—	—	—	—			
0805 0000$_H$	0805 FFFF$_H$	Code flash (ECC Test Area of Bank A)	√	√	√	√			
0806 0000$_H$	083F FFFF$_H$	Reserved	—	—	—	—			
0840 0000$_H$	0840 FFFF$_H$	Code flash (User Boot Area 1) (Bank B)	√	√	√	√			
0841 0000$_H$	0842 FFFF$_H$	Reserved	—	—	—	—			
0843 0000$_H$	0843 7FFF$_H$	Code flash (Product Info Area 1) (Bank B)	√	√	√	√			
0843 8000$_H$	0844 FFFF$_H$	Reserved	—	—	—	—			
0845 0000$_H$	0845 FFFF$_H$	Code flash (ECC Test Area of Bank B)	√	√	√	√			
0846 0000$_H$	0BFE FFFF$_H$	Reserved	—	—	—	—			
0BFF 0000$_H$	0BFF FFFF$_H$	Code flash (ECC Test Area of Global Area)	√	√	√	√			
0C00 0000$_H$	0FFF FFFF$_H$	Code flash (Blank Check Area)*2	√	√	√	√			
1000 0000$_H$	3FFF FFFF$_H$	H-Bus area	√	√	√	√			*3
(1200 0000$_H$	1200 7FFF$_H$	Retention RAM)	√	√	√	√			
4000 0000$_H$	F900 FFFF$_H$	Reserved	—	—	—	—			
F901 0000$_H$	F901 FFFF$_H$	Debug (CPU0)	√	√	√	√			
F902 0000$_H$	F902 FFFF$_H$	Debug (CPU1)	√	√	√	—			
F903 0000$_H$	F97F FFFF$_H$	Reserved	—	—	—	—			
F980 0000$_H$	F980 FFFF$_H$	AIU	—	—	—	—			
F981 0000$_H$	F9FF FFFF$_H$	Reserved	—	—	—	—			
FA00 0000$_H$	FA01 7FFF$_H$	Reserved	—	—	—	—			
FA01 8000$_H$	FA0F FFFF$_H$	Reserved	—	—	—	—			
FA10 0000$_H$	FA10 9BFF$_H$	Trace filter RAM (Cluster RAM) (Cluster 0)	√	—	—	—			
FA10 9C00$_H$	FA1C FFFF$_H$	Reserved	—	—	—	—			
FA1D 0000$_H$	FA1D 0FFF$_H$	Trace filter RAM (Local RAM) (CPU1)	√	—	—	—			
FA1D 1000$_H$	FA1D FFFF$_H$	Reserved	—	—	—	—			
FA1E 0000$_H$	FA1E 0FFF$_H$	Trace filter RAM (Local RAM) (CPU0)	√	—	—	—			
FA1E 1000$_H$	FD9F FFFF$_H$	Reserved	—	—	—	—			
FDA0 0000$_H$	FDA1 FFFF$_H$	Local RAM (CPU1)	√	√	√	—			
FDA2 0000$_H$	FDBF FFFF$_H$	Reserved	—	—	—	—			
FDC0 0000$_H$	FDC1 FFFF$_H$	Local RAM (CPU0)	√	√	√	√			
FDC2 0000$_H$	FDDF FFFF$_H$	Reserved	—	—	—	—			
FDE0 0000$_H$	FDE1 FFFF$_H$	Local RAM (self)	√	√	√	√			
FDE2 0000$_H$	FDFF FFFF$_H$	Reserved	—	—	—	—			

Table 5.2 Address space (Single Map Mode) - U2C (2/2)

Start Address	End Address	Area	Availability of Area √: Available, —: Not available				Access from(*4)		
			U2C8-EVA	U2C8	U2C4	U2C2	CPU	DMA modules	H-Bus modules
FE00 0000$_H$	FE02 7FFF$_H$	Cluster RAM (Cluster 0)	√*5	√*5	√	√			
FE02 8000$_H$	FE06 FFFF$_H$		√*5	√*5	√	—			
FE07 0000$_H$	FE13 7FFF$_H$		√*5	√*5	—	—			
FE13 8000$_H$	FEFF FFFF$_H$	Reserved	—	—	—	—			
FF00 0000$_H$	FFFB 7FFF$_H$	P-Bus area	√	√	√	√			
(FF20 0000$_H$	FF28 FFFF$_H$	Data Flash (Data Area))	√	√	√	√			
(FF32 0000$_H$	FF37 4FFF$_H$	Data Flash (Hardware Property Area))	√	√	√	√			
(FF40 0000$_H$	FF48 FFFF$_H$	Data Flash (Blank Check Area))	√	√	√	√			
FFFB 8000$_H$	FFFB FFFF$_H$	I-Bus area	√	√	√	√			
FFFC 0000$_H$	FFFC 3FFF$_H$	CPU peripheral (self)	√	√	√	√			
FFFC 4000$_H$	FFFC 7FFF$_H$	CPU peripheral (CPU0)	√	√	√	√			
FFFC 8000$_H$	FFFC BFFF$_H$	CPU peripheral (CPU1)	√	√	√	—			
FFFC C000$_H$	FFFF FFFF$_H$	Reserved	—	—	—	—			

Note: The following color coding is used in the map above.

: Fetch and data access available

: Data access available

: Access prohibited

Note 1. Non-overlay mirror area of 0000 0000$_H$ - 03FF FFFF$_H$

Note 2. Blank Check Area for 0000 0000$_H$ - 03FF FFFF$_H$ or 0800 0000$_H$ - 0BFF FFFF$_H$

Note 3. Only GTM can access H-Bus slave modules. For other H-Bus master, this area poses as reserved area.

Note 4. For ICUMHB and AES Engine, see the *RH850/U2C Group Security User's Manual: Hardware*.

Note 5. Cluster RAM (Cluster 0) is divided into 3 areas (CRAM Controllers):

FE00 0000H - FE07 FFFFH: Cluster 0 RAM0 (CRAM00)

FE08 0000H - FE0F FFFFH: Cluster 0 RAM1 (CRAM01)

FE10 0000H - FE13 7FFFH: Cluster 0 RAM2 (CRAM02)

Table 5.3 Address Space (Double Map Mode) – U2C

Start Address	End Address	Area	Availability of Area √: Available, —: Not available			Access from(*3)		
			U2C8-EVA U2C8	U2C4	U2C2	CPU	DMA modules	H-Bus modules
0000 0000$_H$	000F FFFF$_H$	Code flash (User Area Valid Area) (Bank A or B)	√	√	√			
0010 0000$_H$	001F FFFF$_H$		√	√	—			
0020 0000$_H$	002F FFFF$_H$		√	—	—			
0030 0000$_H$	003F FFFF$_H$		√	—	—			
0040 0000$_H$	01FF FFFF$_H$	Reserved	—	—	—			
0200 0000$_H$	020F FFFF$_H$	Code flash (User Area Invalid Area) (Bank B or A)	√	√	√			
0210 0000$_H$	021F FFFF$_H$		√	√	—			
0220 0000$_H$	022F FFFF$_H$		√	—	—			
0230 0000$_H$	023F FFFF$_H$		√	—	—			
0240 0000$_H$	03FF FFFF$_H$	Reserved	—	—	—			
0400 0000$_H$	07FF FFFF$_H$	Code flash (Non-overlay area)(*1)	√	√	√			
0800 0000$_H$	0800 FFFF$_H$	Code flash (User Boot Area Valid Area) (Bank A or B)	√	√	√			
0801 0000$_H$	0802 FFFF$_H$	Reserved	—	—	—			
0803 0000$_H$	0803 7FFF$_H$	Code flash (Product Info Area Valid Area) (Bank A or B)	√	√	√			
0803 8000$_H$	0804 FFFF$_H$	Reserved	—	—	—			
0805 0000$_H$	0805 FFFF$_H$	Code flash (ECC Test Area of Bank A or B)	√	√	√			
0806 0000$_H$	09FF FFFF$_H$	Reserved	—	—	—			
0A00 0000$_H$	0A00 FFFF$_H$	Code flash (User Boot Area Invalid Area) (Bank B or A)	√	√	√			
0A01 0000$_H$	0A02 FFFF$_H$	Reserved	—	—	—			
0A03 0000$_H$	0A03 7FFF$_H$	Code flash (Product Info Area Invalid Area) (Bank B or A)	√	√	√			
0A03 8000$_H$	0A04 FFFF$_H$	Reserved	—	—	—			
0A05 0000$_H$	0A05 FFFF$_H$	Code flash (ECC Test Area of Bank B or A)	√	√	√			
0A06 0000$_H$	0BFE FFFF$_H$	Reserved	—	—	—			
0BFF 0000$_H$	0BFF FFFF$_H$	Code flash (ECC Test Area of Global Area)	√	√	√			
0C00 0000$_H$	0FFF FFFF$_H$	Code flash (Blank Check Area)(*2)	√	√	√			
1000 0000$_H$	FFFF FFFF$_H$	This address area does not change even in double map mode. See **Table 4.1, Address Space (Single Map Mode)**.						

Note: The following color coding is used in the map above.

: Fetch and data access available

: Data access available

: Access prohibited

Note 1. Non-overlay mirror area of 0000 0000$_H$ - 03FF FFFF$_H$

Note 2. Blank Check Area for 0000 0000$_H$ - 03FF FFFF$_H$ or 0800 0000$_H$ - 0BFF FFFF$_H$

Note 3. For ICUMHB and AES Engine, see the *RH850/U2C Group Security User's Manual: Hardware*.

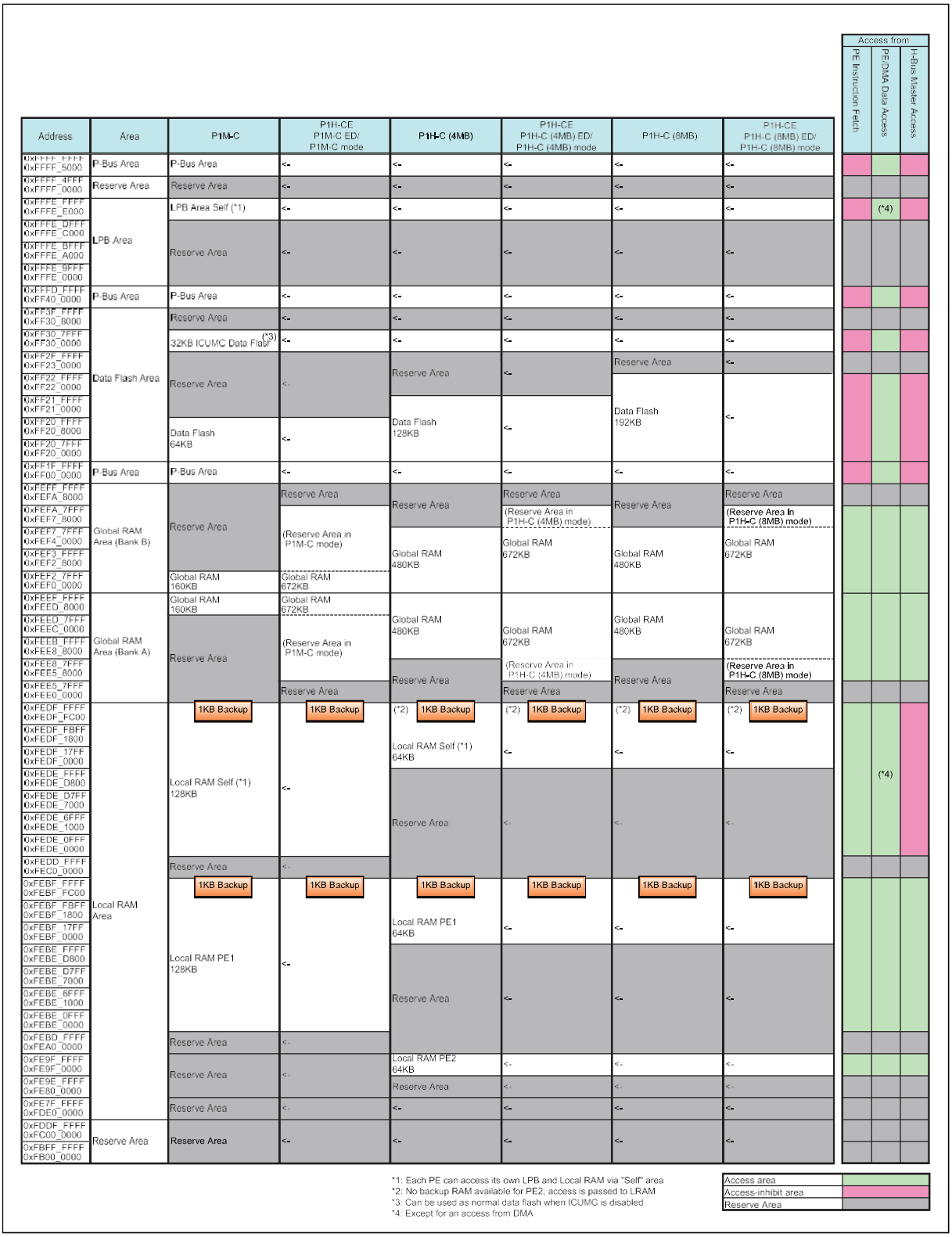


Figure 5.1 Address map – P1x-C (1/2)

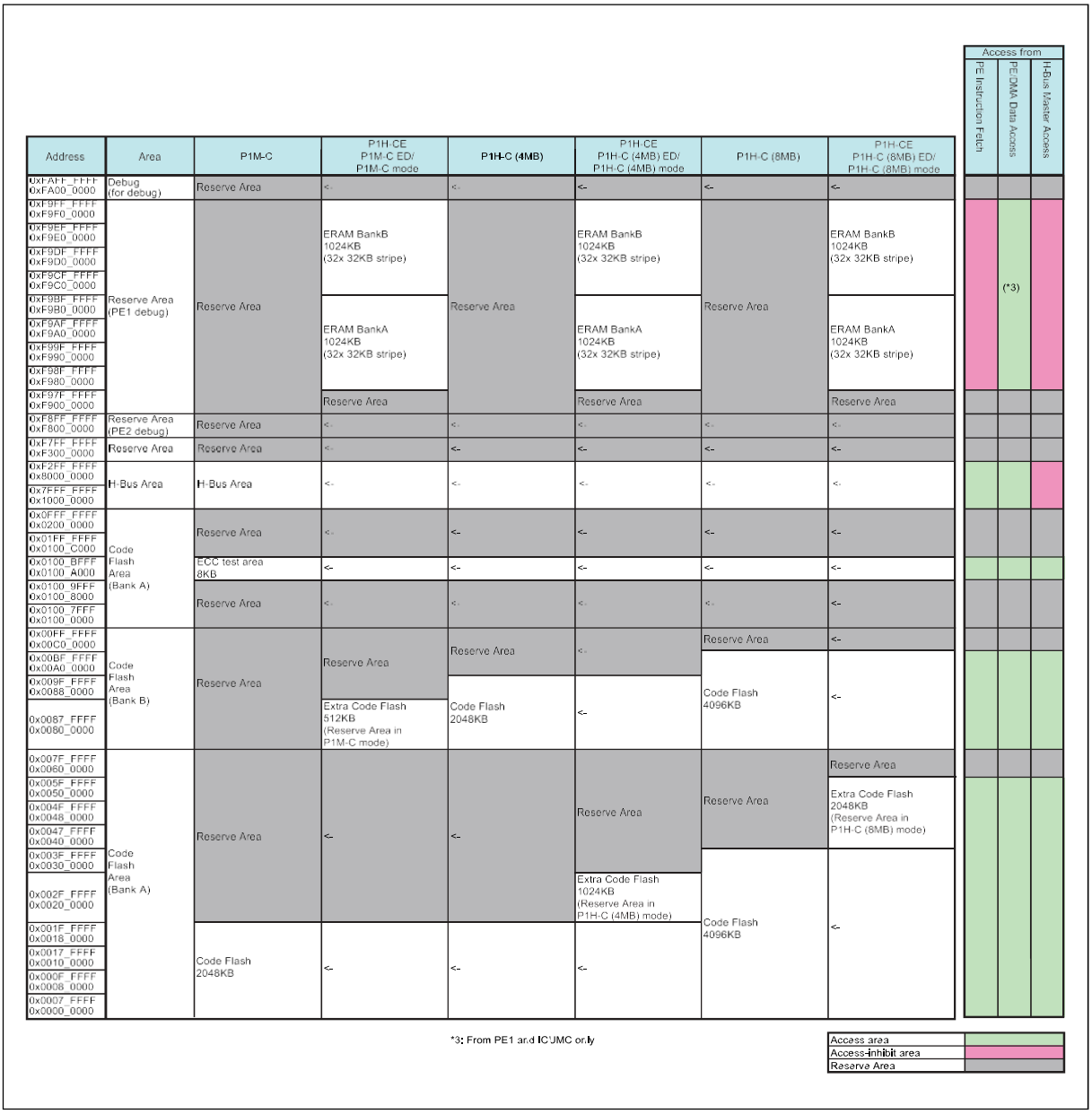


Figure 5.1 Address map – P1x-C (2/2)

6. Operating Mode

6.1 General features

Both the RH850/U2C and RH850/P1x-C microcontrollers offer primary operation modes that include Normal Operating Mode and Serial Programming Mode.

6.2 Operating mode in RH850/U2C

The RH850/U2C has multiple operating modes, which can be selected with the three pins (FLMD0, FLMD1, and TRST) and the setting of STMSEL1, STMSEL0 in option byte. For details of STMSEL1, STMSEL0, see RH850/U2C Group User's Manual: Hardware **Section 53, Flash Memory**. **Table 6.1, Selection of Operating Mode in RH850/U2C** shows the list of the operating modes.

The values of FLMD0, FLMD1, and TRST are latched at the rising edge of POC Reset (Only in the case the FLMD0 is “Low” level) and RESET to determine the operating mode, and part of the values of these pins should be kept during RESET = 1 except that the value of FLMD0 can be changed for selecting Flash Programming Interface in the Serial Programming Mode, for details of which pin should be kept please refer to the **Table 6.1 Selection of Operating Mode in RH850/U2C.** These pins are continually monitored during operation to detect mode errors.

Table 6.1 Selection of Operating Mode in RH850/U2C

Pins			OPBT		Operating Mode	Startup Area	Types of Debug Interface*1*6	Flash Programming Interface
FLMD0	FLMD1	$\overline{\text{TRST}}$	STM SEL1	STM SEL0				
0	x	0	0	0	Normal Operating Mode	User Area*2	NEXUS/LPD	—
0	x	0	0	1	User Boot Mode 0	User Boot Area*3	NEXUS/LPD	—
0	x	0	1	x	Serial Programming Mode 0	Boot firmware	—	CSI
0	x	1*5	x	0	Normal Operating Mode	User Area*2	NEXUS/LPD/ Boundary scan*7	—
0	x	1*5	x	1	User Boot Mode 0	User Boot Area*3	NEXUS/LPD/ Boundary scan*7	—
1	0	x	x	x	Serial Programming Mode 1	Boot firmware	—	2-wire UART, CSI*4

Note 1. For the correspondence between the pin function and pin state in each debug interface. See RH850/U2C Group User's Manual: Hardware **Section 2, Pin Functions**.

Note 2. Reset vector address can be set by option bytes. See RH850/U2C Group User's Manual: Hardware **Section 53, Flash Memory**.

Note 3. The reset vector address of CPU0 is fixed to 0800 0000H (head address in User Boot Area). The reset vector address of CPU 1 can be set by option bytes.

Note 4. For details of Flash Programming Interface is shown in RH850/U2C Group User's Manual: Hardware **Section 53, Flash Memory**. CSI is the “Clocked Serial Interface”.

Note 5. CPU does not run after releasing the reset depending on option byte(CPUBTMSK_EN) if $\overline{\text{TRST}}$=1 is latched at the rising edge of $\overline{\text{RESET}}$. This description is not applicable for the case $\overline{\text{RESET}}$ is pulled up because $\overline{\text{TRST}}$ must be 0 when POC reset is released. BIST is not executed during $\overline{\text{TRST}}$=1 or if $\overline{\text{TRST}}$=1 is latched at the rising edge of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$=1 cannot be latched in the case $\overline{\text{RESET}}$ is pulled up because $\overline{\text{TRST}}$ must be 0 when POC reset is released.

Note 6. Nexus/LPD for debug is determined by the TDI level when TRST is released. Nexus shall be selected when Boundary scan runs.

Note 7. Boundary scan can be run when the CPU and ICUM are not running. Boundary scan is selected by using JTAG instructions. TDI shall be set 1 when TRST is released for running Boundary scan.

6.3 Operating mode in RH850/P1x-C

The RH850/P1x-C supports 3 User modes. Operating modes are selected by the mode terminals FLMD0, FLMD1, MODE0 and MODE1. **Table 6.2 Selection of Operating Mode in RH850/P1x-C** shows the list of the operating modes. Device Mode decoding is only executed after Terminal reset.

Table 6.2 Selection of Operating Mode in RH850/P1x-C

	mode pin				
	FLMD0	**FLMD1**	**MODE0**	**MODE1**	**mode**
User mode	0	x	x	x	Normal Operation Mode
	1	0	x	x	Serial Flash Programming Mode (Following serial I/F are supported 3-wire Clocked serial Interface, 2-wire UART, 1-wire UART)
	1	1	0	1	Boundary SCAN Mode

7. Exception/Interrupts

7.1 General Features

Due to the difference in the CPU structure, the exception types are different in P1x-C and U2C devices.

Table 7.1 List of Exception Sources

RH850/U2C	Priority	RH850/P1x-C	Priority
RESET	1	RESET	1
Memory protection exception (access privilege) MDP*1	2	Memory protection exception (access right) MDP	15
FENMI interrupt	4	FE level non-maskable interrupt FENMI (NMI)	3
FEINT interrupt	4	FE level maskable interrupt FEINT (NMI)	5
System error SYSERR*2	4	System error exception SYSERR (NMI)	4
FPU exception (imprecise) FPI	5	FPU exception FPU (NMI)	6
User interrupt EIINT0-2047	5	EI level maskable interrupt INT	7
Memory protection exception (execution privilege) MIP	7	Memory protection violation (execution right) MIP	9
System error SYSERR*3	7	System error exception SYSERR	10
Coprocessor unusable exception UCPOP	7	Coprocessor unusable exception UCPOP	12
Reserved instruction exception RIE	7	Reserved instruction exception RIE	11
Privilege instruction exception PIE	7	Privileged instruction exception PIE	13
System error SYSERR*4	7	-	-
Misalignment exception MAE	8	Misalign exception MAE	14
Memory protection exception (access privilege) MDP	8	Memory protection exception (access right) MDP	15
FPU exception (precise) FPE	8	FPU exception (precise) FPP	17
FXU exception (precise) FXE	8	-	-
System call SYSCALL	9	System call SYSCALL	19
FE level trap FETRAP	9	FE level trap FETRAP	20
EI level trap 0 TRAP0	9	EI level trap 0 EITRAP0	21
EI level trap 1 TRAP1	9	EI level trap 1 EITRAP1	22
-	-	Debug exception (asynchronous) (NMI)	2
-	-	Debug exception (synchronous) SyncDB	8
-	-	Debug trap DBTRAP	16
-	-	Runtime monitor trap RMTRAP	18

Note 1. The case in which an MDP exception occurs during the processing (table read or automatic context saving onto the register bank) which is performed after a table reference method interrupt (EIINTn) is selected as the result of priority determination. The occurrence of this type of exceptions takes precedence over that of the terminating-type exceptions except the reset.

Note 2. Error due to context saving to the register bank

Note 3. Error due to instruction fetching

Note 4. Error prior to context restoration from the register bank

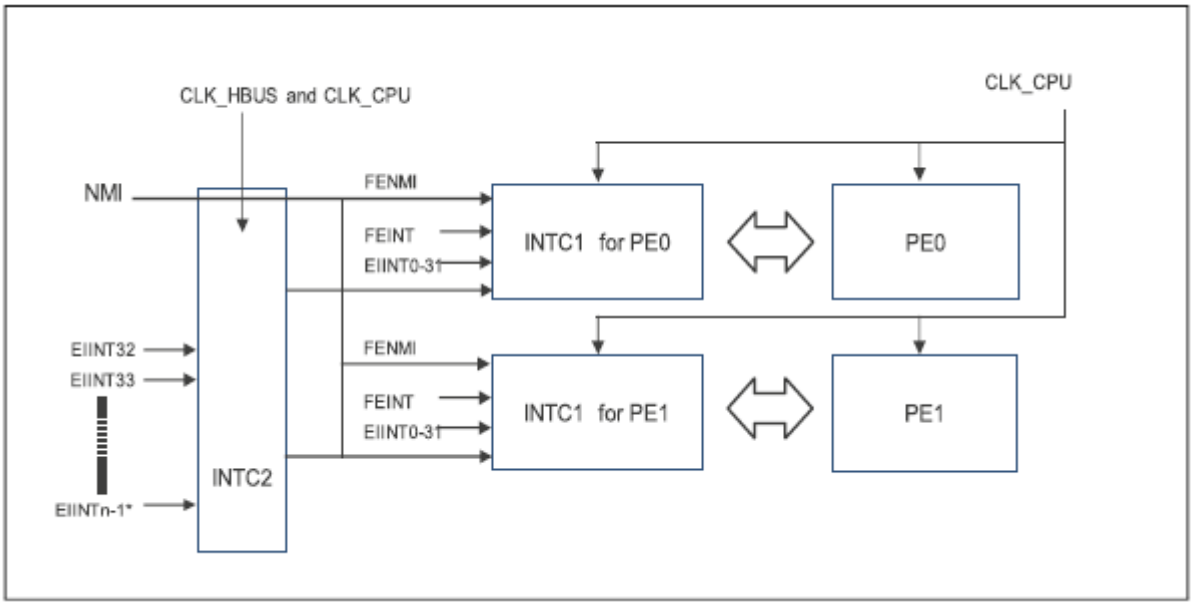


Figure 7.1 Block Diagram of the Interrupt Unit - U2C

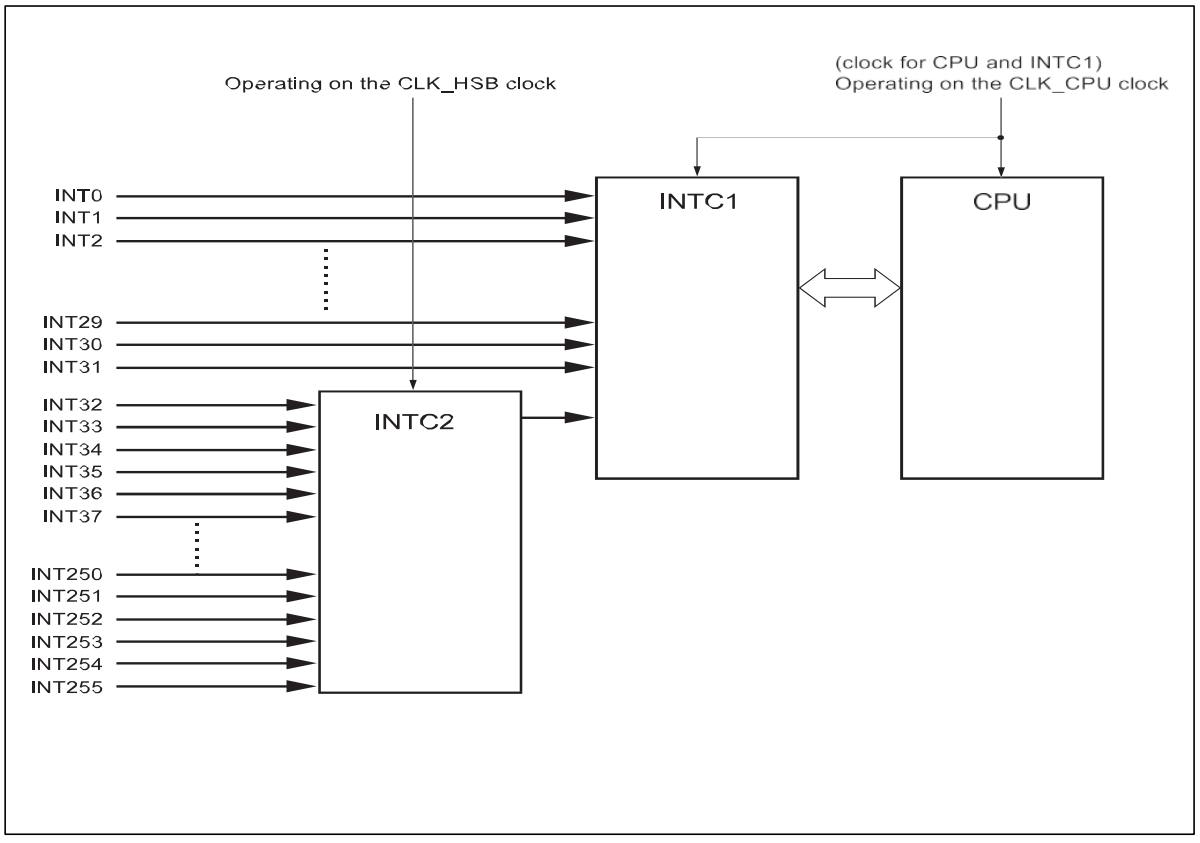


Figure 7.2 Configuration Diagram of EI-level Maskable Interrupt - P1x-C

Note: For more details refer to **RH850/P1x-C Group User's Manual: Hardware** or **RH850/U2C Group User's Manual: Hardware**

8. RESET Controller

8.1 General Features

The RH850/U2C integrates a Standby Controller (STBC). As a result, low-power mode reset functionality is available on this device.

Table 8.1 Reset comparisons between the RH850/U2C and RH850/P1x-C

Reset Category in U2C	Reset Source in U2C	Reset Category in P1x-C	Reset Source in P1x-C
Power On Reset	POC Reset (POCRES) Debugger Reset (by a debugger)	Power On Reset	Power On Reset
System Reset 1	External Reset Primary VMON Reset Debugger Disconnection Reset	System Reset 1	Terminal Reset CVM Reset Debugger Disconnect Reset
System Reset 2	Software System Reset (by SWSRESA, SWSRESA_ICUM)	System Reset 2	Software Reset (by SWSRESA0, SWSRESA1) ECM Reset (if RESC0 = 0)
Application Reset	Software Application Reset (by SWARESA, SWARESA_ICUM)	Application Reset 1	Software Reset (by SWARESA0, SWARESA1) ECM Reset (if RESC0 = 1)
DeepSTOP Reset	DeepSTOP Reset (by DeepSTOP mode trigger)	Limited Reset	Software Reset (by SWLRESAn) ICUMC WDTA Reset
Module Reset	Software Module Reset (by SWMRESA_<name>)	Debug Reset	Debug Reset (by TRSTZ)
JTAG Reset	JTAG Reset (by TRST)	-	-

Besides, there are also implementation differences in terms of:

- Clock supply
- Register base address
- External and internal I/O signals

8.2 Clock Supply

Table 8.2 shows the supplied clock on the RH850/U2C and RH850/P1x-C devices.

Table 8.2 Clock Supply for the Reset Controller on U2C and P1x-C Devices

Unit Name		RH850/U2C	RH850/P1x-C
Reset	Register_access_clock	CLK_LSB	CLK_LSB

8.3 Register Base Address

The base addresses are different. The table 8.3 below provides the Base address details.

Table 8.3 Register Base Addresses of the RH850/U2C and RH850/P1x-C Devices

Reset Controller Base Address RH850/U2C		**Reset Controller** Base Address RH850/P1x-C	
STAC_DPRAM	FF98 0800h	RESF	FFF8 1000h

8.4 External and Internal I/O Signals

Table 8.4 shows pins related to reset are shown on the RH850/U2C and RH850/P1x-C devices.

Table 8.4 I/O pins related to reset are shown in U2C and P1x-C devices

Description	**Pin function Name**	
	RH850/U2C	**RH850/P1x-C**
Reset Input	$\overline{\text{RESET}}$	RESETZ
Debug Reset Input	$\overline{\text{TRST}}$	TRSTZ
Reset Output	$\overline{\text{RESETOUT}}$	RESETOUTZ

8.5 Peripheral Configuration

This section lists the differences by peripheral configuration.

Table 8.5 Differences in the reset control registers of the U2C and P1x-C devices

Register description	**RH850/U2C**	**RH850/U2C Address**	**RH850/P1x-C**	**RH850/P1x-C Address**
Reset Factor Register	RESF	FF98 8500h	RESF	FFF8 1000h
Reset Factor Clear Register	RESFC	FF98 0C00h	RESFC	FFF8 1008h
Reset Configuration Register	-	-	RESC	FFF8 2800h
Boot Control Register	BOOTCTRL	FFFB 2000h	BOOTCTRL	FFC5 8000h
ICUMC Reset Factor Register	-	-	ICUMRESF	FFF8 6300h
ICUMC Reset Factor Clear Register	-	-	ICUMRESFC	FFF8 6308h
Reset Factor Clear Register for Debugger Disconnection Reset	RESFDDC	FF98 0C10h	-	-
Reset Controller Register Key Code Protection Register 0	RESKCPROT0	FF98 0F00h	-	-
Reset Factor Register for Debugger Disconnection Reset	RESFDD	FF98 8510h	-	-

9. Power Supply Circuit

9.1 General Features

Both RH850/U2C and RH850/P1x-C microcontrollers implement dual power supply, but only RH850/U2C microcontrollers implement dual power domain architecture, consisting of Always-On (AWO) and Isolated (ISO) domains. This strategy allows for optimized power consumption and supports low-power modes. The AWO domain is always powered, while the ISO domain can be shut down in standby mode. Additionally, both microcontrollers feature on-chip voltage regulators that supply power to the AWO and ISO domains

The power-on clear (POC) function is integrated into both microcontrollers to ensure safe startup. They also have separate analog power domains for analog-to-digital converters, with dedicated analog supplies. Furthermore, both microcontrollers have multiple I/O power supply pins (E0VCC, E1VCC for both RH850/U2C and RH850/P1x-C and E2VCC for RH850/U2C8 and RH850/U2C8-EVA) and common grounding (VSS for RH850/U2C and RH850/P1x-C and OSVSS for RH850/P1x-C).

The external supply input SYSVCC on RH850/U2C powers the system logic, regulators, and VCC for Flash. In contrast, RH850/P1x-C uses OSVCC to power on-chip oscillator and VDD for internal. Additionally, RH850/U2C has sub power domains like VDD, which can be powered off in DeepSTOP mode.

Table 9.1 shows the external pin list for power supply on both device series.

Table 9.1 External Pin List for Power Supply on RH850/U2C and RH850/P1x-C

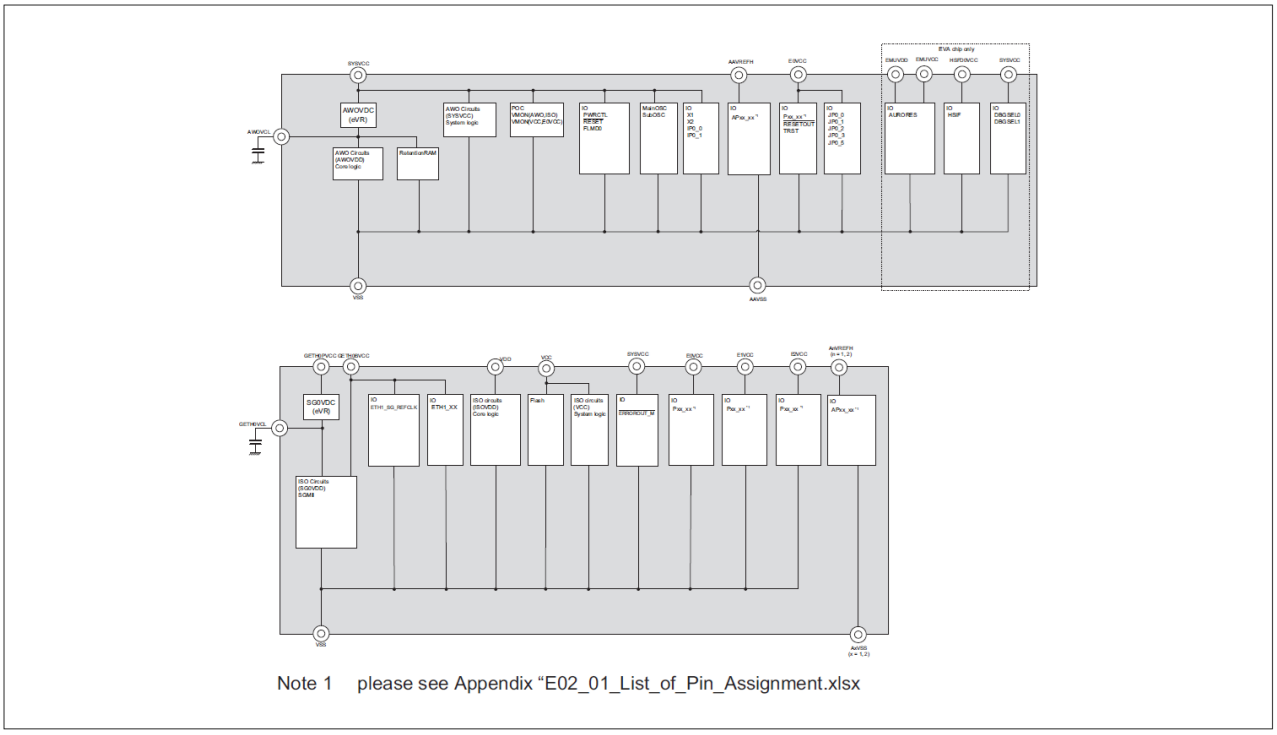
Power Supply	Power Supply Pins U2C	Power Supply for U2C	Power Supply Pins P1x-C	Power Supply for P1x-C
Power supply for internal circuits	SYSVCC	Power supply for System Logic and Internal voltage regulator power POC, VMON LS IntOSC, MainOSC, SubOSC Power supply terminal for Ports	SYSVCC	Power supply for IPs (CVM and OSC)
	VCC	Power supply for FLASH Power supply for Internal voltage regulator power*1*4	VCC	Internal voltage regulator power
	HSFD0VCC*3	RHSIF debug interface (RHSIFD)	VDD	Power supply for Internal
	ISOVCL*1*4	External buffer capacitance of regulator and resistance for ISOVDD	VSS	
	VSS	Common Ground	OSCVSS	Power supply for Oscillator
	AWOVCL	External buffer capacitance of regulator		
Power supply for I/O port	E0VCC	$\overline{\text{RESETOUT}}$ Port group Pxx_xx JP0x	E0VCC	I/O power supply
	E1VCC	Port group Pxx_xx	E1VCC	
	E2VCC*2	Port group Pxx_xx	E0VSS	
	VSS	Common Ground	E1VSS	
Power supply for A/D converters	A1VSS	Analog circuits of ADCK1, Port group AP2xx, AP3xx	A0VCC	Power supply for ADCF
	A1VREFH		A1VCC	
	A2VSS*2	Analog circuits of ADCK2, Port group AP4xx, AP5xx	A0VSS	
	A2VREFH*2		A1VSS	
	AAVSS	Analog circuits of ADCKA, Port group AP0xx, AP1xx	A0VREFH	Reference voltage for ADCF
	AAVREFH		A1VREFH	

Note 1. U2C4 only

Note 2. U2C8/U2C8-EVA only

Note 3. U2C8-EVA only

Note 4. U2C2 only



Note 1 please see Appendix “E02_01_List_of_Pin_Assignment.xlsx

Figure 9.1 Block diagram of Power Supply Circuit in U2C8/U2C8-EVA

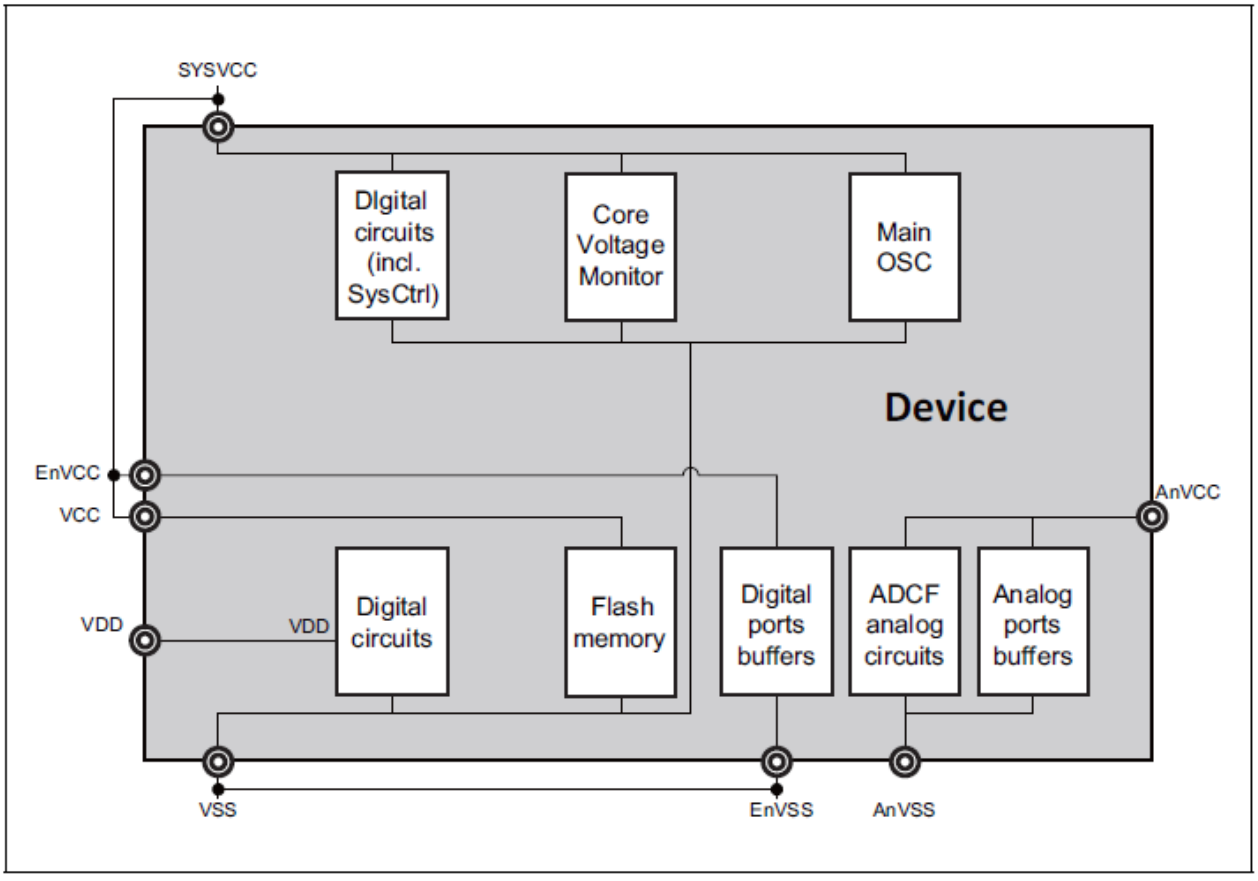


Figure 9.2 Block diagram of Power Supply Circuit in P1H-C and P1H-CE (Dual power supply)

10. Clock Controller

10.1 General Features

Table 10.1 lists the general differences of the clock controller of the RH850/U2C and RH850/P1x-C series.

Table 10.1: Differences of Clock Generators and Outputs on RH850/U2C and RH850/P1x-C

Function	RH850/U2C	RH850/ P1x-C
Clock Generator	Main OSC	Main OSC
	Sub OSC	-
	HS IntOSC (200 MHz)	Internal oscillator (16 MHz)
	LS IntOSC	
	PLL	PLL
	SSCG	-
Clock output	EXTCLK	EXTCLK
Clock connection to peripherals	Support Module standby Mode	Not Available

RH850/U2C series includes dedicated clock connection control to certain peripherals to support Module Standby Mode.

Figure 10.1 and Figure 10.2 shows the block diagram of clock controller configuration individually for RH850/U2C and RH850/P1x-C devices. Please refer to section 11 Clock Monitor (CLMA) for details of clock monitors.

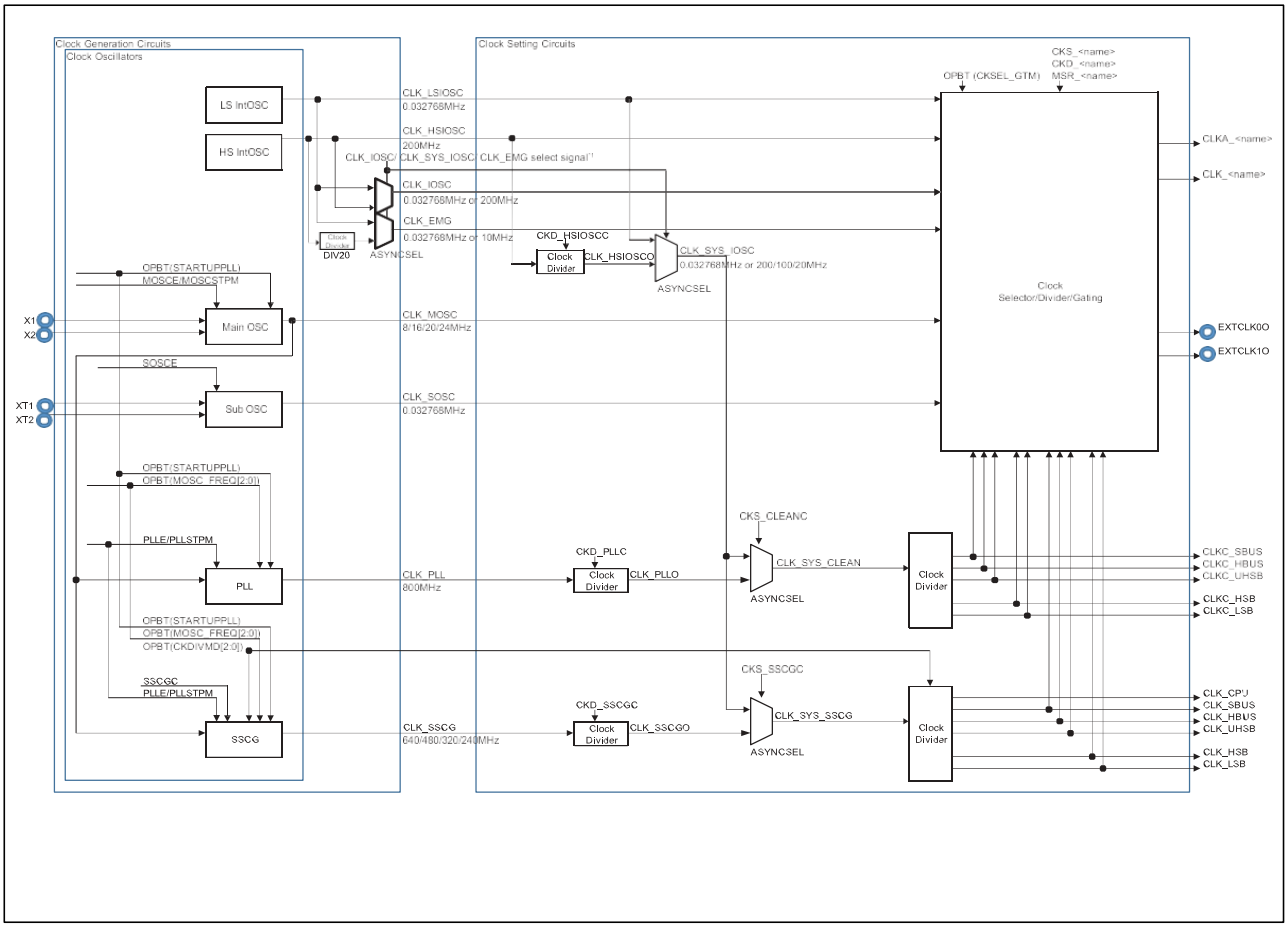


Figure 10.1 Block Diagram of the Clock controller configuration of RH850/U2C

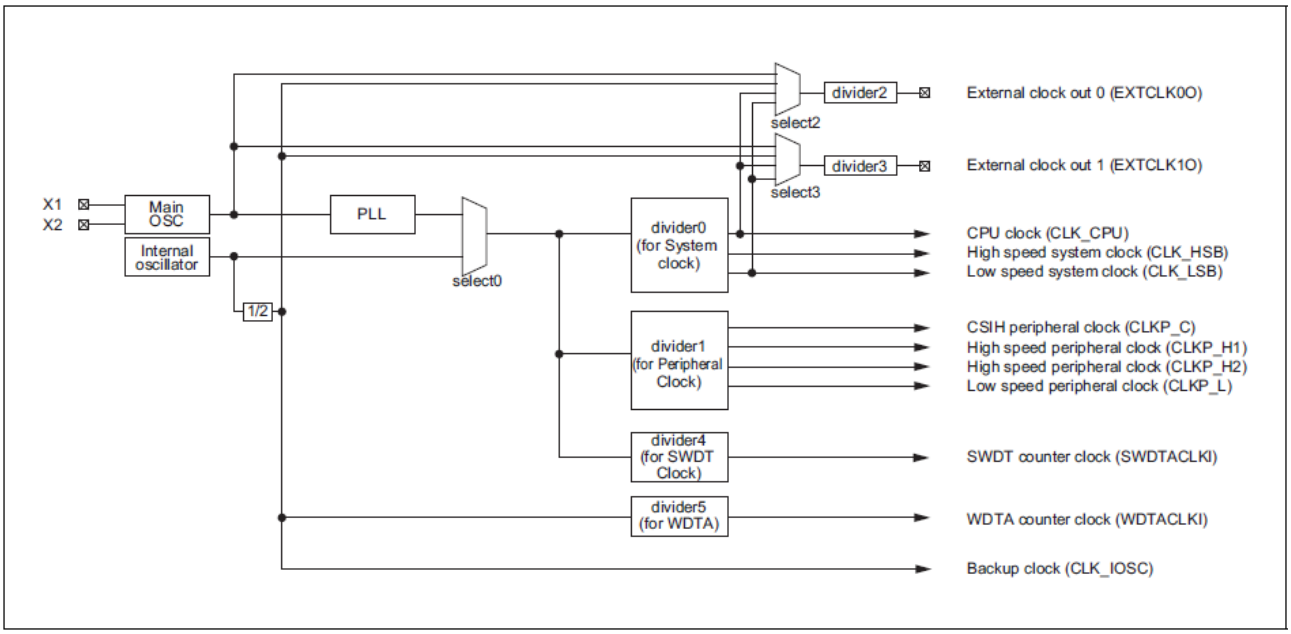


Figure 10.2 Clock diagram of the RH850/P1x-C

From the above figures, it is noticeable that the clock controller configuration of RH850/U2C and RH850/P1x-C are not identical. RH850/U2C has the clock oscillators separated in 3 locations: HS IntOSC, Main OSC and Sub OSC are located in Always-On area (AWO Area), LS IntOSC is located in the SYSVCC area, PLL and SSCG are located in the Isolated area (ISO area). Meanwhile RH850/P1x-C has the internal oscillator that starts at power-up, Main OSC and PLL clocks all on the same Power Domain.

11. Clock Monitor (CLMA)

Clock monitor CLMA detects frequency abnormalities in the monitored clock. It uses sampling clock CLMATSMP to monitor whether the frequency of input clock CLMATMON is within a specific range. Both RH850/U2C and RH850/P1x-C have similar CLMA units with similar functionalities.

11.1 General Features

Clock Monitor CLMA detects frequency abnormalities in the monitored clock for RH850/U2C and RH850/P1x-C and transmits an error notification to the ECM. The thresholds for an error to be announced will be described below.

For RH850/P1x-C microcontroller the minimum and maximum threshold were calculated based on formulas:

- Lower threshold = N_{min}

$$= \frac{\mathrm{fCLMATMON}}{\mathrm{fCLMATSMP}} \times 16 - 1$$

- Upper threshold = N_{max}

$$= \frac{\mathrm{fCLMATMON}}{\mathrm{fCLMATSMP}} \times 16 + 1$$

The thresholds for RH850/U2C are described in Table 11.1 Accuracy of clock frequency used by Clock Monitor of RH850/U2C.

Table 11.1 Accuracy of clock frequency used by Clock Monitor of RH850/U2C

Channel Name	CLMATMON (monitored clock)	CLMATSMP (sampling clock)
CLMA0	±0.1% *1*4	±4.5%
CLMA1	CLK_WDTB: ±4.5%	CLK_LSIOSC: ±10%
	CLK_HSIOSC: ±4.5%	CLK_MOSC: ±0.1%*4
CLMA2	±10%	±4.5%
CLMA3	±0.1% *1*4*5	±0% *3
CLMA4	±0.1% *1 *2	±0% *3
CLMA5	±0.1% *1*4	±0% *3
CLMA6	±0.1% *1*4*5	±0.1% *1
CLMA7	±0.1% *1*4*5	±0.1% *1
CLMA8	±0.1% *1*4	±0% *3

Note 1. Depends on the accuracy of the external parts and PLL output clock.

Note 2. This is the value of “CLK_LSB = CLK_IOSC”.

Note 3. As the corresponding monitor clock and sampling clock are shared with the same clock source. The accuracy is set to be ±0%.

Note 4. In case of using ceramic resonator, frequency accuracy is ±1.0%.

Note 5. When SSCG modulation is disabled. ±0.1%
When SSCG modulation is enabled. +0.1%~-0.1% - "the maximum value of Frequency dithering range"
As for the modulation, refer to Section 13, Clock Controller 13.5.4.4 SSCGC.SELMPERCENT[2:0]

11.2 Unit and Channel Numbers

The RH850/U2C and RH850/P1x-C microcontrollers incorporate CLMA with the following number of channels.

Table 11.2 Channel Numbers of RH850/U2C and RH850/P1x-C

Product Name	RH850/U2C8, RH850/U2C4	RH850/U2C2	RH850/P1M-C	RH850/P1H-C, RH850/P1H-CE
Number of Channels	9(n = 0 to 8)	8(n = 0 to 6, 8)	5(n = 0 to 4)	6(n = 0 to 5)
Name	CLMAn	CLMAn	CLMAn	CLMAn

Table 11.3 Support channel of CLMA6, 7 of RH850/U2C

Cluster	CPU (PEID)	RH850/U2C8-EVA, RH850/U2C8	RH850/U2C4	RH850/U2C2
		(2+2)	(2+2)	(1+1)
0	0	CLMA6	CLMA6	CLMA6
	1	CLMA7	CLMA7	-

11.3 Clock Supply

Table 11.4 Clock supply for RH850/U2C and RH850/P1x-C

Channel Name	U2C			P1x-C		
	CLMATMON (monitored clock)	CLMATSMP (sampling clock)	PLCK (register access clock)	CLMATMON (monitored clock)	CLMATSMP (sampling clock)	PLCK (register access clock)
CLMA0	CLK_MOSC	CLK_HSIOSC/400	CLK_LSB	Main OSC	CLK_IOSC/2	CLK_LSB
CLMA1	CLK_WDTB/2 CLK_HSIOSC/20	CLK_LSIOSC CLK_MOSC / 32	CLK_LSB	CLKP_L (to OTS0)	Main OSC/4	CLK_LSB
CLMA2	CLK_LSIOSC	CLK_HSIOSC/6400	CLK_LSB	WDTACLKI	Main OSC/256	CLK_LSB
CLMA3	CLK_LSB	CLK_MOSC/32	CLK_LSB	CLK_CPU (PE1)/2	Main OSC/4	CLK_LSB
CLMA4	CLK_LSB	CLK_HSIOSC/20	CLK_LSB	CLK_CPU (PE2)/2	Main OSC/4	CLK_LSB
CLMA5	CLKC_SBUS/2 CLKC_UHSB/2	CLKC_LSB/8 (CLEAN)	CLK_LSB	CLK_HSB (to ICUMC)	Main OSC/4	CLK_LSB
CLMA6	CLK_CPU	CLKC_LSB/8 (CLEAN)	CLK_LSB	-	-	-
CLMA7	CLK_CPU	CLKC_LSB/8 (CLEAN)	CLK_LSB	-	-	-
CLMA8	CLKC_LSB (CLEAN)	CLK_MOSC/32	CLK_LSB	-	-	-

11.4 Register Base Address

Table 11.5 Register Base Address of RH850/U2C and RH850/P1x-C

Base Address Name	U2C	P1x-C
CLMAC_base*1	FF98 9000_H	-
CLMA0_base	FF98 9100_H	FFF8 3100_H
CLMA1_base	FF98 9200_H	FFF8 3200_H
CLMA2_base	FF98 9300_H	FFF8 3300_H
CLMA3_base	FF98 1800_H	FFF8 3400_H
CLMA4_base	FF98 1900_H	FFF8 3500_H
CLMA5_base	FF98 $1A00_H$	FFF8 6800_H
CLMA6_base	FF98 $1B00_H$	-
CLMA7_base	FF98 $1C00_H$	-
CLMA8_base	FF98 $1D00_H$	-
CLMAT_base	-	FFF8 3000_H

Note 1. Common registers CLMATEST, CLMATESTS and CLMABCE.

12. Standby Controller (STBC)

12.1 General Features

The RH850/P1x-C offers two primary power-down modes for reducing current consumption: HALT mode and module standby mode. In contrast, the RH850/U2C microcontroller is equipped with a Standby Controller (STBC) that not only supports HALT and module standby modes, but also provides additional chip standby modes (STOP, DeepSTOP, and Cyclic RUN) along with advanced power domain separation (Always-On and Isolated areas) for more granular and flexible low-power operation.

Table 12.1 shows the details of these differences.

Table 12.1 Differences of Power-down Modes on RH850/U2C and RH850/P1x-C

Power-down modes	RH850/U2C	RH850/P1x-C
Chip standby mode	STOP mode*1	-
	DeepSTOP mode*2	-
	Cyclic RUN mode*3	-
Module Standby	Supported	Supported
HALT Mode	Supported	Supported

Note 1. STOP mode is a chip-level chip standby mode in which the clock supply to certain clocks can be stopped.

Note 2. DeepSTOP mode is a chip-level chip standby mode to reduce power consumption further than STOP mode. In addition to the clock supply stop, the power supply to the Isolated area is switched off.

Note 3. Cyclic RUN mode is a low-power operation mode in which limited modules can operate at low speed

RH850 P1x-C has only halt mode as power down mode for CPU. When the HALT instruction is executed, the CPU transits to HALT mode and stops instruction execution. Each CPU (PE1, PE2 and ICUMC) can be controlled individually. **Table 12.2** shows the modules that participate in HALT Mode. The CPU returns from this state by the occurrence of a reset input, interrupt, or exception.

Table 12.2 Modules that participate in HALT mode of P1x-C

Module	Status during HALT Mode
PE1	HALT/Run
PE2	HALT/Run
ICUMC	HALT/Run

RH850/U2C also has halt mode and when the HALT instruction is executed in RUN mode, the CPU transits to HALT mode and stops instruction execution. The CPU can enter “HALT” state by executing the “HALT” instruction to stop its operation in RUN mode. The CPU0(PE0) can issue the “HALT” instruction to enter HALT state in Cyclic RUN mode. Each CPU (PE0, PEn) can be controlled individually. The CPU returns from this state by the occurrence of all resets (except JTAG Reset), interrupt or exception.

12.2 Chip Standby Mode of U2C

The clock operations related to the standby modes are listed in Table 12.3

Table 12.3 Clock Operation in Chip Standby Mode

Power Domain	Clock	STOP	Deep STOP	Cyclic RUN
SYSVCC	CLK_LSIOSC	Operable	Operable	Operable
AWO	CLK_HSIOSC	Operable*1	Operable*1	Operable
AWO	CLK_MOSC	Operable*1	Operable*1	Operable
AWO	CLK_SOSC	Operable	Operable	Operable
AWO	CLK_EMG	Operable	Operable	Operable
AWO	CLK_IOSC	Operable	Operable	Operable
AWO	EXTCLK0O	Operable	Operable	Operable
AWO	EXTCLK1O	Operable	Operable	Operable
AWO	CLKA_LPS	Operable*2	Operable*2	Operable
ISO	CLK_SYS_IOSC	Operable	Inoperable	Operable
ISO	CLK_PLLO	Operable*1	Inoperable	Inoperable
ISO	CLK_SSCG	Operable*1	Inoperable	Inoperable
ISO	CLK_SYS_CLEAN	Operable	Inoperable	Operable
ISO	CLK_SYS_SSCG	Operable	Inoperable	Operable
ISO	CLK_CPU	Inoperable	Inoperable	Operable
ISO	CLK_SBUS	Inoperable	Inoperable	Operable
ISO	CLK_HBUS	Inoperable	Inoperable	Operable
ISO	CLK_UHSB	Operable	Inoperable	Operable
ISO	CLK_HSB	Operable	Inoperable	Operable
ISO	CLK_LSB	Operable	Inoperable	Operable
ISO	CLKC_SBUS	Operable	Inoperable	Operable
ISO	CLKC_HBUS	Operable	Inoperable	Operable
ISO	CLKC_UHSB	Operable	Inoperable	Operable
ISO	CLKC_HSB	Operable	Inoperable	Operable
ISO	CLKC_LSB	Operable	Inoperable	Operable

Note 1. When the Stop Mask Register is set to 1, the oscillator continues operation in chip standby mode.

Note 2. When CLK_HSIOSC stops in chip standby mode, CLKA_LPS is CLK_LSIOSC. In other cases, CLKA_LPS is CLK_HSIOSC / 20.

13. Digital Peripherals

13.1 Communication Interfaces

13.1.1 RLIN3/UART

13.1.1.1 General Features

The functional features of the RLIN3/UART in RH850/P1x-C series are the same as in RH850/U2C devices. However, there are implementation differences in terms of:

- Unit and channel numbers
- Clock connections
- Interrupt assignments
- Base address

Please refer to the related User manual chapters for details.

13.1.1.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

13.1.1.3 Clock Supply

Table 13.1 shows the supplied clock on the RH850/U2C and RH850/P1x-C devices.

Table 13.1 Clock Supply for the RLIN3/UART on RH850/U2C and RH850/P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
RLIN3n (n=0 to 18)*1	Bus clock	CLKC_HSB_RLIN3	CLK_HSB
	Communication clock	CLK_RLIN3	CLKP_L
RLIN3n (n= 23)	Bus clock	CLKC_HBUS_RLIN3_CH23	-
	Communication clock	CLK_RLIN3_CH23	-

Note 1. For P1x-C n = 0 to 3.

13.1.1.4 Register Base Address

Table 13.2 shows the register base addresses on the RH850/U2C and RH850/P1x-C devices.

Table 13.2 Register Base Addresses of the RLIN3/UART on RH850/U2C and RH850/P1x-C Devices[*1]

Base Address Name	RH850/U2C	RH850/P1x-C
<RLIN30_base>	FFC7 C000$_H$	FFD8 C000$_H$
<RLIN31_base>	FF89 B100$_H$	FFCA C000$_H$
<RLIN32_base>	FFC7 C200$_H$	FFD8 D000$_H$
<RLIN33_base>	FF89 B300$_H$	FFCA D000$_H$
<RLIN34_base>	FFC7 C400$_H$	-
<RLIN35_base>	FF89 B500$_H$	-
<RLIN36_base>	FFC7 C600$_H$	-
<RLIN37_base>	FF89 B700$_H$	-
<RLIN38_base>	FFC7 C800$_H$	-
<RLIN39_base>	FF89 B900$_H$	-
<RLIN310_base>	FFC7 CA00$_H$	-
<RLIN311_base>	FF89 BB00$_H$	-
<RLIN312_base>	FFC7 CC00$_H$	-
<RLIN313_base>	FF89 BD00$_H$	-
<RLIN314_base>	FFC7 CE00$_H$	-
<RLIN315_base>	FF89 BF00$_H$	-
<RLIN316_base>	FFC7 D000$_H$	-
<RLIN317_base>	FF89 C100$_H$	-
<RLIN318_base>	FFC7 D200$_H$	-
<RLIN323_base>	FF97 8000$_H$	-

Note 1. The base address in this table corresponds to the U2C and P1x-C devices. For smaller devices, the unit number may vary, but the base address for the specified unit remains the same.

13.1.2 Serial Peripheral Interface (SPI)

The RH850/U2C MSPI (Multichannel Serial Peripheral Interface) and the RH850/P1x-C CSIH (Clocked Serial Interface with FIFO) are both serial communication interfaces, but they have significant architectural and functional differences.

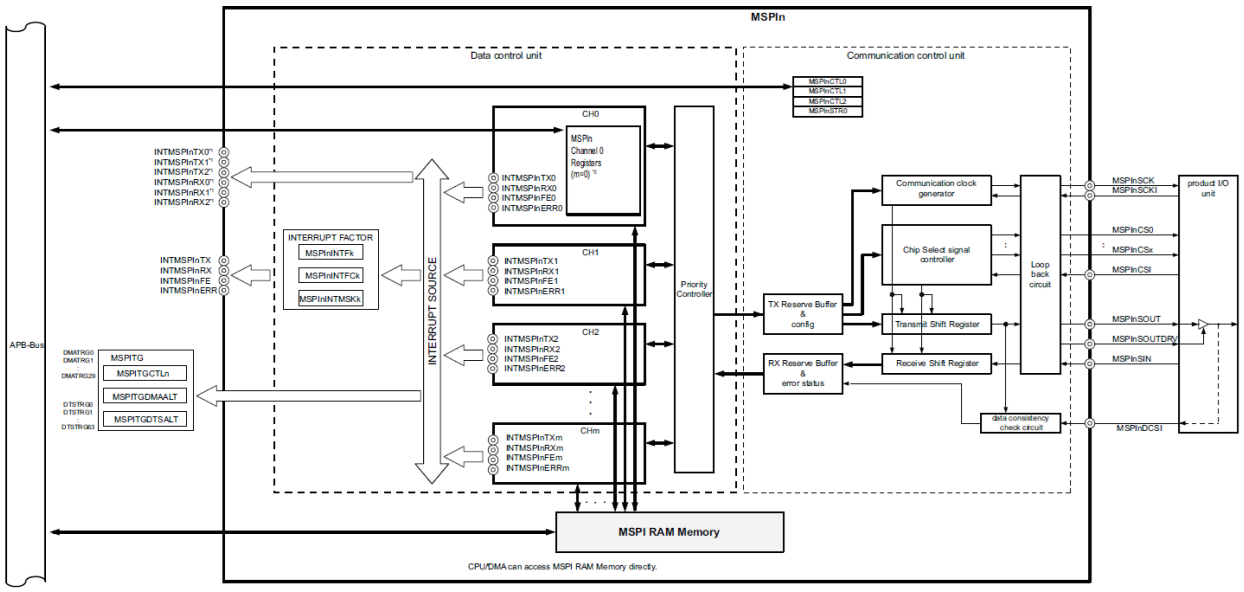
13.1.2.1 General Features

Table 13.3 Functional Overview comparison between RH850/U2C and RH850/P1x-C (1/2)

RH850/U2C	RH850/P1x-C
MSPI	**CSIH**
Full duplex operation	Three-wire serial synchronous data transfer
Support SPI signal: SCK, SIN, SOUT, CS0 to 7	Full duplex operation, receive only mode, or transmit only mode
Master mode and slave mode selectable	Master mode and slave mode selectable
Multiple slaves configuration thanks to up to twelve configurable chip select output signals	Phase of clock and data selectable for each chip select
Maximum transmission speed in master/slave mode: – In Single end mode: up to 20 MHz	Data transfer with MSB or LSB first selectable for each chip select
Clock polarity, clock / data phase: Phase of clock and data selectable for each channel	Transfer data length selectable from 2 to 16 bits in 1-bit units for each chip select
Frame Count: 65535 (2^16 – 1)	EDL (Extended Data Length) function for transferring data with more than 16 bits
Data transfer with MSB or LSB first selectable for each channel	Maximum transmission speed: – in master mode: 20 MHz – in slave mode: 20 MHz
Transfer control channel: Up to 8 for each unit	Bit rate selectable by BRG (baud rate generator) output (at Master mode) or by slave clock
Transfer data length selectable from 2 to 128 incremented in 1-bit units for channel	Transmit mode, Receive mode and Transmit/Receive mode selectable
Three selectable transfer modes: – Transmit-only mode – Receive-only mode – Transmit/receive mode	Buffer size is 128 words (1 word is data 32 bits + ECC 7 bits)
Error detection – Parity error – Data consistency error – Over-write error – Over-read error – Overrun error – CRC error	Memory mode selectable (FIFO, dual buffer, transmit-only buffer, and direct access)
Support of JOB concept for AUTOSAR	Built-in handshake function
JOB enable control bit for AUTOSAR is provided	Error detection (data consistency check, parity, time-out, overflow, and overrun)
LBM (Loop Back Mode) function for self-test	JOB enable control bit for AUTOSAR

Table 13.3 Functional Overview comparison between RH850/U2C and RH850/P1x-C (2/2)

RH850/U2C	RH850/P1x-C
MSPI	**CSIH**
Enforced chip select idle setting	RCB (Recessive Configuration for Broadcasting) bit for Broadcasting
Support Safe-SPI ver1.00 only in master mode	LBM (Loop Back Mode) function for self-test
Supports module standby for each unit	Four different interrupt request signals. (INTCSIHnTIC, INTCSIHnTIR, INTCSIHnTIRE, INTCSIHnTIJC)
MSPI has four different interrupt requests. Communication status – Reception status – Communication error – Job completion	IDLE State Control function.
MSPI has three DMA requests. – Communication status – Reception status – Job completion	Silent mode communication for extended idle time
Receive sample point – The sample point for the RX can be shifted to the next SCK edge	Automatically generation of chip select output signal with configurable active level
Channel Priority Control. – The priority level can be set independently for each channel. If the priority settings of several channels are the same, the lowest interrupt channel number has priority. – Channel lock function – Job Enable Function in the Direct Memory Mode	Data transfer without activated chip select
Communication Stop or IP Initialize. – Communication Stop by the Clear Trigger – IP initialize by the IP enable	Transmission speed for each chip select is selectable out of four predefined baud rates (in master mode) or by clock input signal from master (in slave mode)
Memory Modes – Direct Memory Mode – Fixed Buffer Memory Mode – Fixed FIFO memory Mode	Full DMA support for all CSIH registers (The SPI interface should be accessible by more than one bus-master without explicit SW-synchronization)



Note 1. These interrupts are only for MSPI0 and MSPI1. For more details, refer to **Figure 19.1, MSPI0-1 Interrupt Connection Image**.

Note 2. Refer to **Table 19.18, List of Channel m Registers**.

Figure 13.1 Block diagram of U2C MSPI

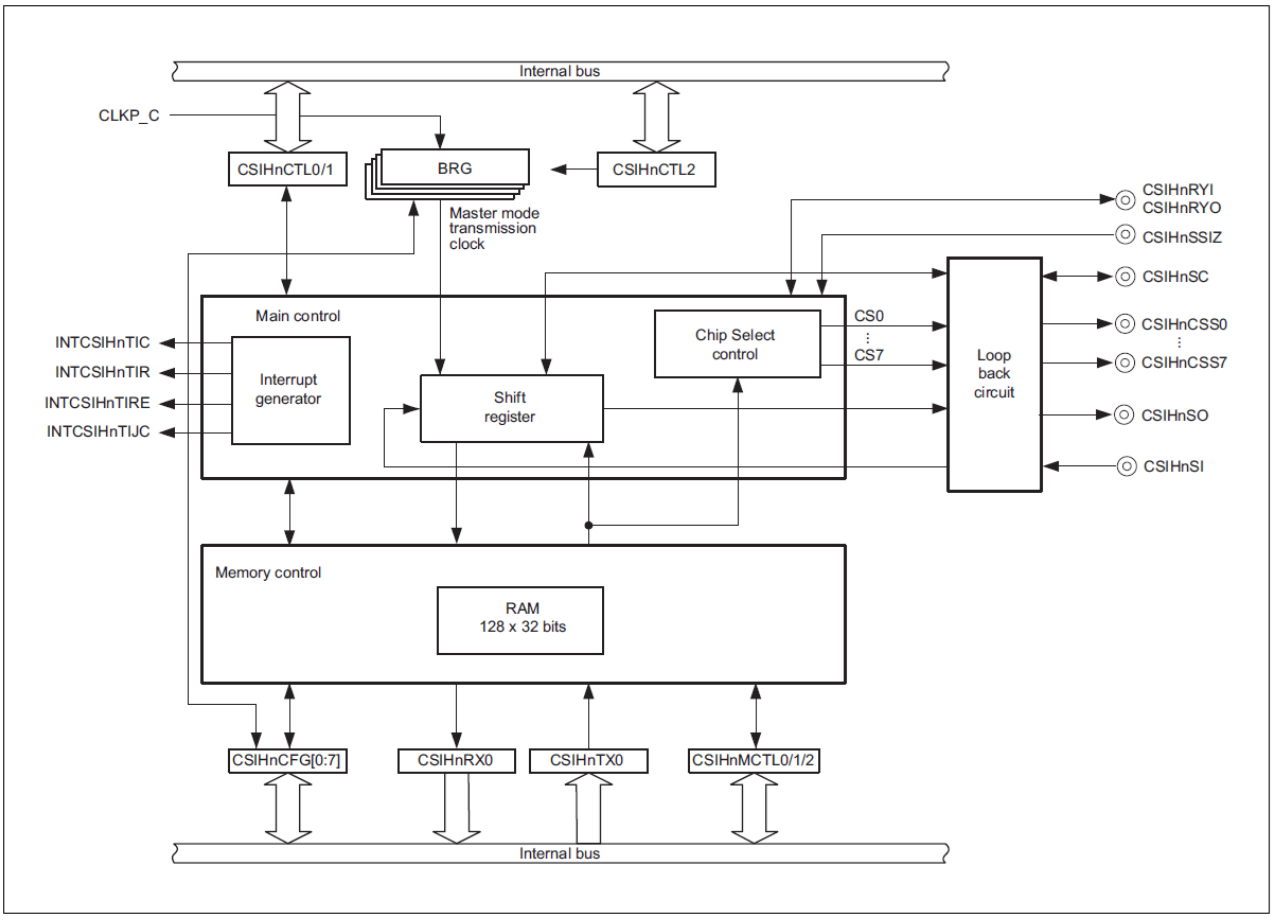


Figure 13.2 Block diagram of P1x-C CSIH

13.1.2.2 Unit and Channel Numbers

Table 13.4 shows the differences between unit and channel numbers on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.4 Unit and Channel of RH850/U2C and RH850/P1x-C

Product name	U2C8-EVA, U2C8	U2C4, U2C2(144 pins)	U2C2(100 pins)	P1x-C
Units	MSPIn(n = 0 to 9)	MSPIn(n = 0 to 7)	MSPIn(n = 0 to 5)	CSIHn (n = 0 to 3)
Channels	56	48	44	4

13.1.2.3 Clock Supply

Table 13.5 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.5. Clock Supply of RH850/U2C and RH850/P1x-C

Unit name	RH850/U2C unit clock	RH850/P1x-C unit clock
PCLK	CLK_HSB_MSPI	CLK_HSB
Communication Clock	CLK_MSPI	CLKP_C

13.1.2.4 Register Base Address

Table 13.6 shows the differences between the register base address on the RH850/U2C devices and the RH850/P1x-C devices.

Tabel 13.6 Register Base Address of RH850/U2C and RH850/P1x-C

RH850/U2C		RH850/P1x-C	
Base Address Name	**Base Address**	**Base Address Name**	**Base Address**
<MSPI0_base>	FFC7 6000$_H$	<CSIH0_base>	FFD8 0000$_H$
<MSPI1_base>	FFD5 E000$_H$	<CSIH1_base>	FFCA 0000$_H$
<MSPI2_base>	FFD8 0000$_H$	<CSIH2_base>	FFD8 3000$_H$
<MSPI3_base>	FFD6 0000$_H$	<CSIH3_base>	FFCA 3000$_H$
<MSPI4_base>	FFD8 2000$_H$	-	-
<MSPI5_base>	FFD6 2000$_H$	-	-
<MSPI6_base>	FFD8 4000$_H$	-	-
<MSPI7_base>	FFD6 4000$_H$	-	-
<MSPI8_base>	FFD8 6000$_H$	-	-
<MSPI9_base>	FFD6 6000$_H$	-	-
<MSPI0_INTF_base>	FFC7 5740$_H$	-	-
<MSPI1_INTF_base>	FFD6 8740$_H$	-	-
<MSPI2_INTF_base>	FFC7 5840$_H$	-	-
<MSPI3_INTF_base>	FFD6 8840$_H$	-	-
<MSPI4_INTF_base>	FFC7 5940$_H$	-	-
<MSPI5_INTF_base>	FFD6 8940$_H$	-	-
<MSPI6_INTF_base>	FFC7 5A40$_H$	-	-
<MSPI7_INTF_base>	FFD6 8A40$_H$	-	-
<MSPI8_INTF_base>	FFC7 5B40$_H$	-	-
<MSPI9_INTF_base>	FFD6 8B40$_H$	-	-
<MSPITG_base>	FFC7 5D00$_H$	-	-

13.1.3 High Speed USRT (HS-USRT)

The High Speed USRT (HS-USRT) is implemented in RH850/P1x-C and is not available in RH850/U2C. For detailed descriptions, please refer to the **RH850/P1x-C Group User's Manual: Hardware**

13.1.4 I3C Bus Interface (RI3C)

The I3C Bus Interface (RI3C) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**

13.1.5 Controller Area Network (CAN)

13.1.5.1 Modules Comparison

The RH850/U2C family implements CAN-FD and CAN XL using advanced, dedicated modules, while the RH850/P1x-C family uses the MCAN CAN controller for CAN-FD. Here's a comparison across features, performance, and compatibility:

Features:

- **RH850/U2C (RS-CANFD & CANXL):**
  - Supports Classical CAN (up to 8 bytes), CAN-FD (up to 64 bytes), and CAN XL (up to 2048 bytes)[1][2][3].
  - CAN XL module provides advanced message filtering (up to 256 RX filter elements), priority queues, multiple FIFO queues, and hardware time-stamping[2][1].
  - CAN-FD supports flexible transmission buffer assignment, flexible CAN mode (pairing channels to a single driver), and advanced error detection (parity, CRC, overrun, etc.)[4][5].
  - CAN XL offers programmable loop-back, fault injection, error logging, and privileged access for safety/security[2][1].
  - DMA and AXI bus support for high-speed data transfer and low CPU impact[2][1].
  - CAN XL supports disabling error signaling in the data phase for maximum throughput, as well as advanced error detection mechanisms (header CRC, 32-bit frame CRC, format check pattern)[6][7].
- **RH850/P1x-C (MCAN):**
  - MCAN controller supports Classical CAN and CAN-FD (up to 64 bytes payload)[8].
  - Standard message filtering and FIFO/buffer management, but less advanced than U2C's CANXL module.
  - No support for CAN XL protocol or its extended features.
  - Error detection and signaling as per ISO 11898-1:2015 for CAN-FD.
  - DMA support is available but less flexible than U2C's implementation.

Performance:

- **RH850/U2C:**
  - CAN-FD: Nominal bit rate up to 1 Mbps, data bit rate up to 8 Mbps[1][9][3].
  - CAN XL: Nominal bit rate up to 1 Mbps, data bit rate up to 16 Mbps[1][2][3].
  - CAN XL supports much larger payloads (up to 2048 bytes) and higher data rates, suitable for zonal architectures and high-bandwidth applications[2][1].
- **RH850/P1x-C (MCAN):**
  - CAN-FD: Nominal bit rate up to 1 Mbps, data bit rate up to 8 Mbps (device dependent)[8].
  - Maximum payload: 64 bytes.
  - No support for CAN XL, so limited to CAN-FD performance.

Compatibility:

- **RH850/U2C:**
  - CAN-FD and Classical CAN are backward compatible; CAN XL is not backward compatible and requires dedicated SIC-XL transceivers for maximum performance[10][11].
  - CAN XL can coexist with CAN-FD nodes, but CAN-FD-only nodes will ignore CAN XL traffic[12].
  - CAN XL supports migration by allowing mixed transceiver types under specific conditions[10].

- **RH850/P1x-C (MCAN):**
    - Compatible with Classical CAN and CAN-FD networks.
    - No support for CAN XL, so not compatible with CAN XL networks or features.

13.1.5.2 CANFD Interface

13.1.5.2.1 General Features

The functional features of CANFD controller in RH850/U2C are the same as in RH850/P1x-C devices. However, there are implementation differences in terms of:

- Unit and channel numbers
- Clock supply
- Interrupt requests
- Register base address

Please refer to the related User manual chapters for details.

13.1.5.2.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

13.1.5.2.3 Clock Supply

Table 13.7 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.7 Clock source of the CANFD on RH850/U2C and RH850/P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
<RSCFDn>/<MTTCAN0/MCANn>	Bus clock	Main OSC clock CLK_CANFD_XIN	CLK_HSB
	Communication clock	High-speed peripheral clock CLK_CANFD_C	CLKP_H2
	Peripheral clock	High-speed peripheral clock CLKC_HSB_CANFD	-
	RAM access clock	Peripheral ultra high speed clock CLKC_UHSB_CANFD	-

13.1.5.2.4 Register Base Address

Table 13.8 shows the difference between the register base addresses on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.8 Register Base Addresses of the CANFD on RH850/U2C and RH850/P1x-C Devices

Base Address Name	RH850/U2C	RH850/P1x-C
<RCFDC0_base>	FF80 0000$_H$	-
<RCFDC1_base>	FF82 0000$_H$	-
<MTTCAN0_base>	-	FFD3 0000$_H$
<MCAN0_base>	-	FFEF 0000$_H$
<MCAN1_base>	-	FFD3 1000$_H$
<MCAN2_base>	-	FFEF 1000$_H$

13.1.5.3 CANXL Interface

The CANXL Interface is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**

13.1.6 FlexRay (FLXA/FLX)

13.1.6.1 General Features

The FlexRay IP implementations on the RH850/U2C and RH850/P1x-C microcontrollers differ notably in architecture, configurability, and feature set. The RH850/U2C FlexRay IP is a newer, more advanced module designed for complex automotive networking and safety-critical applications. It supports up to 128 message buffers with flexible payload lengths (up to 254 bytes), advanced buffer management, scalable message RAM organization, and enhanced data transfer options such as direct host access and automatic hardware-supported network management. Additionally, the U2C offers multiple timers (absolute, relative, and stopwatch) for precise scheduling and more explicit diagnostic configuration options, including CRC handling and slot/cycle/channel filtering.

In contrast, the RH850/P1x-C FlexRay IP is based on an earlier generation and generally offers fewer advanced features, less flexibility in buffer configuration, and more limited register access and integration options. While both devices support two FlexRay channels (A and B) and conform to the FlexRay protocol specification v2.1 with data rates up to 10 Mbit/s per channel, the U2C implementation provides expanded configurability, buffer management, and diagnostic capabilities compared to the P1x-C.

13.1.6.2 Unit and Channel Numbers

Table 13.9 shows the differences between unit and channel numbers on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.9 Unit and Channel Numbers of RH850/U2C and RH850/P1x-C

Product Name	U2C8-EVA, U2C8, U2C4	U2C2	P1M-C, P1H-C(4MB, BGA-156)	P1H-C(4MB, BGA-292), P1H-CE
Units	1	-	1	2

13.1.6.3 Clock Supply

Table 13.10 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.10 Clock Supply of RH850/U2C and RH850/P1x-C

Unit Name	RH850/U2C unit clock	RH850/P1x-C unit clock
Bus Clock	CLK_HBUS_FLXA	CLKP_H1
FlexRay sample clock	CLKC_HSB_FLXA	CLKP_H1
NTU clock Source	-	CLK_HSB

13.1.6.4 Register Base Address

Table 13.11 shows the differences between the register base address on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.11 Register Base Address of RH850/U2C and RH850/P1x-C

RH850/U2C		RH850/P1x-C	
Base Address Name	**Base Address**	**Base Address Name**	**Base Address**
<FLXA0_base>	$1002\ 0000_H$	FLXA0	$1002\ 0000_H$
-	-	FLXA1	$1002\ 1000_H$

13.1.7 Ethernet

13.1.7.1 Modules Comparison

The Ethernet implementations in the RH850/U2C and RH850/P1x-C families differ significantly in terms of supported standards, features, performance, and compatibility, reflecting their respective generational advancements and target applications.

Features:

- **RH850/U2C:**
  - Supports multiple Ethernet standards: 100Base-TX, 1000Base-T1 (Gigabit TSN), and 10Base-T1S[1][2][3][4].
  - Up to 2 independent Ethernet units per device.
  - 10Base-T1S PHY is IEEE 802.3cg-2019 compliant, supporting point-to-point and multidrop topologies, advanced diagnostics, and PLCA features[4][5].
  - TSN (Time-Sensitive Networking) and AVB (Audio Video Bridging) support for deterministic, low-latency communication[2][3].
  - AVB-DMAC hardware enables precise audio/video transport protocol timing[6].
  - Modular evaluation boards allow flexible expansion for Ethernet, CAN-XL, and other interfaces[1][7].
  - No hardware-based gateway/forwarding between Ethernet units; forwarding must be implemented in software[8].
  - MCAL (AUTOSAR) support for TSN R-Switch and AVB units, with configurable transmit queues and port forwarding[9].
- **RH850/P1x-C:**
  - Supports standard 100Base-TX Ethernet[10][11].
  - Ethernet implementation is basic, focused on legacy automotive networking without TSN or 10Base-T1S support.
  - No support for advanced features like TSN, AVB, or 10Base-T1S.
  - No hardware-based audio/video transport protocol support or advanced diagnostics.
  - Evaluation boards provide standard Ethernet connectivity, lacking modular expansion for newer standards[1].
  - MCAL support is available for standard Ethernet units, but without TSN or AVB-specific features.

Performance:

- **RH850/U2C:**
  - Supports up to Gigabit Ethernet (1000Base-T1) with TSN, and 10Base-T1S for low-cost, deterministic networking[2][3][5].
  - 10Base-T1S PHY optimized for low latency and burst mode operation[4][5].
  - AVB-DMAC enables precise timing for audio/video applications[6].
  - Enhanced throughput and queue management for TSN/AVB use cases[9].
  - Evaluation boards can be configured for multiple Ethernet standards, supporting high-bandwidth and low-latency applications[1][7].
- **RH850/P1x-C:**
  - Limited to 100Base-TX Ethernet, suitable for legacy automotive networking[10][11].
  - No support for Gigabit, TSN, or 10Base-T1S, restricting performance in modern zonal or gateway architectures.

- Standard throughput and queue management, without advanced timing or prioritization features.

Compatibility:

- **RH850/U2C:**
  - Compatible with legacy Ethernet standards (100Base-TX) and newer standards (1000Base-T1, 10Base-T1S)[2][3][4][5].
  - TSN and AVB support enables integration into modern automotive E/E architectures.
  - Modular board design allows flexible interface selection and expansion[1][7].
  - No hardware-based Ethernet gateway; software implementation required for message forwarding between units[8].
  - MCAL supports TSN R-Switch and AVB, with flexible queue and port forwarding configuration[9].
- **RH850/P1x-C:**
  - Compatible with standard 100Base-TX Ethernet networks[10][11].
  - No support for TSN, AVB, or 10Base-T1S, limiting compatibility with newer automotive networking standards.
  - Evaluation boards provide basic Ethernet connectivity but lack expansion for advanced standards[1].
  - Physical channel/port availability: One Ethernet channel (ETNA0), with up to two MAC layer interface ports in the largest package (BGA-292)

13.1.7.2 Unit and Channel Numbers

Table 13.12 shows the differences between unit and channel numbers on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.12 Unit and Channel of RH850/U2C and RH850/P1x-C

Product Name	**U2C8-EVA, U2C8, U2C4**		**U2C2**		**P1M-C, P1H-C(4MB, BGA-156)**	**P1H-C(4MB, BGA-292), P1H-CE**
Unit Name	ETND	ETNF	ETND	ETNF	ETNA0	ETNA0
Number of Units	1	1	-	-	1	1

13.1.7.3 Clock Supply

Table 13.13 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.13 Clock Supply of RH850/U2C and RH850/P1x-C

RH850/U2C			RH850/P1x-C		
Unit Name	**Unit Clock Name**	**Supply Clock Name**	**Unit Name**	**Unit Clock Name**	**Supply Clock Name**
ETND	ACLK	CLKC_HBUS_ETND	**ETNA**	HCLK_0	CLK_HSB
	Register access clock	CLKC_HBUS_ETND		HCLK_1	CLK_HSB
ETNF	AXI clock	CLK_HBUS_ETNF		ETH0TXCLK	External clock
	APB clock	CLK_HBUS_ETNF		ETH1TXCLK	External clock
	gPTP clock	CLKC_HBUS_ETNF		ETH0RXCLK	External clock
	PCLA clock	CLKC_HBUS_ETNF		ETH1RXCLK	External clock
ETNFn_T1S	PCLK	CLKC_HBUS_ETNF		ETH0REF50CK	External clock
-	-	-		ETH1REF50CK	External clock

13.1.7.4 Register Base Address

Table 13.14 shows the differences between the register base address on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.14 Register Base Address of RH850/U2C and RH850/P1x-C

RH850/U2C				RH850/P1x-C	
ETND		**ETNF**		**ETNA**	
Base Address Name	**Base Address**	**Base Address Name**	**Base Address**	**Base Address Name**	**Base Address**
<TSNES0_base>	FF94 1000$_H$	<ETNF0_base>	FF1D 0000$_H$	ETNA0	1002 4000$_H$
<TSNES1_base>	FF95 1000$_H$	<ETNF0_T1S_base>	FF97 F000$_H$	-	-
<GPTMA0_base>	FF97 9000$_H$	-	-	-	-
<AXIBMI0_base>	FF94 0000$_H$	-	-	-	-
<AXIBMI1_base>	FF95 0000$_H$	-	-	-	-
<RMACS0_base>	FF94 2000$_H$	-	-	-	-
<RMACA0_base>	FF94 3800$_H$	-	-	-	-
<RMACS1_base>	FF95 2000$_H$	-	-	-	-
<RMACA1_base>	FF95 3800$_H$	-	-	-	-
<SGMII1_base>	FF97 8600$_H$	-	-	-	-
<PWRCTL0_base>	FF97 8400$_H$	-	-	-	-
<PWRCTL1_base>	FF97 8800$_H$	-	-	-	-

13.1.8 Single Edge Nibble Transmission (RSENT/SENT)

13.1.8.1 General Features

The RSENT IP on the RH850/U2C and the SENT IP on the RH850/P1x-C microcontrollers both implement the Single Edge Nibble Transmission (SENT) protocol for automotive sensor data communication, but they differ significantly in terms of supported standards, features, and channel count. RH850/U2C RSENT IP supports the SAE J2716 (APR2016) standard, offering the latest protocol features and compliance meanwhile RH850/P1x-C SENT IP supports the SAE J2716 (JAN2010) standard, providing core protocol features but based on an earlier revision.

For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware** and **RH850/P1x-C Group User's Manual: Hardware**

13.1.8.2 Unit and Channel Numbers

Table 13.15 shows the differences between unit and channel numbers on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.15 Unit and Channel of RH850/U2C and RH850/P1x-C

Product name	RH850/U2C	RH850/P1x-C			
		P1M-C(BGA-156), P1H-C(4MB, BGA-156)	P1M-C(QFP-144, BGA-292)	P1H-C(4MB, BGA-292), P1H-C(8MB)	P1H-CE
Number of channels	8(0 to 7)	4(0 to 3)	6(0 to 5)	8(0 to 7)	10(0 to 9)

13.1.8.3 Clock Supply

Table 13.16 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.16 Clock Supply of RH850/U2C and RH850/P1x-C

Unit name	RH850/U2C unit clock	RH850/P1x-C unit clock
Bus clock	CLK_HSB_RSENT	CLK_LSB
RSENT Communication clock	CLKC_HSB_RSENT	CLKP_H1

13.1.8.4 Register Base Address

Table 13.17 shows the differences between the register base address on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.17 Register Base Address of RH850/U2C and RH850/P1x-C

Product name	RH850/U2C	RH850/P1x-C
Base Address Name	**Base Address**	**Base Address**
<RSENT0_base>	FFD3 3600$_H$	FFCD C000$_H$
<RSENT1_base>	FFD8 D100$_H$	FFCD C100$_H$
<RSENT2_base>	FFD3 3700$_H$	FFCD C200$_H$
<RSENT3_base>	FFD8 D200$_H$	FFCD C300$_H$
<RSENT4_base>	FFD3 3800$_H$	FFCD C400$_H$
<RSENT5_base>	FFD8 D300$_H$	FFCD C500$_H$
<RSENT6_base>	FFD3 3900$_H$	FFCD C600$_H$
<RSENT7_base>	FFD8 D400$_H$	FFCD C700$_H$
<RSENT8_base>	-	FFCD C800$_H$
<RSENT9_base>	-	FFCD C900$_H$
<RSENTTSSEL_base>	FFD3 4500$_H$	-

13.1.9 Peripheral Sensor Interface 5 (PSI5)

The Peripheral Sensor Interface 5 (PSI5) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**

13.1.10 Peripheral Sensor Interface 5 S (PSI5S)

The Peripheral Sensor Interface 5 S (PSI5S) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**

13.1.11 Clock Extension Peripheral Interface (CXPI)

The Clock Extension Peripheral Interface (CXPI) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**

13.2 Timers

13.2.1 Window Watchdog Timer (WDTA/ WDTB)

13.2.1.1 General Features

The functional features of Window Watchdog Timer in RH850/U2C and RH850/P1x-C devices are similar, except the following points referring to Table 13.18

Table 13.18 Functional Differences of Window Watchdog Timer on RH850/U2C and RH850/P1x-C

Functional Features	Use purpose	RH850/U2C	RH850/P1x-C
Interrupt request signals	Configurable counter number	WDTB counter reaches a specific number or 75%	WDTB counter reaches 75%
Implementation Area	-	Both AWO and ISO	-

Figure 13.3, Block Diagram of WDTB0, Figure 13.4, Block Diagram of WDTBn (n = 1) &

Figure 13.5, Block Diagram of WDTBA shows the main components of the WDTB.

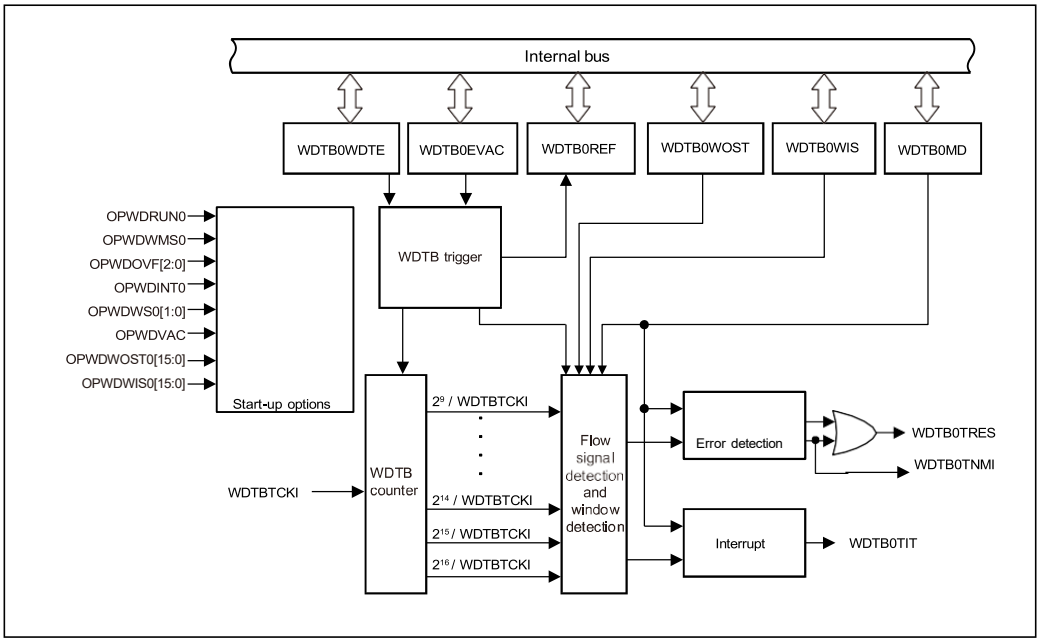


Figure 13.3 Block Diagram of WDTB0

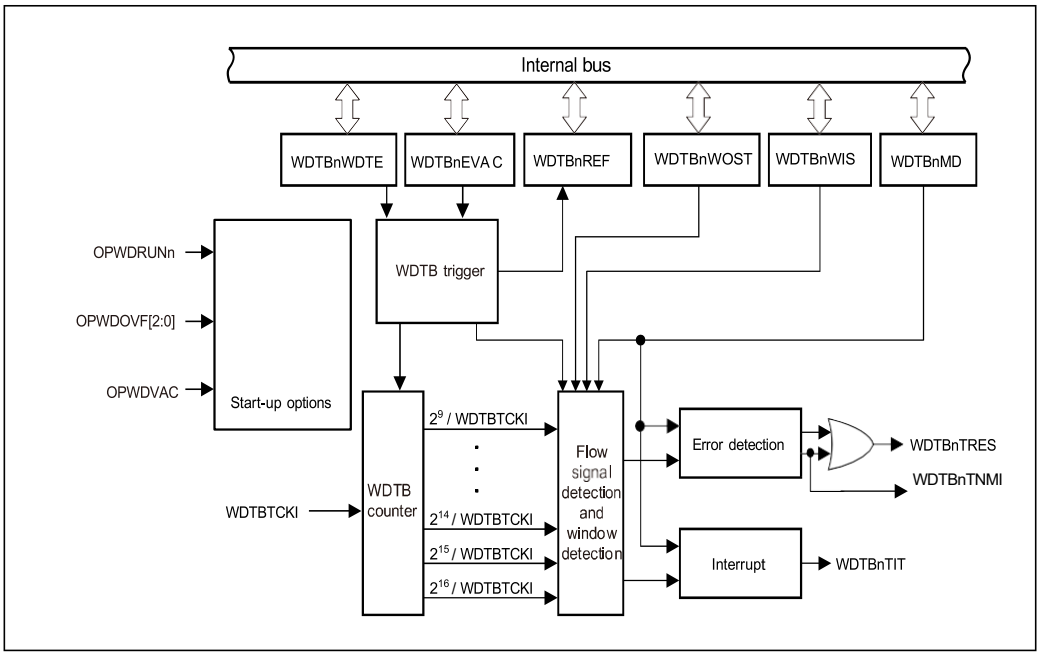


Figure 13.4 Block Diagram of WDTBn (n = 1)

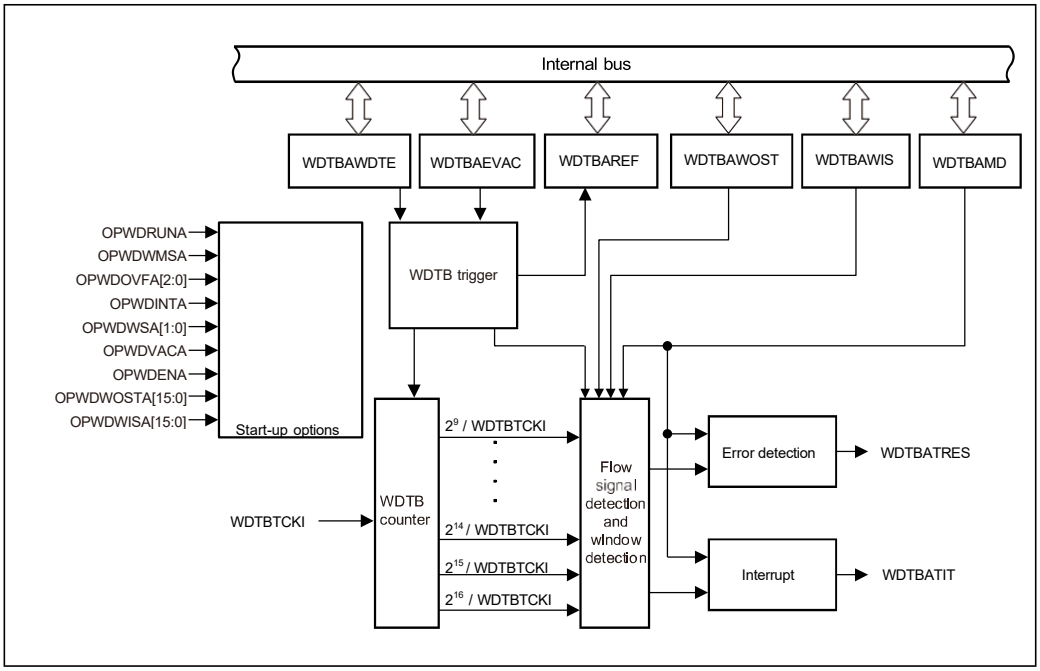


Figure 13.5 Block Diagram of WDTBA

Figure 13.6 shows the main components of the Window Watchdog Timer A

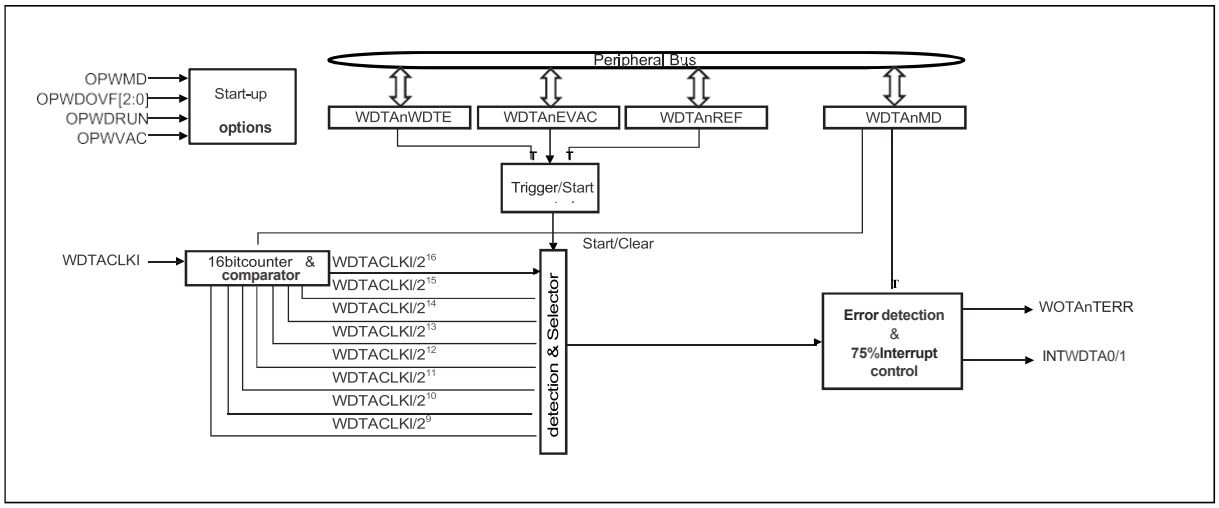


Figure 13.6 Block diagram of the Window Watchdog Timer A

Besides, there are also implementation differences in terms of:

- Unit and Channel Numbers
- Clock Supply
- Interrupt Request
- Reset Sources
- Register Base address
- Internal I/O Signals

13.2.1.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

13.2.1.3 Clock Supply

Table 13.19 shows the differences between the supplied clock on the RH850/U2C and RH850/P1x-C devices.

Table 13.19: Clock source of the WDTB on RH850/U2C and RH850/P1x-C Devices

Unit Clock Name	RH850/U2C	RH850/P1x-C	Description
WDTBn	CLK_HSB_WDTB	-	Bus clock
	CLK_WDTB		Timer count clock
WDTBA	CLK_LSB_WDTBA	-	Bus clock
	CLKA_WDTBA		Timer count clock
WDTAn	-	CLK_HSB	Bus clock
		WDTACLKI	Timer count clock

13.2.1.4 Reset Sources

Table 13.20 shows the different reset sources on the RH850/U2C and RH850/P1x-C devices.

Table 13.20 Reset source of the WDT on RH850/U2C and RH850/P1x-C Devices

Unit Name	RH850/U2C	RH850/P1x-C
WDTAn	-	INTWDTA0/1
WDTBn	INTWDTB0TIT/1TIT	-
WDTBA	INTWDTBATIT	-

13.2.1.5 Register Base address

Table 13.21 shows the differences between the register base addresses on the RH850/U2C and RH850/P1x-C devices.

Table 13.21 Register Base Addresses of the WDT on RH850/U2C and RH850/P1x-C Devices

Register name	RH850/U2C	RH850/P1x-C
<WDTBA_base>	FF9A 5000 H	-
<WDTB0_base>	FFBF 1000 H	-
<WDTB1_base>	FF89 9000 H	-
<WDTA0_base>	-	FFED 0000 H
<WDTA1_base>	-	FFED 1000 H

.

13.2.2 Generic Timer Module (GTM)

13.2.2.1 General Features

The RH850/U2C features a newer GTM IP version (v4.1) with potential improvements in scalability, configurability, and safety compared to the GTM IPs in the RH850/P1x-C series (v207/v208). The core architecture and programming model remain similar, but U2C may offer more advanced capabilities and higher channel counts.

Figure 13.7 shows the block diagram of the RH850/U2C GTM IP.

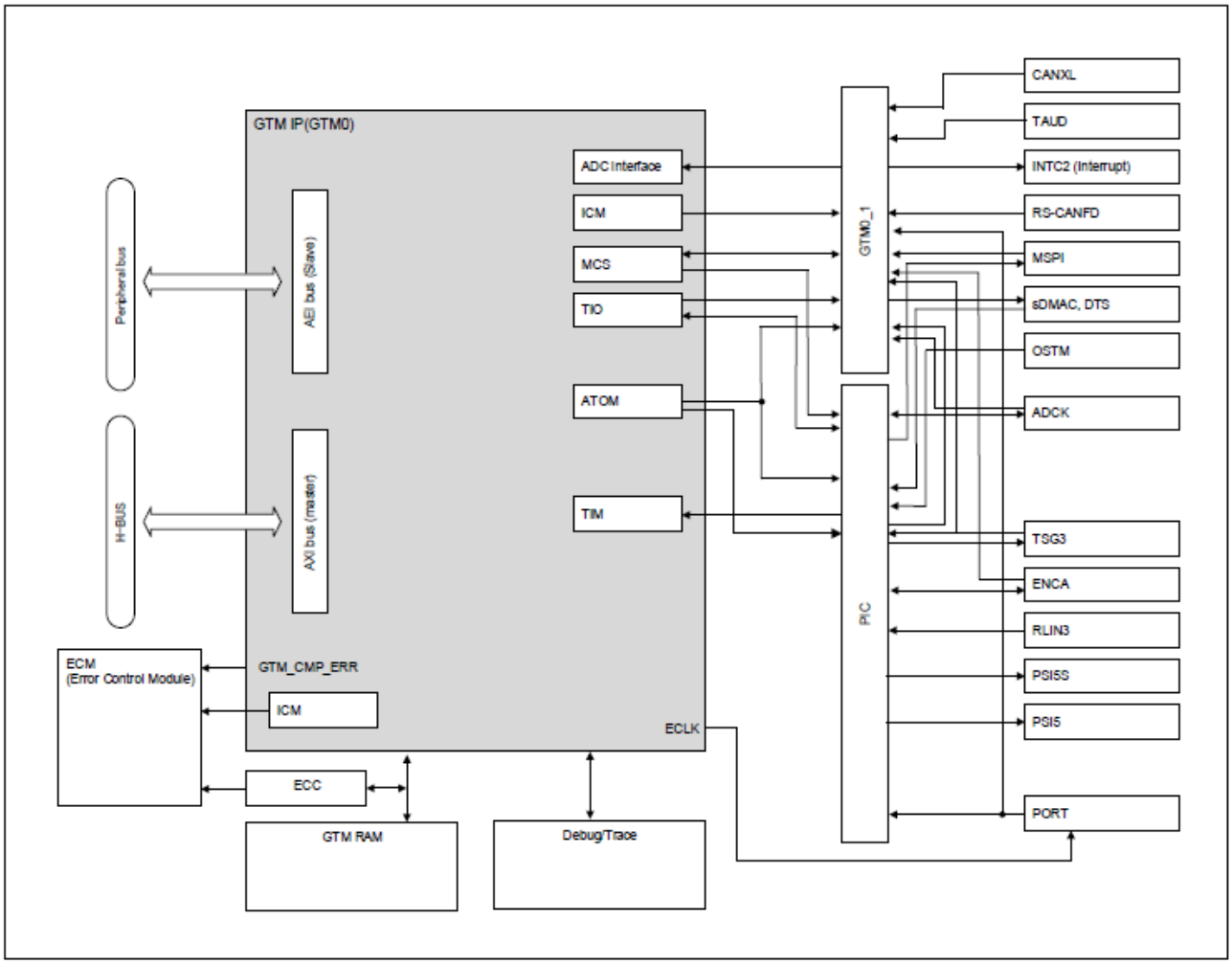


Figure 13.7 Block Diagram of RH850/U2C GTM

Figure 13.8 shows the block diagram of the RH850/P1x-C GTM IP.

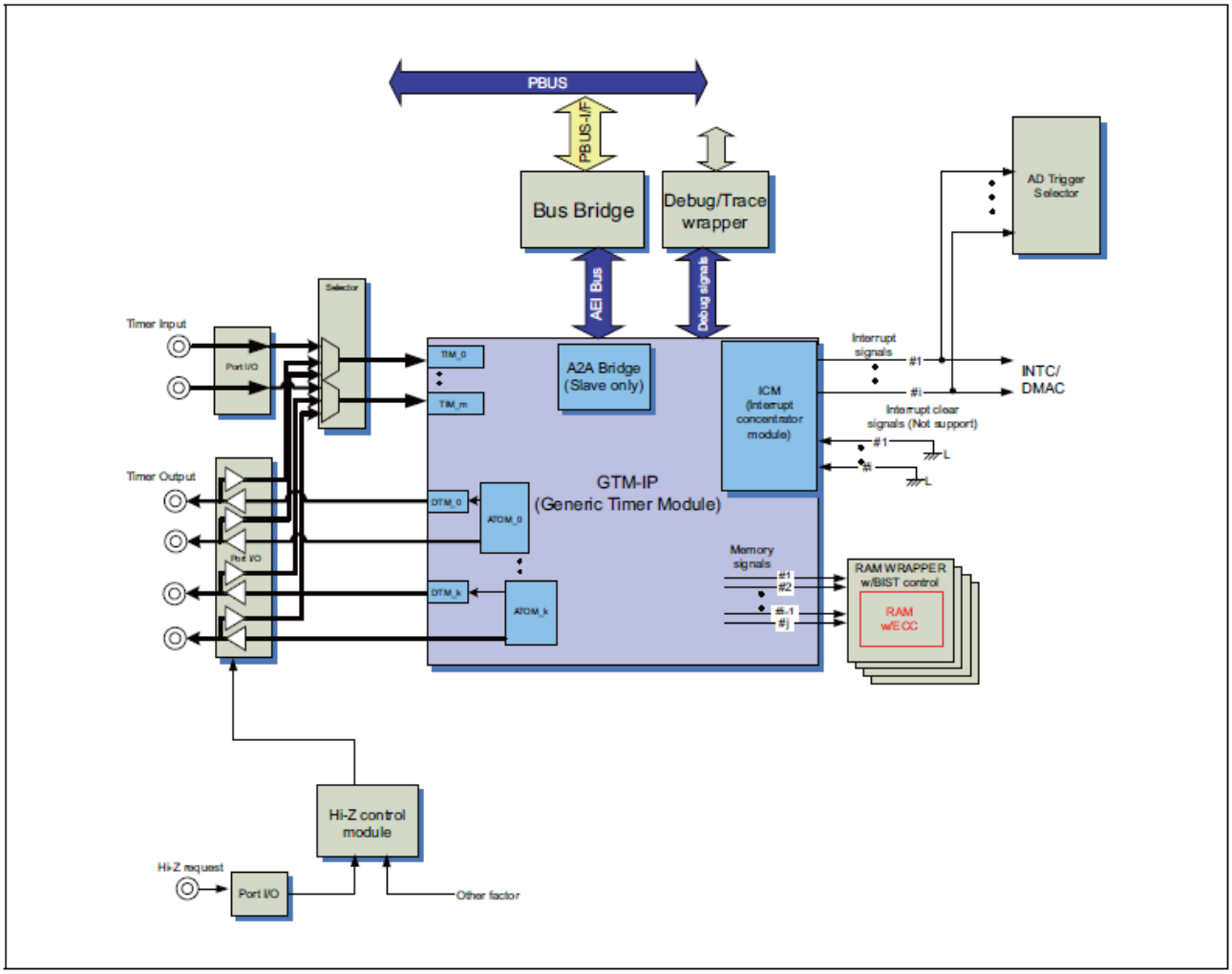


Figure 13.8 Block Diagram of RH850/P1x-C GTM

13.2.2.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

13.2.2.3 Clock Supply

Table 13.22 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.22 Clock Supply of RH850/U2C and RH850/P1x-C

Unit name		RH850/U2C unit clock	RH850/P1x-C unit clock
GTM Cluster 0 to n[*1] (MCS0-1 and associated RAM)	GTM Main Clock	CLK_GTM Switchable between 1/1(high) and 1/2(low) frequency	-
	Register access clock	CLK_GTM	-
GTM	AEI-bus clock	-	CLK_HSB
	GTM global clock	-	CLK_HSB

Note 1. For RH850/U2C8-EVA and RH850/U2C8 n is 2. For RH850/U2C4 and RH850/U2C2 n is 1.

13.2.2.4 Register Base Address

Table 13.23 shows the differences between the register base address on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.23 Register Base Address of RH850/U2C and RH850/P1x-C

Register Base Name	RH850/U2C base address	RH850/P1x-C base address
<GTM0_base>	FF60 0000$_H$	FFE0 0000$_H$
<GTM0_1_base>	FFF5 8000$_H$	-

13.2.3 System Timer (STM)

The System Timer (STM) is implemented in RH850/P1x-C and is not available in RH850/U2C. For detailed descriptions, please refer to the **RH850/P1x-C Group User's Manual: Hardware.**

13.2.4 OS Timer (OSTM)

The OS Timer (OSTM) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.5 Long-Term System Counter (LTSC)

The Long-Term System Counter (LTSC) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.6 Timer Array Unit D (TAUD)

The Low-Power Sampler (LPS) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.7 Timer Array Unit J (TAUJ)

The Timer Array Unit J (TAUJ) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.8 Motor Control Timer (TSG3)

The Motor Control Timer (TSG3) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.9 Timer Option (TAPA)

The Timer Option (TAPA) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.10 Real-Time Clock (RTCA)

The Real-Time Clock (RTCA) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.2.11 Encoder Timer A (ENCA)

The Encoder Timer A (ENCA) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.3 External Memory Interfaces

The MMCA (Multi Media Card Interface A) and SFMA (Serial Flash Memory Interface A) modules in the RH850/U2C microcontroller family, and the MEMC (Memory Controller) in the RH850/P1x-C family, are all external memory interface modules, but they differ significantly in their supported memory types, protocols, and features:

- **MMCA (RH850/U2C):** This module is designed specifically for interfacing with eMMC storage devices. It supports the JEDEC JESD84-A441 standard, offers various bus widths (1/4/8-bit), high-speed mode, block transfer, boot operation, DMA support, and ECC for peripheral RAM. MMCA is tailored for block-based storage and is not a generic memory expansion interface.

- **SFMA (RH850/U2C):** This module is intended for high-speed serial flash memory access, supporting external serial flash devices via SPI, Dual SPI, and Quad SPI modes. It is optimized for interfacing with serial NOR flash and allows memory-mapped access but does not support DMA or interrupts. SFMA is not designed for general-purpose RAM expansion.

- **MEMC (RH850/P1x-C):** This is a generic external memory controller for parallel memory devices such as SRAM, NOR flash, or ASICs. MEMC provides address/data bus control, chip select management, and programmable wait states for parallel memory devices. It does not support the specialized eMMC or serial flash protocols, nor does it offer DMA or ECC features found in MMCA/SFMA.

For more details refer to **RH850/P1x-C Group User's Manual: Hardware** and **RH850/U2C Group User's Manual: Hardware.**

13.4 Peripheral Interconnect (PIC)

13.4.1 General Features

Motor control functions in RH850/P1x-C devices include PIC2C. In the RH850/U2C series, TAPA and PIC are covered in separate chapters, with PIC having two sections: PIC1 and PIC2.

Table 13.24 Functional Differences of PIC on RH850/U2C and RH850/P1x-C

Functional Features RH850/U2C		Functional Features RH850/P1x-C
PIC1	**PIC2**	**PIC2C**
• Simultaneous start trigger function • TSG simultaneous start trigger function (external trigger) • INT signal output selection function • PWM output function with dead time • High accuracy triangle wave PWM output function with dead time • Delay pulse output function with dead time • Trigger pulse width measurement function • Encoder capture trigger select function • Two-phase encoder control function • Two-phase encoder control function • Three-phase pulse input control function • Three-phase encoder control function • Timer input select function • Switch function between TSG output and low/high level output • Hi-Z control function • Timer output monitor function • TSG3 synchronous start and clear function • TAUD input selection function • GTM synchronous start trigger	• ADCK trigger selection • ENCA trigger selection • PSI5S time stamp and sync signal selection • PSI5 time stamp and sync signal selection • GTM timer input selection • TAUD trigger output function • Baud rate measurement for an UART (RLIN3) • Hi-Z control function over external pin for GTM output • GTM output monitor for PWM diagnostic • IO sharing CAN / GTM-Internal arbitration • MSPI trigger selection function • TSG3 inputs from GTM	• ADCF trigger select function • Signal routing function for GTM:

Besides, there are also implementation differences in terms of:

- Unit and Channel Numbers
- Clock Supply
- Interrupt Request
- Reset Sources
- Register Base address
- External I/O Signals
- Internal I/O Signals
- Peripheral Configuration

Please refer to the related User manual chapters for details

13.4.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

13.4.3 Clock Supply

Table 13.25 shows the difference between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 13.25 Clock source of the PIC1/PIC0 on U2C and P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
PIC2C/PIC1/PIC2	Bus clock	CLKC_HSB	CLK_HSB
	Communication clock	-	-

13.4.4 Register Base Address

Table 13.26 Register Base Addresses of the PIC1/PIC0 on U2C and P1x-C Devices

Base Address Name	Base address U2C	Base address P1x-C
<PIC10_base>/<PIC2C_base>	FFBF AF00$_H$	FFD6 8000$_H$
<PIC1_SELB_base>	FFBF B800$_H$	-
<PIC20_base>	FFBF C000$_H$	-
<PIC21_base>	FFBF C800$_H$	-
<PIC22_base>	FFBF D000$_H$	-
<PIC2_SELB_base>	FFBF E000$_H$	

13.5 PWM Output/Diagnostic (PWM-Diag)

The PWM Output/Diagnostic (PWM-Diag) is implemented in RH850/U2C and is not available in RH850/P1-xC. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

13.6 Serial Sound Interface (SSIF)

The Serial Sound Interface (SSIF) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

14. Analog peripherals

14.1 Analog to Digital Converter (ADCKn / ADCFn)

14.1.1 General Features

Table 14.1 lists the functional differences of ADC on RH850/U2C and RH850/P1x-C devices.

Table 14.1 Functional Differences of ADC on RH850/U2C and RH850/P1x-C

Feature	RH850/U2C	RH850/P1x-C
ADC Units	ADCKn	ADCFn
Track & Hold (T&H)	Supported on certain channels on ADCK1, ADCK2 and ADCKA	-
Scan Groups	5 Scan Groups per ADCK unit	5 Scan Groups per ADCF unit
Diagnostic Function	• Wiring-break detection mode 1 (pull-down) • Wiring-break detection mode 2 (pull-down or pull-up) • Voltage monitoring function	-
Self-Diagnostic Function	• Pin-level self-diagnostic function • T&H path self-diagnostic function • A/D core self-diagnostic function • Wiring-break detection self-diagnostic function • Voltage monitoring self-diagnostic function • A/D conversion of A/D conversion data path diagnosis	• PIN level diagnostic function • SAR-ADC diagnostic function • Open wiring and break detection
Wait Function	Support to insert a wait before the A/D conversion sampling time.	-
Sampling Time and Settings	• Default: 18 cycles • Common settings for all scans: 102 or 204 or 252 cycles • Extended sampling: 60 or 102 or 138 or 252 cycles	18 cycles
Error Detection	• Read and clear functions for the data registers • Parity check for the data registers • Overwrite check for the data registers • ID error • Upper/Lower Limit Check (8 tables) • Trigger overlap Check	• Read and clear functions for the data registers • Parity check for the data registers • Overwrite check for the data registers • Upper/Lower Limit Check (8 tables) • ID error
A/D conversion monitor output	Supported	-

14.1.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

14.1.3 Clock Supply

Table 14.2 shows the difference between the supplied clock of ADC on U2C and P1x-C devices.

Table 14.2 Clock Supply of the ADC on U2C and P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
ADCKn/ADCFn	Register access clock	CLKC_LSB_SADC	CLK_LSB
	CLKAD	CLKC_LSB_SADC	-
ADCKA	Register access clock	CLKA_ADC	-
	CLKAD	CLKA_ADC	-
AVSEG	Register access clock	CLKA_ADC	

14.1.4 Register Base address

Table 14.3 Register Base Address of the ADC on U2C and P1x-C Devices

Base Address Name	Base Address U2C	Base Address P1x-C
<ADCK1_base>/<ADCF0_base>	FFF2 0000$_H$	FFF9 1000$_H$
<ADCK2_base>/<ADCF1_base>	FFF2 1000$_H$	FFF9 2000$_H$
<ADCKA_base>	FF9A 2000$_H$	-
<ADCKA_SELB_base>	FF9A 3000$_H$	-
<AVSEG_base>	FF9A 3400$_H$	-

14.2 Temperature Sensor (OTS)

14.2.1 General Features

The functional features of the Temperature Sensor in RH850/P1x-C series are similar in RH850/U2C devices. However, there are implementation differences in terms of:

- Clock connections
- Interrupt assignments
- Base address

Please refer to the related User manual chapters for details.

14.2.2 Unit and Channel Numbers

Both devices have 1 unit and 1 channel.

14.2.3 Clock supply

Table 14.4 shows the supplied clock on the RH850/U2C and RH850/P1x-C devices.

Table 14.4 Clock Supply for the Temperature Sensor on RH850/U2C and RH850/P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
OTS0	Operation clock	CLKC_LSB	CLK_HSB
	Register access clock	CLK_LSB	CLKP_L

14.2.4 Register Base Address

Table 14.5 shows the differences between the register base addresses on the RH850/U2C and RH850/P1x-C devices.

Table 14.5 Register Base Addresses of the Temperature Sensor on RH850/U2C and RH850/P1x-C Devices

Register name	RH850/U2C	RH850/P1x-C
<OTS0_base>	FFC0 0200_H	FFF9 3000_H

14.3 Low-Power Sampler (LPS)

The Low-Power Sampler (LPS) is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware.**

15. Functional Safety

15.1 General Features

Both RH850/U2C and RH850/P1x-C families provide comprehensive safety modules, including robust hardware mechanisms and software-based supervision. The main differences lie in the evolution of safety concepts, the balance of hardware vs. software responsibility, and the level of system integration and flexibility, with U2C reflecting newer safety philosophies and P1x-C maintaining a more traditional approach.

Table 15.1 shows the General Features of the safety mechanisms on the RH850/U2C and RH850/P1x-C devices.

Table 15.1 General Features of the Safety Mechanisms on RH850/U2C and RH850/P1x-C (1/2)

Item	Safety Mechanisms	
	RH850/U2C	RH850/P1x-C
ASIL level	ASIL D	ASIL D
Power Supply Voltage Monitor	VMON	CVM
Clock Monitor	Supported	Supported
Data Protection	ECC for code flash, data flash and RAM EDC for instruction cache	ECC for code flash, data flash and RAM EDC for instruction cache
Watchdog Timer	Supported	Supported
Data CRC	Supported	Supported
Access Protection	MPU Guards for memories and peripherals	MPU Guards for memories and peripherals
SW Measures	End-to-End (E2E) protection for data integrity across communication interfaces Input redundancy and plausibility checks Output loopback or output monitoring (if not covered by hardware) Watchdog timer management and supervision (external watchdogs are assumed for higher ASIL) Software flow monitoring and control flow checks Periodic software self-tests and diagnostics for safety mechanisms Error handling and safe state transition routines Safety-related software partitioning and memory protection	Software protection of flash memory using dedicated registers (FHVE3 and FHVE15) to prevent unauthorized programming, erasure, or blank checking Software-based comparison and monitoring of timer outputs and inputs to detect failures in the Timer Output Module (TOM) and Timer Input Module (TIM) Implementation of software routines for error handling and diagnostics in case of detected faults by hardware mechanisms (ECC/EDC, watchdog, clock monitor, etc.) Use of software to configure and monitor memory protection units and guard functions for illegal access prevention Periodic software self-tests and BIST routines for startup and runtime verification Software management of external safety measures, such as external watchdog timers and voltage monitors, as required by the SEooC approach Safe State Management and error escalation procedures

Table 15.1 General Features of the Safety Mechanisms on RH850/U2C and RH850/P1x-C (2/2)

Item	Safety Mechanisms	
	RH850/U2C	RH850/P1x-C
HW Self Diagnosis features (ADC)	Self-diagnosis of the wiring-break detection A/D converter self-diagnosis Pin-level self-diagnosis Self-diagnosis of the T&H path Self-diagnosis of the voltage monitor function A/D conversion of A/D conversion data path diagnosis	Self-diagnosis of the wiring-break detection A/D converter self-diagnosis Pin-level self-diagnosis
Redundant Channels / Output Loop Back	GPIO PWM ADC GTM	Timer PWM GTM
Serial Interfaces (SPI, CAN, LIN, Ethernet)	Internal and External Loopback/Self-Test Error Detection and Reporting Interrupt Generation for Error/Status Events CRC/Data Integrity Checking/ECC Dual-Core Lockstep and Multi-Core Safety	Internal and External Loopback/Self-Test Error Detection and Reporting Interrupt Generation for Error/Status Events CRC/Data Integrity Checking/ECC
Lockstep	Supported	Supported
Error Control Module (ECM)	Supported	Supported

For further details, please refer to the safety manual.

15.2 Error Control Module (ECM)

15.2.1. General Features

The Error Control Module (ECM) in the RH850/U2C microcontroller is significantly more advanced and safety-oriented compared to the ECM in the RH850/P1x-C microcontroller.

Table 15.2 lists the specification overview of ECM on RH850/U2C and RH850/P1x-C devices.

Table 15.2 Specification overview of ECM on RH850/U2C and RH850/P1x-C (1/3)

Feature	RH850/U2C	RH850/P1x-C
Safety processing	ECM can handle the following processing in response to error signal inputs from individual modules. • Error flag set • Interrupt generation Either FE or EI level interrupt generation can be selected for individual errors. Notified CPU can be selected with one, multicast or broadcast for individual errors. If there is configuration that interrupt does not notify anywhere, it means interrupt generation is disable. • Internal reset generation System Reset 2 generation can be controlled (enabled/disabled) for individual errors. • Error pin output Pin output mask can be controlled (enabled/disabled) for individual errors. Output can be toggled in response to a timer input or made at a fixed level.	ECM can handle the following processing in response to error signal inputs from individual modules. • Error flag set • EI level interrupt generation EI level interrupt generation can be controlled (enabled/disabled) for individual errors. • FE level interrupt generation FE level interrupt generation can be controlled (enabled/disabled) for individual errors. • Internal reset generation System reset 2 generation can be controlled (enabled/disabled) for individual errors. • Error pin output Pin output mask can be controlled (enabled/disabled) for individual errors. Output can be toggled in response to a timer input or made at a fixed level.
Error status	ECM incorporates error source status registers, which can be used to confirm the error status from the error flag. ECM can capture the error source without own clock. The error flags are only cleared by a Power On Reset, DeepSTOP Reset or writing to clear register. In case of External reset (System Reset 1), System Reset 2, Application Reset, Module Reset and JTAG Reset, the error flags are kept and the reset generation source can be confirmed by reading the status register after reset.	ECM incorporates the error status register, which can be used to confirm the error status from the error flag. The error flags are only cleared by software or a power on reset. In case of reset except for power on reset, the error flags are kept and the reset generation source can be confirmed by reading the status register after reset

Table 15.2 Specification overview of ECM on RH850/U2C and RH850/P1x-C (2/3)

Feature	RH850/U2C	RH850/P1x-C
Debug, self-diagnosis	• Pseudo errors can be generated for debug and self-diagnosis. The operation during injection of pseudo errors is identical to that for the occurrence of real errors. All configurations for the masking of the error pin output, interrupt, or Error Control Module Reset apply in the same way. • ECM incorporates a loop-back function of the error output pin (ERROROUT_M) that is used to diagnose the path to the error output pin. The status of the error output pin is reflected to an internal register and can be confirmed by reading the register.	• Pseudo errors can be generated for debug and self-diagnosis. The operation during injection of pseudo errors is identical to that for the occurrence of real errors. All configurations for the mask to the error pin output, interrupt, or Error Control Module Reset apply in the same way. • ECM incorporates a loop-back function of the error pin output that is used to diagnose the path to the error output pin. The status of the error output pin is reflected to an internal register and can be confirmed by reading the register.
Self-Diagnostic Function	• Pin-level self-diagnostic function • T&H path self-diagnostic function • A/D core self-diagnostic function • Wiring-break detection self-diagnostic function • Voltage monitoring self-diagnostic function • A/D conversion of A/D conversion data path diagnosis	-
Timeout function	ECM incorporates a function that generates an error output or Error Control Module Reset when the count value of the delay timer matches with the delay timer compare register because the delay timer was not stopped during the interrupt processing after being started simultaneously with the occurrence of an interrupt request..	ECM incorporates a function that generates an error signal output or Error Control Module Reset when the count value of the delay timer matches with the delay timer compare register because the delay timer was not stopped during the interrupt processing after being started simultaneously with the occurrence of an interrupt request.
Port safe state	Error triggers (ERROROUTnZ) connect to port safe state and ECM can control the state of general purpose I/O to a condition (Hi-Z) according to user configuration.	-

Table 15.2 Specification overview of ECM on RH850/U2C and RH850/P1x-C (3/3)

Feature	RH850/U2C	RH850/P1x-C
Register protection	A write-protection with a key code is implemented to protect registers from illegal write access.	A write-protection with a special sequence is incorporated to protect registers from inadvertent write access.
Error output and Error triggers clear masking	ECM incorporates a function that can mask software clearance of Error output and Error triggers until the counter which is started from error occurrence reaches the value specified in the configuration registers. If another error occurs during time counting, then the time count is reset and restarted from 0.	ECM incorporates a function that can mask software clearance for ERROROUTZ until the time which is counted from error occurrence reaches with the Error Output Clear Invalidation Configuration register. If another error occurs during time counting, then the time count is reset and restarted from the beginning.
Hi-Z control signal trigger into PIC	ECM triggers Hi-Z control signal into PIC. Hi-Z control signal (ERROROUTZ) is triggered at the same condition when ECM activates Error output pin.	ECM triggers Hi-Z control signal into PIC. Hi-Z control signal is triggered at the same condition when ECM activates ERROROUTZ pin.
Others	ECM is duplexed. ECM incorporates the error output pin. Error output and Error triggers for Port Safe State from the ECM master and checker are constantly compared. If they do not match, an ECM compare error occurs.	ECM is duplexed. ECM incorporates the error output pin.

15.2.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

15.2.3 Clock supply

Table 15.3 shows the difference between the supplied clock of ECM on RH850/U2C and RH850/P1x-C devices.

Table 15.3 Clock Supply of the ECM on RH850/U2C and RH850/P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
ECM/ECMn	KCRC module clock	CLK_HSB	CLK_HSB
	Register access clock	CLK_ECMCNT	CLK_IOSC/2

15.2.4 Register Base Address

Table 15.4 shows the differences between the register base addresses on the RH850/U2C and RH850/P1x-C devices.

Table 15.4 Register Base Addresses of the ECM on RH850/U2C and RH850/P1x-C Devices

Register name	RH850/U2C	RH850/P1x-C
<ECM_base>/ <ECMM0_base>	FFCC D000$_H$	FFD6 0000$_H$
<ECMM_base>/ <ECMC0_base>	FFCC E000$_H$	FFD6 1000$_H$
<ECMC_base>/ <ECM0_base>	FFCC F000$_H$	FFD6 2000$_H$
<ECMM1_base>	-	FFCB 0000$_H$
<ECMC1_base>	-	FFCB 1000$_H$
<ECM1_base>	-	FFCB 2000$_H$

15.3 Data CRC (KCRC/DCRB)

15.3.1 General Features

Both RH850/U2C and RH850/P1x-C platforms provide hardware CRC modules with AUTOSAR-compliant features. However, the U2C platform offers more advanced, scalable, and safety-integrated CRC capabilities, with enhanced support for modern communication protocols and multi-core/virtualized environments.

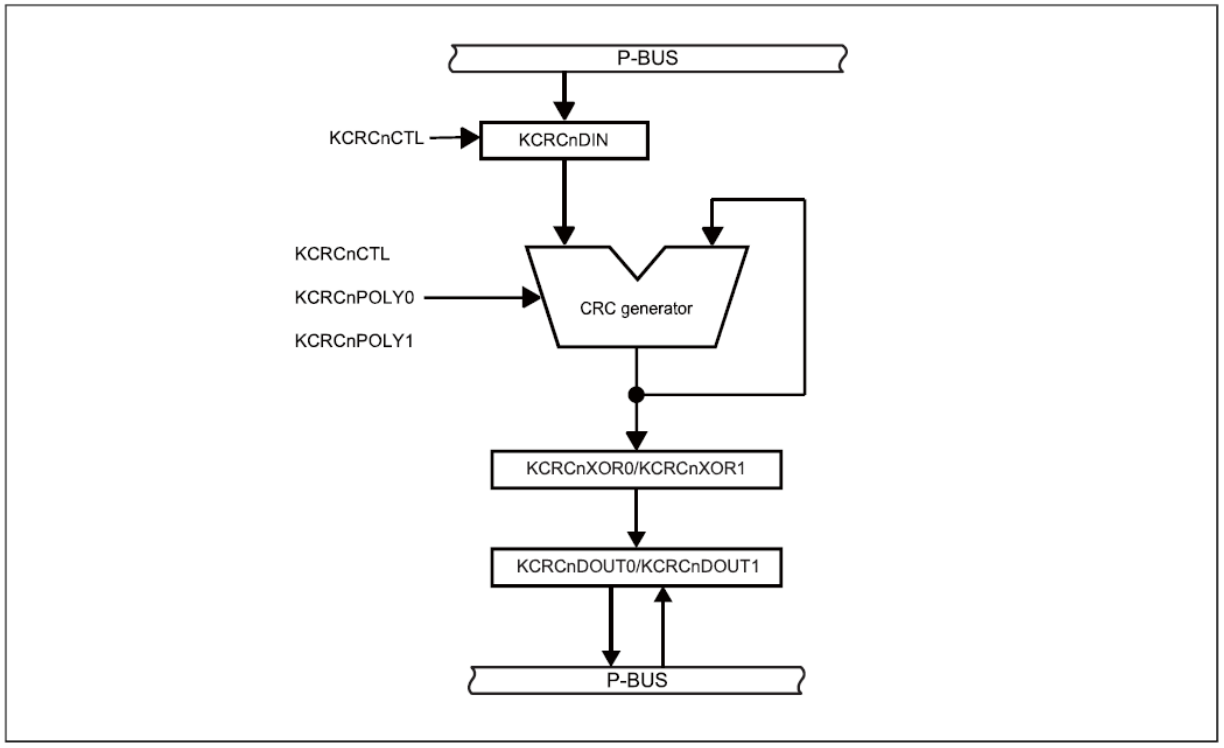


Figure 15.1 Block Diagram of Data CRC Function K

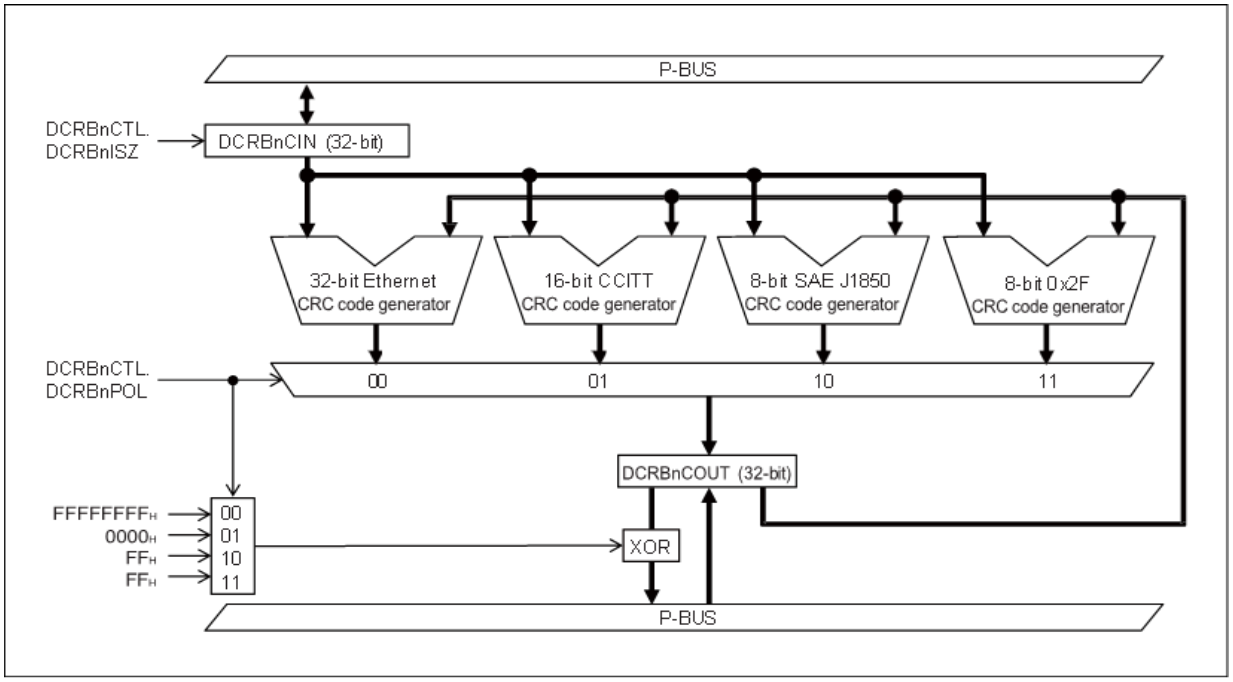


Figure 15.2 Block diagram of Data CRC Function B

15.3.2 Unit and Channel Numbers

The unit and/or channel number is different between RH850/P1x-C and RH850/U2C. For details, please refer to **Section 1. Feature Overview**

15.3.3 Clock supply

Table 15.5 shows the difference between the supplied clock of Data CRC on U2C and P1x-C devices.

Table 15.5 Clock Supply of the Data CRC on U2C and P1x-C Devices

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
KCRCn/DCRBn	KCRC module clock	CLK_HSB	CLK_HSB
	Register access clock	CLK_HSB	CLK_HSB

15.3.4 Register Base Address

Table 15.6 shows the differences between the register base addresses on the RH850/U2C and RH850/P1x-C devices.

Table 15.6 Register Base Addresses of the Data CRC on RH850/U2C and RH850/P1x-C Devices

Register name	RH850/U2C	RH850/P1x-C
<KRC0_base>/ <DCRB0_base>	FFD4 0000$_H$	FFD5 0000$_H$
<KRC1_base>/ <DCRB1_base>	FFD8 E000$_H$	FFD7 0000$_H$
<KRC2_base>/ <DCRB2_base>	FFD4 0200$_H$	FFD5 1000$_H$
<KRC3_base>/ <DCRB3_base>	FFD8 E200$_H$	FFD7 1000$_H$
<KRC4_base>/ <DCRB4_base>	FFD4 0400$_H$	FFD5 2000$_H$
<KRC5_base>/ <DCRB5_base>	FFD8 E400$_H$	FFD7 2000$_H$
<KRC6_base>/ <DCRB6_base>	FFD4 0600$_H$	FFD5 3000$_H$
<KRC7_base>/ <DCRB7_base>	FFD8 E600$_H$	FFD7 3000$_H$

16. Renesas Security IP Module (ICUMHB/ICUMC)

- ICUMHB is implemented for RH850/U2C devices.
- ICUMC is implemented for RH850/P1x-C devices.

The ICUMHB module in the RH850/U2C microcontroller is a highly advanced hardware security module (HSM) that offers comprehensive security and cryptographic capabilities. It features a dedicated secure processor (ICUP), multiple cryptographic engines supporting a wide range of algorithms (including AES with 128/192/256-bit keys, SM4, SHA-1/2/3, SM3), a true random number generator, and a public key cryptography coprocessor (PKCC) for RSA and ECC. ICUMHB also includes a direct memory access controller (DMAC) for efficient data transfers, exclusive access to secure flash/data flash, and robust protection mechanisms for debugging and testing. It supports advanced hardware-level domain separation and secure memory management, making it suitable for high-security automotive applications and compliance with standards like EVITA-Full and ASIL D.

In contrast, the ICUMC module in the RH850/P1x-C microcontroller provides only basic cryptographic functions and security features. It includes a dedicated secure CPU (RH850G3K), hardware accelerator for AES, a random number generator, hardware-level domain separation, secure flash/data flash areas, and robust debug/flash access protection. However, ICUMC lacks the extensive cryptographic algorithm support, dedicated secure CPU for advanced cryptography, advanced domain separation, and secure memory management found in the ICUMHB. Notably, ICUMC does not provide hardware acceleration for asymmetric cryptography (RSA/ECC) and supports only the EVITA-Medium security level

For more detailed information, please refer to the security manuals.

17. On-chip Debug (OCD)

17.1 General Features

Table 17.1 Functional Differences of On-chip Debug on RH850/U2C and RH850/P1x-C (1/2)

Functional Features	RH850/U2C	RH850/P1x-C
Debug Interface	NEXUS JTAG	NEXUS JTAG
	Low Pin Count Debug Interface (4-pin) (LPD4)	Low Pin Debug Interface (4 pins) (LPD4)
	Aurora trace interface [For U2C8-EVA only]	-
	Trigger Input / Output pin (EVTI/EVTO)	-
	RHSIF debug interface (RHSIFD).[For U2C8-EVA only]	-
	Reset out pin RESETOUT	-
Run Control Functions	Debug functions	Debug functions
	On-chip break functions	On-chip break functions
	Software break function	Software break function
	Forced break function	Forced break function
	Peripheral break control	-
	Forced reset function	Forced reset function
	Reset mask function	Mask Function
	Event detection function	Event detection function
	Trigger input interface	Trigger Input Interface (P1H-CE only)
	Trigger output interface	Trigger Output Interface (P1H-CE only)
	Debug interrupt interface function	Debug Interrupt Interface Function (P1H-CE only)
	Multi core debug function	-
Trace Control Functions	Trace RAM [For U2C8-EVA only]	Trace Interface: Aurora (P1H-CE only)
	Trace filter RAM [For U2C8-EVA only]	-
	Software trace	Software Trace
	Trace over reset	-
	Global timestamp information	-
	The trace message format conforms to the Nexus standard	-
	Windowed instruction trace or data trace	-

Table 17.1 Functional Differences of On-chip Debug on RH850/U2C and RH850/P1x-C (2/2)

Debug Support Functions	Hot plug-in function	Hot plug-in function
	Security function	Security function
	Halt after reset	-
	Halt after reset with FBIST	-
	ICUMHB debug function	-
	GTM debug function	-
	Device ID function	-
	Reset output pin	-
Calibration Functions	Real-time RAM monitoring (RRM)	Real-time RAM Monitor (RRM)
	Dynamic memory modification (DMM)	Dynamic Memory Modify (DMM)
	Global Calibration Function Unit (GCFU)	-

For more details refer to **RH850/P1x-C Group User's Manual: Hardware** and **RH850/U2C Group User's Manual: Hardware.**

18. Memory

18.1 Flash Memory

18.1.1 General Features

RH850/U2C provides a more advanced, scalable, and safety/security-focused flash memory subsystem compared to RH850/P1x-C. U2C is better suited for applications requiring high reliability, functional safety, and secure operations, while P1x-C offers solid but more basic flash memory features.

Table 18.1 Features Differences of Flash memory on RH850/U2C and RH850/P1x-C

Functional Features	RH850/U2C	RH850/P1x-C
Code Flash Capacity	Up to 8 MB (banked, multi-bank support)	Up to 10 MB (multi-core, banked)
Data Flash Capacity	Up to 384 KB + 64 KB (ICUMHB, security module)	Up to 192 KB + 32 KB (ICUMC exclusive)
Flash Architecture	Advanced banked structure: multi-bank, bank swap, secure regions	Banked structure, less advanced bank swap/secure region features
OTA Update Support	Yes: Robust, with flexible bank usage and secure update	Not explicitly supported
Security/Protection	Advanced: Hardware-level domain separation, flash protection, ICUMHB HSM	Standard: OTP, ID authentication, block protection, option bytes
Calibration/Emulation RAM	Up to 4 MB ERAM (emulation devices only)	Only P1H-CE variant: 2 MB ERAM; others do not support this
Boot/Configuration Areas	User boot area, product info area, ECC test area, hardware property area	Option bytes in extended flash area, boot area depends on mode
Security Module	ICUMHB (HSM) with advanced crypto services, ACEU (AES)	ICUMC (HSM) for security, less advanced than U2C
Flash Suspend/Resume	Supported	Not explicitly specified
Functional Safety	ASIL-D, advanced safety mechanisms, robust error detection	ASIL-D, standard safety mechanisms
Emulation/Debug Support	Advanced: Real-time RAM monitoring, dynamic memory modification (emulation devices)	Only P1H-CE: Emulation RAM; others do not support this

Table 18.2 Basic Functional Differences of Flash memory on RH850/U2C and RH850/P1x-C

Basic Functions	RH850/U2C		RH850/P1x-C	
	Serial Programming	Self-Programming	Serial Programming	Self-Programming
Blank checking	Support	Support	Support	Conditional support
Block erasure	Support	Support	Support	Support
Programming	Support	Support	Support	Support
Verification and checksum	-	-	Support	-
Reading	Support	Support	Support	Support
Setting of Security Settings (Setting an ID Codes)	Support	Support	Support	Conditional Support
Setting an ID	-	-	-	Support
Setting of Block Protection	Support	Support	Conditional support	Support
Setting of Configuration Settings	Support	Support	-	-
Setting for OTP (one-time programming)	-	-	Support	Support
Protection Settings			Support	Support
Setting of option bytes	-	-	Support	Support
Clearing the configuration	-	-	Support	-

18.1.2 Register Base Address

Table 18.3 shows the differences between the register base address on the RH850/U2C devices and the RH850/P1x-C devices.

Table 18.3 Register Base Address of RH850/U2C and RH850/P1x-C

Register Name	RH850/U2C	RH850/P1x-C
<CCIB0_base>/<DCIB0>	FFFB 0800$_H$	FFC5 9800$_H$
<SCDS_base>/<DCIB1>	FFCD 0000$_H$	FFC5 9900$_H$
<FACI0_base>/<SCDS>	FFA1 0000$_H$	FFCD 0000$_H$
<FACI2_base>/<SYSCTL>	FFA1 8000$_H$	FFF8 0800$_H$

18.1.3 Clock Supply

Table 18.4 shows the differences between the supplied clock on the RH850/U2C devices and the RH850/P1x-C devices.

Table 18.4 Clock Supply of RH850/U2C and RH850/P1x-C

Unit Name		RH850/U2C unit clock	RH850/P1x-C unit clock
FACIn/FACI	Peripheral clock	CLK_LSB	CLK_LSB

18.2 RAM

This section describes the differences between RAM areas of RH850/U2C and RH850/P1x-C using as references RH850/U2C8 and RH850/P1H-C(8MB).

An overview of RAM on RH850/U2C and RH850/P1x-C is described in Table 18.5.

Table 18.5 Overview of RAM on RH850/U2C8 and RH850/P1H-C(8MB)

RAM Type	RH850/U2C8		RH850/P1H-C(8MB)	
	RAM Size	RAM Initialization	RAM Size	RAM Initialization
Local RAM per CPU	128KB	SW only	64 KB	HW supported
Cluster RAM /Global RAM	1248KB		960 KB	
Retention RAM	32KB		-	
Trace RAM	32KB	-	-	-
I-cache RAM(tag)	256 line x 2/core	-	256 line x 2/core	-
I-cache RAM(data)	2KB x 4/core	-	4KB x 4/core	-

18.2.1 Local RAM

Local RAM remains unchanged and there is no functional difference between RH850/U2C and RH850/P1x-C.

Still, there are implementation differences in terms of

- RH850/U2C does not have implemented buffers between CPU and RAM.
- Start and End Address

Table 18.6 Start and End Address of Local RAM on RH850/U2C8 and RH850/P1H-C(8MB)

Address name	RH850/U2C8		RH850/P1H-C(8MB)	
	Start Address	End Address	Start Address	End Address
Local RAM (self)	FDE0 0000$_H$	FDE1 FFFF$_H$	FEDF 0000$_H$	FEDF FFFF$_H$
Local RAM (CPU1)	FDA0 0000$_H$	FDA1 FFFF$_H$	FEBC 0000$_H$	FEBF FFFF$_H$
Local RAM (CPU0)	FDC0 0000$_H$	FDC1 FFFF$_H$	FE9F 0000$_H$	FE9F FFFF$_H$

For details, please refer to **RH850/P1x-C Group User's Manual: Hardware** and **RH850/U2C Group User's Manual: Hardware.**

18.2.2 Cluster RAM

The Cluster RAM or Global RAM remains unchanged and there is no functional difference between RH850/U2C and RH850/P1x-C.

Still, there are implementation differences in terms of

- Start and End Address

Table 18.7 Start and End Address of Cluster RAM on RH850/U2C8 and Global RAM on RH850/P1H-C(8MB)

Address Name	RH850/U2C8		RH850/P1H-C(8MB)	
	Start Address	End Address	Start Address	End Address
Cluster RAM 0	FE00 0000$_H$	FE13 7FFF$_H$	-	-
Global RAM (bank A)	-	-	FEE8 8000$_H$	FEEF FFFF$_H$
Global RAM (bank B)	-	-	FEF0 0000$_H$	FEF7 7FFF$_H$

For details, please refer to **RH850/P1x-C Group User's Manual: Hardware** or **RH850/U2C Group User's Manual: Hardware.**

18.2.3 Retention RAM

The Retention RAM is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**.

18.2.4 I-Cache RAM

The I-Cache RAM remains unchanged and there is no functional difference in RH850/U2C and RH850/P1x-C.

18.2.5 Trace RAM

The Trace RAM is implemented in RH850/U2C and is not available in RH850/P1x-C. For detailed descriptions, please refer to the **RH850/U2C Group User's Manual: Hardware**.

19. Software Ecosystem comparison

Table 19.1 Ecosystem Comparison (1/2)

Ecosystem	RH850/U2C	RH850/P1x-C
IDE	Supported by Green Hills Multi, IAR Embedded Workbench, Renesas CS+, and Smart Configurator (graphical code generation). These IDEs offer advanced debugging, multicore support, and functional safety editions. Smart Configurator provides GUI-based peripheral and pin configuration, code generation, and plausibility checks. Eclipse-based e2 studio is not a primary IDE for U2C.	Supported by Renesas e2 studio (Eclipse-based IDE) and CS+. Also compatible with iSYSTEM WinIDEA, Lauterbach TRACE32, PLS UDE, Tasking IDE, and WindRiver Compiler. No support for Smart Configurator or graphical code generation tools. GHS Multi IDE is supported but lacks code generation or pin configuration features.
Programmer	Supported by Renesas PG-FP6 programmer and Renesas Flash Programming Software (RFP), with both on-line and off-line programming. Multiple partner programmer vendors also support U2C.	Supported by Renesas PG-FP6 programmer and RFP, with programming security IDs supported. Partner programmer support is available, but advanced features like those for U2C are not mentioned.
Emulator	Supported by Renesas E2 On-Chip Debugging Emulator and IE850A Full Functional Emulator (AURORA Trace). Third-party emulator support includes Lauterbach TRACE32, iSYSTEM, and PLS UDE. High-end trace and advanced monitoring features are available.	Supported by Renesas E1/E2 emulator and third-party emulators (iSYSTEM WinIDEA, Lauterbach TRACE32, PLS UDE). No emulation devices for P1x-C; only piggyback boards are available. OCD trace features can be used with Lauterbach or E2 emulator.
Auto code generation	Supported by Smart Configurator for GUI-based code generation, peripheral/port driver configuration, and pin assignment.	No support for Smart Configurator or similar tools. Manual driver development is required.
Evaluation boards	Modular evaluation platform with piggyback boards for all package variants and main boards for added functionality (Ethernet, FlexRay, CAN, LIN). Add-on extension boards are available for advanced features.	Piggyback boards and mainboards are available for various pin counts, but no emulation adapters or advanced network feature boards are mentioned.
Driver library	In-house AUTOSAR MCAL (ASIL D, ISO26262 compliant) and AUTOSAR BSW/OS from major third-party suppliers. Security software (HSM) and sample code for SPI and CAN-XL peripherals are available.	No Smart Configurator or MCAL support. No official driver code for FlexRay/CAN/UART; only some application code for RS-CANFD and RLIN3 (GHS environment). Manual driver development is required.

Table 19.1 Ecosystem Comparison (2/2)

Ecosystem	RH850/U2C	RH850/P1x-C
Security drivers	Security stack (CycurHSM) and HSM Security Software available from multiple vendors. ISO21434 and China crypto supported in hardware.	Security features are present but less advanced, with no mention of dedicated security driver stacks or ISO21434 support.
Virtual platform	Virtual platform solutions are available from Synopsys and ASTC. Virtualization solution platform with RTA-HVR (Hypervisor), RTA-CAR (Classic AUTOSAR), and CycurHSM. Built-in hardware support for hypervisor, privilege management, and freedom-from-interference.	No information available regarding virtual platform solutions. It is possible that the device does not support such features or that documentation is not available.

Revision history

Rev.	Date	Description	
		Section	Summary
1.00	2026.01.30	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

5. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

6. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

7. Power ON/OFF sequence

   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply

   after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

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