RX210 Group, RX230 Group, RX231 Group

Migrating from the RX210 Group to the RX230 Group or RX231 Group

Introduction

This application note describes guidelines for migrating microcontroller code from the RX210 Group to the RX230 Group or RX231 Group, which are highly compatible with the RX210 Group.

With the exception of some dedicated pins, the pin assignments of the RX230 Group and RX231 Group are identical to those of the RX210 Group. The RX230 Group and RX231 Group have the same functions (backward compatible) as the RX210 Group as well as new functions that are not included in RX210 Group microcontrollers.

The specifications of the RX210 Group microcontrollers are compared below with those of RX230 Group and RX231 Group microcontrollers with the same package pin counts, and information is provided to enable users to confirm points of difference.

100-pin, 64-pin, and 48-pin packages

The RX231 Group is available in three versions: A, B, and C. The differences between these three versions are summarized below.

Peripheral Module	Version A	Version B	Version C
CAN interface	Yes	Yes	No
SD host interface (SDHIa)	No	Yes	No
Security functions	No	Yes	No

The descriptions in this application note apply mainly to version B.

This application note provides guidelines for smooth migration from the RX210 Group to the RX230 Group or RX231 Group. It does does not cover all the details of the differences in the specifications of the above products.

Refer to the User's Manual: Hardware of each of the above products when migrating program code.

Target Devices

RX210 Group, RX230 Group, and RX231 Group

When not otherwise indicated, descriptions refer to the 100-pin package version of the RX210 Group, RX230 Group, and RX231 Group.

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1. Overview for Migration Design

Compared to the RX210 Group, the RX230 Group and RX231 Group are improved to have higher processing power and reduce power consumption. The DSP and communication functions are also enhanced. In addition, the FPU and encryption/decryption function (optional) are newly added.

There are some points to keep in mind about hardware and software when migrating from the RX210 Group to RX230 Group and RX231 Group.

Section 2 “Notes on the Pin Design” describes notes on hardware. Section 3 “Notes on the Function Settings” describes notes on software.

2. Notes on the Pin Design

The RX231 Group provides USB communication functionality, and the RX230 Group and RX231 Group incorporate enhanced RTC functionality that enables operation on a dedicated battery backup power supply. Therefore, some pin assignments differ from those of the RX210 Group.

Notes on 100-pin packages are described below. For notes on 64-pin and 48-pin packages, refer to tables for differences in pin function and differences in power supply, clock, and system control pins in section 4.2 “Differences in Pin Functions”.

2.1 Main Clock Oscillator

The main clock frequency in the RX230 Group and RX231 Group are the same as the RX210 Group when VCC ≥ 2.4 V. However, when VCC < 2.4 V, the main clock frequency in the RX230 Group and RX231 Group are limited to the range from 1 to 8 MHz.

2.2 VCL Pin (External Capacity)

On the RX230 Group and RX231 Group, connect a 4.7μF smoothing capacitor to the VCL pin for internal power supply stabilization.

2.3 VBATT Pin

Power can be supplied to the realtime clock (RTC) and sub-clock oscillator from the dedicated battery backup power pin (VBATT pin) when the voltage of the VCC pin drops in the RX230 Group and RX231 Group.

When the battery backup function is not used in the RTC or when the sub-clock oscillator is not used, connect the VBATT pin to the VCC pin.

2.4 Mode-Setting Pins

The pin assignment of the mode-setting pins in the RX231 Group is the same as the RX210 Group. In single-chip mode, the levels of the MD pin and PC7/UB pin after a reset is released are the same between the two groups. However, for boot mode or user boot mode, refer to the following notes on handling the PC7/UB pin.

The RX231 Group does not have user boot mode. In the RX210 Group, the MCU operates in user boot mode when a reset is released while the MD pin is low and the PC7/UB pin is high. Under those settings, the RX231 Group operates in boot mode (USB interface). The RX230 Group has no UB pin, so there is no boot mode (USB interface).

Table 2.1 lists mode-setting pins and operating modes.

When using the on-chip debugging emulator (E1/E20 emulator), connect the MD pin to the E1/E20 emulator and drive the PC7/UB pin low, or connect the MD pin and PC7/UB pin to the E1/E20 emulator. Refer to “On-Chip Debugging Emulator” listed in 5 Reference Documents for details.

Notes on mode-setting pins apply to the 100-pin, 64-pin, and 48-pin packages.

Refer to 3.2.1 UB Code for the alternate function of user boot mode.

Table 2.1 Mode-Setting Pins and Operating Modes

Mode-Setting Pin		Operating Mode		
MD	**PC7/UB**	**RX210**	**RX230**	**RX231**
High	—	Single-chip mode	Single-chip mode	
Low	Low	Boot mode	Boot mode (SCI interface)	
	High	User boot mode when the UB code is used. Boot mode when the UB code is not used.	Boot mode (SCI interface)	Boot mode (USB interface)

2.5 General I/O Ports

Ports PH0 to PH3 are not provided on RX231 Group microcontrollers. Port PJ1 is not provided on RX230 Group and RX231 Group microcontrollers. Change these pins to other general I/O ports.

2.6 External Interrupt Pins

The PH1/IRQ0 pin and PH2/IRQ1 pin are not provided in the RX231 Group.

Change the IRQ0 pin to the P30/IRQ0 pin or PD0/IRQ0 pin.

Change the IRQ1 pin to the P31/IRQ1 pin or PD1/IRQ1 pin.

2.7 Input Pin for the Clock Frequency Accuracy Measurement Circuit

The PH0/CACREF pin is not provided in the RX231 Group.

Change the CACREF pin to the PA0/CACREF pin or PC7/CACREF pin.

2.8 Analog Input Pins

Pins AN016 to AN023 (8 channels) in the RX231 Group correspond to pins AN008 to AN015 in the RX210 Group. Pins AN024 to AN031 (8 channels) are added to the RX231 Group.

The AVCC0 pin in the RX230 Group and RX231 Group is the analog voltage supply pin for the 12-bit A/D converter and 12-bit D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and 12-bit D/A converter.

The AVSS0 pin in the RX230 Group and RX231 Group is the analog ground pin for the 12-bit A/D converter and 12-bit D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and 12-bit D/A converter.

Refer to 3.6 12-Bit A/D Converter for details on software for analog input.

2.9 I/O Pins for the 8-Bit Timer

Pins PH1/TMO0, PH2/TMRI, and PH3/TMCI0 are not provided in the RX231 Group.

The TMO0 pin is a compare match output pin. Change this pin to the P22/TMO0 pin or PB3/TMO0 pin.

The TMRI0 pin is a counter reset input pin. Change this pin to the P20/TMRI0 pin or PA4/TMRI0 pin.

The TMCI0 pin is an input pin for the external clock to be input to the counter. Change this pin to the P21/TMCI0 pin or PB1/TMCI0 pin.

2.10 I/O Pins for Multi-Function Timer Pulse Unit 2

The PJ1/MTIOC3A pin is not provided in the RX230 Group and RX231 Group.

The MTIOC3A pin is a TGRA3 input capture input/output compare output/PWM output pin for multi-function timer pulse unit 2. Change this pin to the P14/MTIOC3A pin, P17/MTIOC3A pin, PC1/MTIOC3A pin or PC7/MTIOC3A pin.

2.11 Analog Pin for Comparator A1

The PE3/CMPA1 pin and comparator A are not provided in the RX230 Group and RX231 Group.

The PE3/CMPA1 is an input pin for the comparator A1 analog signal. Change this pin to the PE1/CMPB0 pin, PA3/CMPB1 pin, P15/CMPB2 pin, or P26/CMPB3 pin that is an input pin for the comparator B analog signal.

3. Notes on the Function Settings

The RX230 Group and RX231 Group provide a high level of compatibility with software that runs on the RX210 Group. Nevertheless, thorough evaluation is necessary because of differences with the operation timing and electrical characteristics of the RX210 Group.

The processing capabilities of the RX230 Group and RX231 Group can be enhanced by making use of improved DSP instructions and newly added FPU instructions. To take advantage of these improvements it is necessary to rebuild your source code using a compiler, assembler, and library generator capable of generating instruction codes for the RXv2 instruction set architecture.

For details, see the information on compilers in 5, Reference Documents.

Points related to function settings that differ between the RX210 Group and the RX230 Group and RX231 Group, which should be kept in mind when writing software, are touched on below.

For details on points of difference in modules and functions, see 4.3, Differences in Modules and Functions.

When making use of this application note, make sure to perform thorough evaluation on the target system.

3.1 Floating-Point Operation

The floating-point operation instructions (FPU instructions) are newly added in the RX230 Group and RX231 Group supporting operation with the float type or double type in C. When using the FPU instructions, set the RM[1:0] bits (floating-point rounding-mode setting) in the floating-point status word (FPSW) register.

When using the FPU instructions in the exception handling routine, save the floating-point status word (FPSW) on the stack within the exception handling routine.

Refer to sections CPU and Exception Handling of User's Manual: Hardware listed in 5 Reference Documents for details.

3.2 Option-Setting Memory

Check the setting values for the IWDTTOPS[1:0] bits (IWDT timeout period select) in the option function select register 0 (OFS0) and the VDSEL[1:0] bits (voltage detection 0 level select) in the option function select register 1 (OFS1).

Refer to 4.4.5 Option-Setting Memory for differences. Refer to User's Manual: Hardware listed in 5 Reference Documents for details.

3.2.1 UB Code

User boot mode is not provided in the RX230 Group and RX231 Group. UB code A and UB code B necessary for user boot mode are also not provided.

In the RX230 Group and RX231 Group, the user area/data area of the flash memory can be programmed and read with an arbitrary interface using start-up program protection instead of user boot mode.

Refer to the Start-Up Program Protection section of User's Manual: Hardware listed in 5 Reference Documents for details.

3.3 Clock Generation Circuit

The following clocks have been added on the RX230 Group: peripheral module clock A (PCLKA) supplied to MTU2 and SSI clock (SSISCK) supplied to the SSI and LPT clock (LPTCLK) supplied to the LPT. The following clocks have been added on the RX231 Group: peripheral module clock A (PCLKA) supplied to MTU2, SSI clock (SSISCK) supplied to the SSI, USB clock (UCLK) supplied to the USB, and LPT clock (LPTCLK) supplied to the LPT, and CAN clock (CANCLK) supplied to the CAN. The peripheral modules other than MTU2 operate in synchronization with peripheral module clock B (PCLKB). For software that uses MTU2 on the RX210 Group, set the frequency of peripheral module clock B (PCLKB) to the same frequency as peripheral module clock A (PCLKA).

The multiplication factor of the PLL circuit of the RX230 Group and RX231 Group is selectable within a range of 4 to 13.5 (in increments of 0.5). The PLL oscillation frequency is 24 MHz to 54 MHz (VCC ≥ 2.4 V). When using the PLL circuit, change the settings to satisfy these conditions.

The following table lists the frequencies of on-chip oscillators in the RX230 Group and RX231 Group.

On-Chip Oscillator	RX210	RX230 and RX231
High-speed on-chip oscillator (HOCO)	32 MHz, 36.864 MHz, 40 MHz, 50 MHz	32 MHz, 54 MHz
Low-speed on-chip oscillator (LOCO)	125 kHz	4 MHz
IWDT-dedicated on-chip oscillator	125 kHz	15 kHz

When changing the system clock (ICLK) in the RX230 Group and RX231 Group to the frequency that is higher than 32 MHz, set the memory wait cycle setting register (MEMWAIT).

Refer to 4.4.7 Clock Generation Circuit for the differences. Refer to User's Manual: Hardware and Application Note: Initial Setting listed in 5 Reference Documents for details.

3.4 Low Power Consumption

Change deep software standby mode in the RX210 Group to software standby mode in the RX230 Group and RX231 Group. Current consumption of software standby mode is equal to that of deep software standby mode.

Change all-module clock stop mode in the RX210 Group to deep sleep mode in the RX230 Group and RX231 Group. Current consumption of deep sleep mode is equal to that of all-module clock stop mode.

Change operating power control modes to the following modes: High-speed operating mode, middle-speed operating mode, and low-speed operating mode.

Refer to 4.4.9 Low Power Consumption for the differences. Refer to User's Manual: Hardware listed in 5 Reference Documents for details.

3.5 Battery Backup Function

When voltage of the VCC pin drops in the RX230 Group and RX231 Group, power can be supplied to the RTC and the sub-clock oscillator from the VBATT pin.

When not using the battery backup function in the RTC or when not using the sub-clock oscillator, set the VBATTDIS bit in the VBATT control register (VBATTCR) to 1 (battery backup function disabled).

3.6 12-Bit A/D Converter

The 12-bit A/D converter is enhanced, and I/O registers used for this function are added in the RX231 Group. For software that uses pins AN008 to AN015 in the RX210 Group, assign the eight channels to any of pins AN016 to AN031 that are expanded in the RX230 Group and RX231 Group.

Refer to 4.4.24 12-Bit A/D Converter for the differences. Refer to 12-Bit A/D Converter (S12ADE) of User's Manual: Hardware listed in 5 Reference Documents for details.

3.7 Comparator A

The RX230 Group and RX231 Group does not have comparator A. Change comparator A to comparator B (comparator B0 to comparator B3).

Refer to User's Manual: Hardware listed in 5 Reference Documents for details.

3.8 Flash Memory

Since the flash memory in the RX230 Group and RX231 Group needs shorter time to be programmed and erased, the manufacturing efficiency is improved and power consumption is reduced, which can reduce the manufacturing cost. Software that is used in self-programming of single-chip mode in the RX210 Group has to be changed.

Refer to 4.4.29 ROM (flash memory for code storage) for the differences. Refer to User's Manual: Hardware and Application Note: Initial Setting (R01AN2185EJ) listed in 5 Reference Documents for details.

4. Points of Difference

4.1 Differences in Outline of Specifications

Table 4.1 lists differences in outline of specifications. Maximum specifications of the 100-pin package are listed. The number of channels for the peripheral module varies with the number of pins of the package.

Specifications that exist only in one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that exist in both groups are indicated in black.

Table 4.1 Differences in Outline of Specifications

Item		RX210	RX230 and RX231
CPU	Central processing unit	• Maximum operating frequency: 50 MHz • 32 bit RX (RXv1) • Register 16 general-purpose registers (32 bits) 8 control registers (32 bits) 1 accumulator (64 bits) • 73 basic instructions — • 9 DSP instructions • 10 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits —	• Maximum operating frequency: 54 MHz • 32 bit RX (RXv2) • Register 16 general-purpose registers (32 bits) 10 control registers (32 bits) 2 accumulator (72 bits) • 75 basic instructions • 11 floating-point instructions • 23 DSP instructions • 10 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit → 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	Not available	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	Capacity:1024/768/512/384/256/128/96/64 Kbytes • 50 MHz, no-wait memory access • On-board programming Boot mode (SCI) — User boot mode Self-programming • Off-board programming	• Capacity: 512/384/256/128/64 Kbytes • 32 MHz or less: no-wait memory access 32 to 54 MHz: No wait states for a hit, wait states for a miss • On-board programming Boot mode (SCI) Boot mode (USB interface) — Self-programming • Off-board programming
	RAM	Capacity: 96/64/32/20/16/12 Kbytes 50 MHz, no-wait memory access	Capacity: 64/32 Kbytes 54 MHz, no-wait memory access
	E2 DataFlash	Capacity: 8 Kbytes	Capacity: 8 Kbytes

Item	RX210	RX230 and RX231
MCU operating mode	Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)	Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock generation circuits	Main clock oscillator Sub-clock oscillator Low-speed and high-speed on-chip oscillators PLL frequency synthesizer IWDT-dedicated on-chip oscillator — • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) • The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) — • S12AD run in synchronization with the PCLKB: 50 MHz (at max.) • Peripheral modules other than S12AD run in synchronization with the peripheral module clock (PCLK): 32 MHz (at max.) • Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 25 MHz (at max.) *4 • The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)	Main clock oscillator Sub-clock oscillator Low-speed and high-speed on-chip oscillators PLL frequency synthesizer IWDT-dedicated on-chip oscillator USB-dedicated PLL frequency synthesizer*3 • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) • The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) • MTU2a runs in synchronization with the PCLKA: 54 MHz (at max.) • S12AD run in synchronization with the PCLKB: 54 MHz (at max.) • Peripheral modules other than MTU2a and S12AD run in synchronization with the PCLKB: 32 MHz (at max.) • Devices connected to external buses run in synchronization with the BCLK: 16 MHz (at max.) *4 • The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets	RES# pin reset Power-on reset Voltage monitoring reset Watchdog timer reset Independent watchdog timer reset Software reset Deep software standby reset	RES# pin reset Power-on reset Voltage monitoring reset Watchdog timer reset Independent watchdog timer reset Software reset —

Item	RX210	RX230 and RX231
Voltage detection circuit	• Voltage detection circuit (LVDAa) • When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. • Selectable detection voltage levels Voltage detection circuit 0: 4 levels Voltage detection circuit 1: 16 levels Voltage detection circuit 2: 16 levels	• Voltage detection circuit (LVDAb) • When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. • Selectable detection voltage levels Voltage detection circuit 0: 4 levels Voltage detection circuit 1: 14 levels Voltage detection circuit 2: 4 levels
Battery backup function	Not available	Available
Low power consumption functions	• Module stop function • Low power consumption modes: Sleep mode All-module clock stop mode Software standby mode Deep software standby mode	• Module stop function • Low power consumption modes: Sleep mode — Software standby mode — Deep sleep mode
Function for lower operating power consumption	• Operating power control modes High-speed operating mode Middle-speed operating mode 1A Middle-speed operating mode 1B Middle-speed operating mode 2A*1 Middle-speed operating mode 2B*1 Low-speed operating mode 1 Low-speed operating mode 2	• Operating power control modes High-speed operating mode Middle-speed operating mode — — — — Low-speed operating mode
Interrupt controller	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 7 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, IWDT interrupt, and VBATT power monitoring interrupt) • 16 levels specifiable for the order of priority

Item	RX210	RX230 and RX231
External bus extension	• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. • Capacity of each area: 16 Mbytes (CS0 to CS3) • A chip-select signal (CS0# to CS3#) can be output for each area. • Each area is specifiable as an 8-bit or 16-bit bus space • The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility	• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. • Capacity of each area: 16 Mbytes (CS0 to CS3) • A chip-select signal (CS0# to CS3#) can be output for each area. • Each area is specifiable as an 8-bit or 16-bit bus space • The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
Memory protection unit	Not available	Available
DMA controller	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
Data transfer controller	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
General I/O ports	100-pin /64-pin /48-pin • I/O: 84/48/34 • Input: 1/1/1 • Pull-up resistors: 84/48/34 • Open-drain outputs: 53/35/26 • 5-V tolerance: 4/2*2/2	100-pin /64-pin /48-pin • I/O: 79/43/30 (RX231 Group) 83/47/34 (RX230 Group) • Input: 1/1/1 • Pull-up resistors: 79/43/30(RX231 Group) 83/47/34 (RX230 Group) • Open-drain outputs: 58/34/26 • 5-V tolerance: 8/5/5
Event link controller	• Event signals of 59 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B and port E	• Event signals of 63 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B and port E
Multi-function pin controller	Capable of selecting the input/output function from multiple pins	Capable of selecting the input/output function from multiple pins

Item		RX210	RX230 and RX231
Timers	16-bit timer pulse unit	Not available (available in products with 144 or more pins)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2	Controls the high-impedance state of the MTU's waveform output pins	Controls the high-impedance state of the MTU's waveform output pins

Item		RX210	RX230 and RX231
	8-bit timer	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Realtime clock	RTCb • Clock source: Sub-clock • Time/calendar • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values	RTCe • Clock source: Sub-clock • Time/calendar • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values

Item		RX210	RX230 and RX231
Communication function	Serial communications interfaces	• 7 channels (SCI0, 1, 5, 6, 8, 9, 12) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12) — • Simple I²C • Simple SPI — — • Event linking by the ELC (only on channel 5) • Start frame and information frame are included (SCI12)	• 7 channels (SCI0, 1, 5, 6, 8, 9, 12) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 • Start-bit detection: Level or edge detection is selectable. • Simple I²C • Simple SPI • 9-bit transfer mode • Bit rate modulation • Event linking by the ELC (only on channel 5) • Supports the serial communications protocol, which contains the start frame and information frame (SCI12)
	I²C bus interface	• 1 channel • Communications formats: I²C bus format/SMBus format • Master/slave selectable • Supports the fast mode	• 1 channel • Communications formats: I²C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode

Item		RX210	RX230 and RX231
	Serial peripheral interface	RSPI • 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception	RSPIa • 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
Communication function	IrDA interface	Not available	• 1 channel (SCI5 used) • Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	USB 2.0 host/function module	Not available	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated.*3 • Host/function module: 1 port • Compliant with USB version 2.0 • Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) • OTG (ON-The-Go) is supported. • Isochronous transfer is supported. • BC (Battery Charger) is supported.
	CAN module	Not available	• 1 channel*3 • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 message boxes

Item		RX210	RX230 and RX231
	Serial sound interface	Not available	• 1 channel*3 • Capable of duplex communications • Various serial audio formats supported • Master/slave function supported • Programmable word clock or bit clock generation function • 8/16/18/20/22/24/32-bit data formats supported • On-chip 8-stage FIFO for transmission/reception • Supports WS continue mode in which the SSIWS signal is not stopped.
	SD host interface	Not available	Available*3
Security functions		Not available	Available*3
A/D converter		• 12 bits (16 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel (in operation with ADCLK at 50 MHz) • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) — • Sample-and-hold function — • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC	• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 0.83 μs per channel when the ADCLK is operating at 54 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Detection of analog input disconnection • Double trigger mode (A/D conversion data duplicated) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU, TPU), an external trigger signal, or ELC
Temperature sensor		• 1 channel • Temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA). • Module stop state can be set.	• 1 channel • The temperature sensor outputs a voltage to the 12-bit A/D converter via a gain amplifier. —

Item	RX210	RX230 and RX231
D/A converter	• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH	• 2 channels • 12-bit resolution • Output voltage: 0.4 to AVCC0 – 0.5 V
CRC calculator	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator A	• 2 channels • Comparison of reference voltage and analog input voltage	Not available
Comparator B	• 2 channels × 1 unit • Comparison of reference voltage and analog input voltage —	• 2 channels × 2 units • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit	Not available	Detection pin: 24 channels
Data Operation Circuit	• Comparison, addition, and subtraction of 16-bit data • Module stop state can be set. • Data operation circuit interrupt request —	• Comparison, addition, and subtraction of 16-bit data • Module stop state can be set. • Data operation circuit interrupt request • Event link function
Power supply voltages/Operating frequencies	VCC = 1.62 to 1.8 V: 20 MHz VCC = 1.8 to 2.7 V: 32 MHz VCC = 2.7 to 5.5 V: 50 MHz	VCC = 1.8 to 2.4 V: 8 MHz VCC = 2.4 to 2.7 V: 16 MHz VCC = 2.7 to 5.5 V: 54 MHz
Operating temperature	D version: -40 to +85 °C G version: -40 to +105 °C	D version: -40 to +85°C G version: -40 to +105°C
Connection to the VCL pin	Connect the VCL pin to the VSS pin via the 0.1 μF smoothing capacitor	Connect the VCL pin to the VSS pin via the 4.7 μF smoothing capacitor

Item	RX210	RX230 and RX231			
Packages		RX210			
		Chip Version			RX230 and RX231
	Package	A	B	C	
	100-pin TFLGA (PTLG0100KA-A) 5.5 × 5.5 mm, 0.5 mm pitch	—	○	—	○
	100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65 mm pitch	○	○	○	—
	100-pin LFQFP (PLQP0100KB-A) 14 × 14 mm, 0.50 mm pitch(previous code: 100-pin LQFP (PLQP0100KB-A))	○	○	○	○
	64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch	—	—	—	○
	64-pin TFLGA (PTLG0064JA-A) 6 × 6 mm, 0.65-mm pitch	—	○	—	—
	64-pin HWQFN (PWQN0064KC-A) 9 × 9 mm, 0.5 mm pitch	—	—	—	○
	64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.5 mm pitch (previous code: 64-pin LQFP (PLQP0064KB-A))	○	○	○	○
	64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch	—	○	○	—
	48-pin LFQFP (PLQP0048KB-A) 7 × 7 mm, 0.5 mm pitch (previous code: 48-pin LQFP (PLQP0048KB-A))	—	○	—	○
	48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch	—	—	—	○
	○: Available —: Not available				

Notes: 1. This mode is available only in chip version B. Chip versions A and C does not have this mode.
2. 1 for chip version A products listed below because P17 is not 5V tolerant in those products.
R5F52108ADFM, R5F52107ADFM, R5F52106ADFM, R5F52105ADFM
3. RX231 Group only. Not implemented on the RX230 Group.
4. When the BCLK pin is not used. When used: RX231 Group: 12.5MHz RX230 Group: 16MHz

4.2 Differences in Pin Functions

This section describes the differences in pin functions and pins for power supply, clocks, and system control.

Specifications that exist only in one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that have no difference between the two groups are indicated in black. Note that the RX230 Group is not equipped with USB, CAN, and SDHI modules, so it does not have the pins associated with them.

4.2.1 100-Pin Packages

Table 4.2 lists differences in the pin functions for the 100-pin package. Table 4.3 lists differences in pins for power supply, clocks and system control for the 100-pin package.

Table 4.2 Differences in the Pin Functions for the 100-Pin Package

I/O Port	RX210	RX230 and RX231
P03	DA0	DA0
P05	DA1	DA1
P07	ADTRG0#	ADTRG0#
P12	TMCI1, SCL, IRQ2	TMCI1, SCL, IRQ2
P13	MTIOC0B, TMO3, SDA, IRQ3	MTIOC0B, TMO3, TIOCA5, SDA, IRQ3
P14	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4	MTIOC3A, MTCLKA, TMRI2, TIOCB5, TCLKA, CTS1#, RTS1#, SS1#, CTXD0, USB0_OVRCURA, TS13, IRQ4, CVREFB2
P15	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5	MTIOC0B, MTCLKB, TMCI2, TIOCB2, TCLKB, RXD1, SMISO1, SSCL1, CRXD0, TS12, IRQ5, CMPB2
P16	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL-DS, IRQ6, RTCOUT, ADTRG0#	MTIOC3C, MTIOC3D, TMO2, TIOCB1, TCLKC, TXD1, SMOSI1, SSDA1, MOSIA, SCL, USB0_VBUS, USB0_VBUSEN, USB0_OVRCURB, IRQ6, RTCOUT, ADTRG0#
P17	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS, IRQ7	MTIOC3A, MTIOC3B, TMO1, POE8#, TIOCB0, TCLKD, SCK1, MISOA, SDA, SSITXD0, IRQ7, CMPOB2
P20	MTIOC1A, TMRI0, TXD0, SMOSI0, SSDA0	MTIOC1A, TMRI0, TIOCB3, TXD0, SMOSI0, SSDA0, USB0_ID, SSIRXD0, TS9
P21	MTIOC1B, TMCI0, RXD0, SMISO0, SSCL0	MTIOC1B, TMCI0, TIOCA3, RXD0, SMISO0, SSCL0, USB0_EXICEN, SSIWS0, TS8
P22	MTIOC3B, MTCLKC, TMO0, SCK0	MTIOC3B, MTCLKC, TMO0, TIOCC3, SCK0, USB0_OVRCURB, AUDIO_MCLK, TS7
P23	MTIOC3D, MTCLKD, CTS0#, RTS0#, SS0#	MTIOC3D, MTCLKD, TIOCD3, CTS0#, RTS0#, SS0#, SSISCK0, TS6
P24	CS0#, MTIOC4A, MTCLKA, TMRI1	CS0#, MTIOC4A, MTCLKA, TMRI1, TIOCB4, USB0_VBUSEN, TS5
P25	CS1#, MTIOC4C, MTCLKB, ADTRG0#	CS1#, MTIOC4C, MTCLKB, TIOCA4, TS4, ADTRG0#
P26	CS2#, MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1	CS2#, MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1, SSIRXD0, TS3, CMPB3
P27	CS3#, MTIOC2B, TMCI3, SCK1	CS3#, MTIOC2B, TMCI3, SCK1, SSIWS0, TS2, CVREFB3
P30	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0-DS, RTCIC0	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, AUDIO_MCLK, IRQ0, RTCIC0, CMPOB3
P31	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1-DS, RTCIC1	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, SSISCK0, IRQ1, RTCIC1

I/O Port	RX210	RX230 and RX231
P32	MTIOC0C, TMO3, TXD6, SMOSI6, SSDA6, IRQ2-DS, RTCOUT, RTCIC2	MTIOC0C, TMO3, TIOCC0, TXD6, SMOSI6, SSDA6, USB0_VBUSEN, IRQ2, RTCOUT, RTCIC2
P33	MTIOC0D, TMRI3, POE3#, RXD6, SMISO6, SSCL6, IRQ3-DS	MTIOC0D, TMRI3, POE3#, TIOCD0, RXD6, SMISO6, SSCL6, TS1, IRQ3
P34	MTIOC0A, TMCI3, POE2#, SCK6, IRQ4	MTIOC0A, TMCI3, POE2#, SCK6, TS0, IRQ4
P35	NMI	NMI
P36	—	—
P37	—	—
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P43	AN003	AN003
P44	AN004	AN004
P45	AN005	AN005
P46	AN006	AN006
P47	AN007	AN007
P50	WR0#, WR#	WR0#, WR#, TS20
P51	WR1#, BC1#, WAIT#	WR1#, BC1#, WAIT#, TS19
P52	RD#	RD#, TS18
P53	—	TS17
P54	ALE, MTIOC4B, TMCI1	ALE, MTIOC4B, TMCI1, CTXD0, TS16
P55	WAIT#, MTIOC4D, TMO3	WAIT#, MTIOC4D, TMO3, CRXD0, TS15
PA0	A0, BC0#, MTIOC4A, SSLA1, CACREF	A0, BC0#, MTIOC4A, TIOCA0, SSLA1, CACREF
PA1	A1, MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA	A1, MTIOC0B, MTCLKC, TIOCB0, SCK5, SSLA2, SSISCK0
PA2	A2, RXD5, SMISO5, SSCL5, SSLA3	A2, RXD5, SMISO5, SSCL5, SSLA3, IRRXD5
PA3	A3, MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6-DS, CMPB1	A3, MTIOC0D, MTCLKD, TIOCD0, TCLKB, RXD5, SMISO5, SSCL5, SSIRXD0, IRRXD5, IRQ6, CMPB1
PA4	A4, MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5-DS, CVREFB1	A4, MTIC5U, MTCLKA, TMRI0, TIOCA1, TXD5, SMOSI5, SSDA5, SSLA0, SSITXD0, IRTXD5, IRQ5, CVREFB1
PA5	A5, RSPCKA	A5, TIOCB1, RSPCKA
PA6	A6, MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA	A6, MTIC5V, MTCLKB, TMCI3, POE2#, TIOCA2, CTS5#, RTS5#, SS5#, MOSIA, SSIWS0
PA7	A7, MISOA	A7, TIOCB2, MISOA
PB0	A8, MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA	A8, MTIC5W, TIOCA3, RXD6, SMISO6, SSCL6, RSPCKA, SDHI_CMD
PB1	A9, MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4-DS	A9, MTIOC0C, MTIOC4C, TMCI0, TIOCB3, TXD6, SMOSI6, SSDA6, SDHI_CLK, IRQ4, CMPOB1
PB2	A10, CTS6#, RTS6#, SS6#	A10, TIOCC3, TCLKC, CTS6#, RTS6#, SS6#
PB3	A11, MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	A11, MTIOC0A, MTIOC4A, TMO0, POE3#, TIOCD3, TCLKD, SCK6, SDHI_WP
PB4	A12, CTS9#, RTS9#, SS9#	A12, TIOCA4, CTS9#, RTS9#, SS9#
PB5	A13, MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9	A13, MTIOC2A, MTIOC1B, TMRI1, POE1#, TIOCB4, SCK9, USB0_VBUS, SDHI_CD
PB6	A14, MTIOC3D, RXD9, SMISO9, SSCL9	A14, MTIOC3D, TIOCA5, RXD9, SMISO9, SSCL9, SDHI_D1

I/O Port	RX210	RX230 and RX231
PB7	A15, MTIOC3B, TXD9, SMOSI9, SSDA9	A15, MTIOC3B, TIOCB5, TXD9, SMOSI9, SSDA9, SDHI_D2
PC0	A16, MTIOC3C, CTS5#, RTS5#, SS5#, SSLA1	A16, MTIOC3C, TCLKC, CTS5#, RTS5#, SS5#, SSLA1, TS35
PC1	A17, MTIOC3A, SCK5, SSLA2	A17, MTIOC3A, TCLKD, SCK5, SSLA2, TS33
PC2	A18, MTIOC4B, RXD5, SMISO5, SSCL5, SSLA3	A18, MTIOC4B, TCLKA, RXD5, SMISO5, SSCL5, SSLA3, IRRXD5, SDHI_D3, TS30
PC3	A19, MTIOC4D, TXD5, SMOSI5, SSDA5	A19, MTIOC4D, TCLKB, TXD5, SMOSI5, SSDA5, IRTXD5, SDHI_D0, TS27
PC4	A20, CS3#, MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0	A20, CS3#, MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0, SDHI_D1, TSCAP
PC5	A21, CS2#, WAIT#, MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA	A21, CS2#, WAIT#, MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA, TS23
PC6	A22, CS1#, MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA	A22, CS1#, MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA, TS22
PC7	A23, CS0#, MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF	A23, CS0#, MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF
PD0	D0[A0, D0], IRQ0	D0[A0, D0], IRQ0, AN024
PD1	D1[A1, D1], MTIOC4B, IRQ1	D1[A1, D1], MTIOC4B, IRQ1, AN025
PD2	D2[A2, D2], MTIOC4D, IRQ2	D2[A2, D2], MTIOC4D, IRQ2, AN026
PD3	D3[A3, D3], POE8#, IRQ3	D3[A3, D3], POE8#, IRQ3, AN027
PD4	D4[A4, D4], POE3#, IRQ4	D4[A4, D4], POE3#, IRQ4, AN028
PD5	D5[A5, D5], MTIC5W, POE2#, IRQ5	D5[A5, D5], MTIC5W, POE2#, IRQ5, AN029
PD6	D6[A6, D6], MTIC5V, POE1#, IRQ6	D6[A6, D6], MTIC5V, POE1#, IRQ6, AN030
PD7	D7[A7, D7], MTIC5U, POE0#, IRQ7	D7[A7, D7], MTIC5U, POE0#, IRQ7, AN031
PE0	D8[A8, D8], SCK12, AN008	D8[A8, D8], SCK12, AN016
PE1	D9[A9, D9], MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN009, CMPB0	D9[A9, D9], MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN017, CMPB0
PE2	D10[A10, D10], MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7-DS, AN010, CVREFB0	D10[A10, D10], MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN018, CVREFB0
PE3	D11[A11, D11], MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN011, CMPA1	D11[A11, D11], MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AUDIO_MCLK, AN019, CLKOUT
PE4	D12[A12, D12], MTIOC4D, MTIOC1A, AN012, CMPA2	D12[A12, D12], MTIOC4D, MTIOC1A, AN020, CMPA2, CLKOUT
PE5	D13[A13, D13], MTIOC4C, MTIOC2B, IRQ5, AN013	D13[A13, D13], MTIOC4C, MTIOC2B, IRQ5, AN021, CMPOB0
PE6	D14[A14, D14], IRQ6, AN014	D14[A14, D14], IRQ6, AN022
PE7	D15[A15, D15], IRQ7, AN015	D15[A15, D15], IRQ7, AN023
PH0	CACREF	— (No I/O port on RX231 only)
PH1	TMO0, IRQ0	— (No I/O port on RX231 only)
PH2	TMRI0, IRQ1	— (No I/O port on RX231 only)
PH3	TMCI0	— (No I/O port on RX231 only)
PJ1	MTIOC3A	— (No I/O port)
PJ3	MTIOC3C, CTS6#, RTS6#, SS6#	MTIOC3C, CTS6#, RTS6#, SS6#

Table 4.3 Differences in Pins for Power Supply, Clocks, and System Control for the 100-Pin Package

Pin Number				
QFP	**LGA**	**RX210**	**RX230**	**RX231**
1	A2	VREFH	VREFH	VREFH
3	C2	VREFL	VREFL	VREFL
5	C1	VCL	VCL	VCL
6	D4	— (PJ1)	VBATT	VBATT
7	D3	MD, FINED	MD, FINED	MD, FINED
8	D1	XCIN	XCIN	XCIN
9	D2	XCOUT	XCOUT	XCOUT
10	E3	RES#	RES#	RES#
11	E1	XTAL	XTAL	XTAL
12, 62	E2, F10	VSS	VSS	VSS
13	F1	EXTAL	EXTAL	EXTAL
14, 60	F2, G10	VCC	VCC	VCC
35	J6	— (PH3)	— (PH3)	VCC_USB
36	K5	— (PH2)	— (PH2)	USB0_DM
37	K6	— (PH1)	— (PH1)	USB0_DP
38	J5	— (PH0)	— (PH0)	VSS_USB
41	G5	BCLK	BCLK	BCLK
45	H7	— (PC7)	— (PC7)	UB (PC7)
94	A4	VREFL0	VREFL0	VREFL0
96	C4	VREFH0	VREFH0	VREFH0
97	B3	AVCC0	AVCC0	AVCC0
99	B2	AVSS0	AVSS0	AVSS0

4.2.2 64-Pin Packages

Table 4.4 lists differences in the pin functions for the 64-pin package. Table 4.5 lists differences in pins for power supply, clocks and system control for the 64-pin package.

Table 4.4 Differences in the Pin Functions for the 64-Pin Package

I/O Port	RX210	RX230 and RX231
P03	DA0	DA0
P05	DA1	DA1
P14	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4	MTIOC3A, MTCLKA, TMRI2, TIOCB5, TCLKA, CTS1#, RTS1#, SS1#, CTXD0, USB0_OVRCURA, TS13, IRQ4, CVREFB2
P15	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5	MTIOC0B, MTCLKB, TMCI2, TIOCB2, TCLKB, RXD1, SMISO1, SSCL1, CRXD0, TS12, IRQ5, CMPB2
P16	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL-DS, IRQ6, RTCOUT, ADTRG0#	MTIOC3C, MTIOC3D, TMO2, TIOCB1, TCLKC, TXD1, SMOSI1, SSDA1, MOSIA, SCL, USB0_VBUS, USB0_VBUSEN, USB0_OVRCURB, IRQ6, RTCOUT, ADTRG0#
P17	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS, IRQ7	MTIOC3A, MTIOC3B, TMO1, POE8#, TIOCB0, TCLKD, SCK1, MISOA, SDA, SSITXD0, IRQ7, CMPOB2
P26	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1, USB0_VBUSEN, SSIRXD0, TS3, CMPB3
P27	MTIOC2B, TMCI3, SCK1	MTIOC2B, TMCI3, SCK1, SSIWS0, TS2, CVREFB3
P30	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0-DS, RTCIC0	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, AUDIO_MCLK, IRQ0, RTCIC0, CMPOB3
P31	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1-DS, RTCIC1	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, SSISCK0, IRQ1, RTCIC1
P32	MTIOC0C, TMO3, TXD6, SMOSI6, SSDA6, IRQ2-DS, RTCOUT, RTCIC2	— (No I/O port)
P35	NMI	NMI
P36	—	—
P37	—	—
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P43	AN003	AN003
P44	AN004	AN004
P46	AN006	AN006
P54	MTIOC4B, TMCI1	MTIOC4B, TMCI1, CTXD0, TS16
P55	MTIOC4D, TMO3	MTIOC4D, TMO3, CRXD0, TS15
PA0	MTIOC4A, SSLA1, CACREF	MTIOC4A, TIOCA0, SSLA1, CACREF
PA1	MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA	MTIOC0B, MTCLKC, TIOCB0, SCK5, SSLA2, SSISCK0
PA3	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6-DS, CMPB1	MTIOC0D, MTCLKD, TIOCD0, TCLKB, RXD5, SMISO5, SSCL5, SSIRXD0, IRRXD5, IRQ6, CMPB1

I/O Port	RX210	RX230 and RX231
PA4	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5-DS, CVREFB1	MTIC5U, MTCLKA, TMRI0, TIOCA1, TXD5, SMOSI5, SSDA5, SSLA0, SSITXD0, IRTXD5, IRQ5, CVREFB1
PA6	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA	MTIC5V, MTCLKB, TMCI3, POE2#, TIOCA2, CTS5#, RTS5#, SS5#, MOSIA, SSIWS0
PB0	MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA	MTIC5W, TIOCA3, RXD6, SMISO6, SSCL6, RSPCKA, SDHI_CMD
PB1	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4-DS	MTIOC0C, MTIOC4C, TMCI0, TIOCB3, TXD6, SMOSI6, SSDA6, SDHI_CLK, IRQ4, CMPOB1
PB3	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, TMO0, POE3#, TIOCD3, TCLKD, SCK6, SDHI_WP
PB5	MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9	MTIOC2A, MTIOC1B, TMRI1, POE1#, TIOCB4, SCK9, SDHI_CD
PB6	MTIOC3D, RXD9, SMISO9, SSCL9	MTIOC3D, TIOCA5, RXD9, SMISO9, SSCL9, SDHI_D1
PB7	MTIOC3B, TXD9, SMOSI9, SSDA9	MTIOC3B, TIOCB5, TXD9, SMOSI9, SSDA9, SDHI_D2
PC2	MTIOC4B, RXD5, SMISO5, SSCL5, SSLA3	MTIOC4B, TCLKA, RXD5, SMISO5, SSCL5, SSLA3, IRRXD5, SDHI_D3,TS30
PC3	MTIOC4D, TXD5, SMOSI5, SSDA5	MTIOC4D, TCLKB, TXD5, SMOSI5, SSDA5, IRTXD5, SDHI_D0, TS27,
PC4	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0, SDHI_D1, TSCAP
PC5	MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA	MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA, USB0_ID, TS23
PC6	MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA	MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA, USB0_EXICEN, TS22
PC7	MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF	MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF
PE0	SCK12, AN008	SCK12, AN016
PE1	MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN009, CMPB0	MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN017, CMPB0
PE2	MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7-DS, AN010, CVREFB0	MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN018, CVREFB0
PE3	MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN011, CMPA1	MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AUDIO_MCLK, AN019, CLKOUT
PE4	MTIOC4D, MTIOC1A, AN012, CMPA2	MTIOC4D, MTIOC1A, AN020, CMPA2, CLKOUT
PE5	MTIOC4C, MTIOC2B, IRQ5, AN013	MTIOC4C, MTIOC2B, IRQ5, AN021, CMPOB0
PH0	CACREF	— (No I/O port on RX231 only)
PH1	TMO0, IRQ0	— (No I/O port on RX231 only)
PH2	TMRI0, IRQ1	— (No I/O port on RX231 only)
PH3	TMCI0	— (No I/O port on RX231 only)

Table 4.5 Differences in Power Supply, Clock, and System Control Pins for the 64-Pin Package

Pin Number				
QFP	**LGA**	**RX210**	**RX230**	**RX231**
2	B1	VCL	VCL	VCL
3	C2	MD, FINED	MD, FINED	MD, FINED
4	C1	XCIN	XCIN	XCIN
5	D1	XCOUT	XCOUT	XCOUT
6	D2	RES#	RES#	RES#
7	H1	XTAL	XTAL	XTAL
8, 40	E1, E7	VSS	VSS	VSS
9	G2	EXTAL	EXTAL	EXTAL
10, 38	E6, F1	VCC	VCC	VCC
12	E2	— (P32)	VBATT	VBATT
21	G3	— (PH3)	— (PH3)	VCC_USB
22	H3	— (PH2)	— (PH2)	USB0_DM
23	H4	— (PH1)	— (PH1)	USB0_DP
24	G4	— (PH0)	— (PH0)	VSS_USB
27	G5	— (PC7)	— (PC7)	UB (PC7)
52	A6	VREFL	VREFL	VREFL
54	A5	VREFH	VREFH	VREFH
59	A4	VREFL0	VREFL0	VREFL0
61	A3	VREFH0	VREFH0	VREFH0
62	A2	AVCC0	AVCC0	AVCC0
64	B2	AVSS0	AVSS0	AVSS0

4.2.3 48-Pin Packages

Table 4.6 lists differences in the pin functions for the 48-pin package. Table 4.7 lists Differences in pins for power supply, clocks and system control for the 48-pin package.

Table 4.6 Differences in the Pin Functions for the 48-Pin Package

I/O Port	RX210	RX230 and RX231
P14	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4	MTIOC3A, MTCLKA, TMRI2, TIOCB5, TCLKA, CTS1#, RTS1#, SS1#, CTXD0, USB0_OVRCURA, TS13, IRQ4, CVREFB2
P15	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5	MTIOC0B, MTCLKB, TMCI2, TIOCB2, TCLKB, RXD1, SMISO1, SSCL1, CRXD0, TS12, IRQ5, CMPB2
P16	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL-DS, IRQ6, ADTRG0#	MTIOC3C, MTIOC3D, TMO2, TIOCB1, TCLKC, TXD1, SMOSI1, SSDA1, MOSIA, SCL, IRQ6, ADTRG0#
P17	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS, IRQ7	MTIOC3A, MTIOC3B, TMO1, POE8#, TIOCB0, TCLKD, SCK1, MISOA, SDA, SSITXD0, IRQ7, CMPOB2
P26	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1, USB0_VBUSEN, SSIRXD0, TS3, CMPB3
P27	MTIOC2B, TMCI3, SCK1	MTIOC2B, TMCI3, SCK1, SSIWS0, TS2, CVREFB3
P30	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0-DS	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, AUDIO_MCLK, IRQ0, CMPOB3
P31	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1-DS	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, SSISCK0, IRQ1
P35	NMI	NMI
P36	—	—
P37	—	—
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P46	AN006	AN006
PA1	MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA	MTIOC0B, MTCLKC, TIOCB0, SCK5, SSLA2, SSISCK0
PA3	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6-DS, CMPB1	MTIOC0D, MTCLKD, TIOCD0, TCLKB, RXD5, SMISO5, SSCL5, SSIRXD0, IRRXD5, IRQ6, CMPB1
PA4	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5-DS, CVREFB1	MTIC5U, MTCLKA, TMRI0, TIOCA1, TXD5, SMOSI5, SSDA5, SSLA0, SSITXD0, IRTXD5, IRQ5, CVREFB1
PA6	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA	MTIC5V, MTCLKB, TMCI3, POE2#, TIOCA2, CTS5#, RTS5#, SS5#, MOSIA, SSIWS0
PB0	MTIC5W,RXD6, SMISO6, SSCL6, RSPCKA	MTIC5W, TIOCA3, RXD6, SMISO6, SSCL6, RSPCKA
PB1	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4-DS	MTIOC0C, MTIOC4C, TMCI0, TIOCB3, TXD6, SMOSI6, SSDA6, IRQ4, CMPOB1
PB3	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, TMO0, POE3#, TIOCD3, TCLKD, SCK6
PB5	MTIOC2A, MTIOC1B, TMRI1, POE1#,	MTIOC2A, MTIOC1B, TMRI1, POE1#, TIOCB4

I/O Port	RX210	RX230 and RX231
PC4	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0, TSCAP
PC5	MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA	MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA, USB0_ID, TS23
PC6	MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA	MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA, USB0_EXICEN, TS22
PC7	MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF	MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF
PE1	MTIOC4C, TXD12, TXDX12, SIOX12, SSDA12, AN009, CMPB0	MTIOC4C, TXD12, TXDX12, SIOX12, SSDA12, AN017, CMPB0
PE2	MTIOC4A, RXD12, RXDX12, SSCL12, IRQ7-DS, AN010, CVREFB0	MTIOC4A, RXD12, RXDX12, SSCL12, IRQ7, AN018, CVREFB0
PE3	MTIOC4B, POE8#, CTS12#, RTS12#, AN011, CMPA1	MTIOC4B, POE8#, CTS12#, RTS12#, AUDIO_MCLK, AN019, CLKOUT
PE4	MTIOC4D, MTIOC1A, AN012, CMPA2	MTIOC4D, MTIOC1A, AN020, CMPA2, CLKOUT
PH0	CACREF	— (No I/O port on RX231 only)
PH1	TMO0,IRQ0	— (No I/O port on RX231 only)
PH2	TMRI0,IRQ1	— (No I/O port on RX231 only)
PH3	TMCI0	— (No I/O port on RX231 only)

Table 4.7 Differences in Power Supply, Clock, and System Control Pins for the 48-Pin Package

Pin Number (QFP)	RX210	RX230	RX231
1	VCL	VCL	VCL
2	MD, FINED	MD, FINED	MD, FINED
3	RES#	RES#	RES#
4	XTAL	XTAL	XTAL
5, 30	VSS	VSS	VSS
6	EXTAL	EXTAL	EXTAL
7, 28	VCC	VCC	VCC
17	— (PH3)	— (PH3)	VCC_USB
18	— (PH2)	— (PH2)	USB0_DM
19	— (PH1)	— (PH1)	USB0_DP
20	— (PH0)	— (PH0)	VSS_USB
21	— (PC7)	— (PC7)	UB (PC7)
39	VREFL	VREFL	VREFL
41	VREFH	VREFH	VREFH
44	VREFL0	VREFL0	VREFL0
46	VREFH0	VREFH0	VREFH0
47	AVCC0	AVCC0	AVCC0
48	AVSS0	AVSS0	AVSS0

4.3 Differences in Modules and Functions

Table 4.8 lists the differences in modules and functions. This table describes the differences in the maximum specifications for the 100-pin package. Refer to 4.4 differences in details on specifications and User's Manual: Hardware listed in 5 Reference Documents for details on the differences in modules and functions.

Table 4.8 Differences in Modules and Functions

No.	Module or Function Name	RX210	RX230	RX231
1	CPU	Δ	Δ	Δ
2	Operating modes	Δ	Δ	Δ
3	Address Space	Δ	Δ	Δ
4	Resets	Δ	Δ	Δ
5	Option-setting memory	Δ	Δ	Δ
6	Voltage detection circuit (LVDAa/LVDAb)	Δ	Δ	Δ
7	Clock generation circuit	Δ	Δ	Δ
8	Clock frequency accuracy measurement circuit (CAC)	Δ	Δ	Δ
9	Low power consumption	Δ	Δ	Δ
10	Battery backup function	—	○	○
11	Register write protection function	Δ	Δ	Δ
12	Exception handling	Δ	Δ	Δ
13	Interrupt controller (ICUb)	Δ	Δ	Δ
14	Buses	Δ	Δ	Δ
15	Memory-protection unit (MPU)	—	○	○
16	DMA controller (DMACA)	◎	◎	◎
17	Data transfer controller (DTCa)	Δ	Δ	Δ
18	Event link controller (ELC)	Δ	Δ	Δ
19	I/O ports	Δ	Δ	Δ
20	Multi-function pin controller (MPC)	Δ	Δ	Δ
21	Multi-function timer pulse unit 2 (MTU2a)	◎	◎	◎
22	Port output enable 2 (POE2a)	◎	◎	◎
23	16-bit timer pulse unit (TPUa)	—	○	○
24	8-bit timer (TMR)	◎	◎	◎
25	Compare match timer (CMT)	◎	◎	◎
26	Realtime clock (RTCb/RTCe)	Δ	Δ	Δ
27	Low-power timer (LPT)	—	○	○
28	Watchdog timer (WDTA)	◎	◎	◎
29	Independent watchdog timer (IWDTa)	Δ	Δ	Δ
30	USB 2.0 host/function module (USBd)	—	—	○
31	Serial communications interface (SCIc, SCId/SCIg, SCIh)	Δ	Δ	Δ
32	IrDA interface	—	○	○
33	I^2C bus interface (RIIC/RIICa)	Δ	Δ	Δ
34	CAN interface (RSCAN)	—	—	○
35	Serial sound interface (SSI)	—	○	○
36	Serial peripheral interface (RSPI/RSPIa)	Δ	Δ	Δ
37	CRC calculator (CRC)	◎	◎	◎
38	SD host interface (SDHIa)	—	—	○
39	Security functions	—	—	○
40	Capacitive touch sensing unit (CTSU)	—	○	○
41	A/D converter (S12ADb/S12ADE)	Δ	Δ	Δ
42	D/A converter (DA/R12DAA)	Δ	Δ	Δ

No.	Module or Function Name	RX210	RX230	RX231
43	Temperature sensor (TEMPSA)	Δ	Δ	Δ
44	Comparator A (CMPA)	○	—	—
45	Comparator B (CMPB/CMPBa)	Δ	Δ	Δ
46	Data operation circuit (DOC)	Δ	Δ	Δ
47	RAM	◎	◎	◎
48	ROM (flash memory for code storage)	Δ	Δ	Δ
49	E2 DataFlash Memory (flash memory for data storage)	Δ	Δ	Δ
50	Package (LFQFP48/64/100 only)	Δ	Δ	Δ

Legend

◎: All groups have this module or function.

○ or —: Not all groups have this module or function.
○ means that the module or function is available on the group indicated.
— means that the module or function is not available on the group indicated.

Δ: All groups have this module or function, but the specifications differ between groups.
Where the module symbols differ, indications are as follows: Module or symbol name (symbol for RX210/symbol for RX231).

4.4 Differences in Details on Specifications

This section describes differences in details of specifications. Specifications that exist only in one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that have no difference between the two groups are not described.

4.4.1 CPU

Table 4.9 lists differences in the CPU.

Table 4.9 Differences in the CPU

Item	RX210	RX230 and RX231
Instruction set architecture	RXv1	RXv2
Register set	• 16 general-purpose registers (32 bits) • 8 control registers (32 bits) Interrupt stack pointer (ISP) User stack pointer (USP) — Interrupt table register (INTB) Program counter (PC) Processor status word (PSW) Backup PC (BPC) Backup PSW (BPSW) Fast interrupt vector register (FINTV) — • 1 accumulator (64 bits) in single-chip mode (ACC)	• 16 general-purpose registers (32 bits) • 10 control registers (32 bits) Interrupt stack pointer (ISP) User stack pointer (USP) Exception table register (EXTB) Interrupt table register (INTB) Program counter (PC) Processor status word (PSW) Backup PC (BPC) Backup PSW (BPSW) Fast interrupt vector register (FINTV) Floating-point status word (FPSW) • 2 accumulator (72 bits) in single-chip mode (ACC0, ACC1)
Addressing modes	10 addressing modes: Immediate Register direct Register indirect Register relative Post-increment register indirect Pre-decrement register indirect Indexed register indirect Control register direct PSW direct Program counter relative —	10 modes Immediate Register direct Register indirect Register relative Post-increment register indirect Pre-decrement register indirect Indexed register indirect Control register direct PSW direct Program counter relative Accumulator direct
Basic instructions	73 basic instructions — —	75 basic instructions Storing with LI flag clear (MOVCO) Loading with LI flag set (MOVLI)

Item	RX210	RX230 and RX231
Floating-point instructions	—	11 floating-point instructions Floating-point addition (FADD) Floating-point comparison (FCMP) Floating-point division (FDIV) Floating-point multiplication (FMUL) Floating-point square root (FSQRT) Floating-point subtraction (FSUB) Floating point to integer conversion (FTOI) Floating point to integer conversion (FTOU) Integer to floating-point conversion (ITOF) Conversion from floating-point to integer (ROUND) Integer to floating-point conversion (UTOF)
DSP instructions	9 DSP instructions Multiply-Accumulate the high-order word (MACHI) Multiply-Accumulate the low-order word (MACLO) Multiply the high-order word (MULHI) Multiply the low-order word (MULLO) Move the high-order longword from accumulator (MVFACHI) Move the middle-order longword from accumulator (MVFACMI) Move the high-order longword to accumulator (MVTACHI) Move the low-order longword to accumulator (MVTACLO) Round the accumulator word (RACW) — — — — — — — — — — — — —	23 DSP instructions Multiply-Accumulate the high-order word (MACHI) Multiply-Accumulate the low-order word (MACLO) Multiply the high-order word (MULHI) Multiply the low-order word (MULLO) Move the high-order longword from accumulator (MVFACHI) Move the middle-order longword from accumulator (MVFACMI) Move the high-order longword to accumulator (MVTACHI) Move the low-order longword to accumulator (MVTACLO) Round the accumulator word (RACW) Extend multiply-accumulate to the accumulator (EMACA) Extended multiply-subtract to the accumulator (EMSBA) Extended multiply to the accumulator (EMULA) Multiply-Accumulate the lower-order word and higher-order word (MACLH) Multiply-Subtract the higher-order word (MSBHI) Multiply-Subtract the lower-order word and higher-order word (MSBLH) Multiply-Subtract the lower-order word (MSBLO) Multiply lower-order word and higher order word (MULLH) Move the guard longword from the accumulator (MVFACGU) Move the lower-order longword from the accumulator (MVFACLO) Move the guard longword to the accumulator (MVTACGU) Round the accumulator longword (RACL) Round the accumulator longword (RDACL) Round the accumulator word (RDACW)

Item	RX210	RX230 and RX231
Vector table	• Fixed vector table • Relocatable vector table	• Exception vector table • Interrupt vector table
Memory protection unit	—	Available

4.4.2 Operating Modes

Table 4.10 lists the differences in operating modes. Table 4.11 lists the difference in the I/O register related to operating modes.

Table 4.10 Differences in Operating Modes

Item	RX210	RX230 and RX231
Types of operating modes	• Single-chip mode • Boot mode The SCI is used. — • User boot mode • On-chip ROM enabled expansion mode • On-chip ROM disabled expansion mode	• Single-chip mode • Boot mode SCI interface USB interface* — • On-chip ROM enabled expansion mode • On-chip ROM disabled expansion mode
Pins for setting a mode	MD, PC7	MD, UB (PC7)

Note: * Available on the RX231 Group only. Not implemented on the RX230 Group.

Table 4.11 Difference in the I/O Register Related to Operating Modes

Register Symbol	Bit Symbol	RX210	RX230 and RX231
MDSR	—	Mode status register	Not available

4.4.3 Address Space

Figure 4.1 to Figure 4.3 shows the memory maps in the respective operating modes.

Figure 4.1 Memory Map in Each Operating Mode (Single-chip mode)

Figure 4.2 Memory Map in Each Operating Mode (On-chip ROM enabled extended mode)

Figure 4.3 Memory Map in Each Operating Mode (On-chip ROM disabled extended mode)

4.4.4 Resets

Table 4.12 lists the differences in resets. Table 4.13 lists the difference in the I/O register related to resets.

Table 4.12 Differences in Resets

Item	RX210	RX230 and RX231
Types of resets	RES# pin reset Power-on reset Voltage monitoring 0 reset Voltage monitoring 1 reset Voltage monitoring 2 reset Deep software standby reset Independent watchdog timer reset Watchdog timer reset Software reset	RES# pin reset Power-on reset Voltage monitoring 0 reset Voltage monitoring 1 reset Voltage monitoring 2 reset — Independent watchdog timer reset Watchdog timer reset Software reset

Table 4.13 Difference in the I/O Register Related to Resets

Register Symbol	Bit Symbol	RX210	RX230 and RX231
RSTSR0	DPSRSTF	Deep software standby reset detect flag	Reserved

4.4.5 Option-Setting Memory

Table 4.14 lists the differences in the option-setting memory. Table 4.15 lists the differences in I/O registers related to the option-setting memory, and Figure 4.4 shows a comparative of the option-setting memory.

Table 4.14 Differences in the Option-Setting Memory

Item	RX210	RX230 and RX231
For user boot mode	UB code A UB code B Endian select register B	None
For single-chip mode	Endian select register S	Endian select register

Table 4.15 Differences in I/O Registers Related to the Option-Setting Memory

Register Symbol	Bit Symbol	RX210	RX230 and RX231
OFS0	IWDTTOPS [1:0]	IWDT timeout period select 00: 1024 cycles (03FFh) 01: 4096 cycles (0FFFh) 10: 8192 cycles (1FFFh) 11: 16384 cycles (3FFFh)	IWDT timeout period select 00: 128 cycles (007Fh) 01: 512 cycles (01FFh) 10: 1024 cycles (03FFh) 11: 2048 cycles (07FFh)
	IWDTSLCSTP	IWDT sleep mode count stop control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode	IWDT sleep mode count stop control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby mode, and deep sleep mode
OFS1	VDSEL[1:0]	Voltage detection 0 level select 00: 3.80 V is selected 01: 2.80 V is selected 10: 1.90 V is selected 11: 1.72 V is selected	Voltage detection 0 level select 00: 3.84 V is selected 01: 2.82 V is selected 10: 2.51 V is selected 11: 1.90 V is selected
	FASTSTUP	Reserved	Power-on fast startup time
MDEB	—	Endian select register B (for selecting endian in user boot mode)	Not available
MDES	—	Endian select register S (for selecting endian in single-chip mode)	Not available
MDE	—	Not available	Endian select register (for selecting endian in single-chip mode)

Figure 4.4 Comparative of Option-Setting Memory

4.4.6 Voltage Detection Circuit

Table 4.16 lists the differences in voltage detection circuits. Table 4.17 lists the differences in I/O registers related to voltage detection circuits.

Table 4.16 Differences in Voltage Detection Circuits

Item		RX210	RX230 and RX231
Voltage monitoring 0		Available	Available
Voltage monitoring 1	Detection voltage	Selectable from 16 levels	Selectable from 14 levels
Voltage monitoring 2	Detection voltage	Selectable from 16 levels (varies according to whether VCC or the CMPA2 pin input voltage is selected)	Selectable from 4 levels (same whether VCC or the CMPA2 pin input voltage is selected)
Digital filter		Voltage monitoring 1, voltage monitoring 2	Not available
Comparator A		Available	Not available

Table 4.17 Differences in I/O Registers Related to Voltage Detection Circuits

Register Symbol	Bit Symbol	RX210	RX230 and RX231
LVD1CR1	LVD1IDTSEL [1:0]	Voltage Monitoring 1/Comparator A1 Interrupt/ELC Event Generation Condition Select b1 b0 0 0: When VCC ≥ Vdet1 (rise) is detected 0 1: When VCC < Vdet1 (drop) is detected 1 0: When drop and rise are detected 1 1: Do not set	Voltage Monitoring 1 Interrupt ELC Event Generation Condition Select b1 b0 0 0: When VCC ≥ Vdet1 (rise) is detected 0 1: When VCC < Vdet1 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited
	LVD1IRQSEL	Voltage Monitoring 1/Comparator A1 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt	Voltage Monitoring 1 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt
LVD1SR	LVD1DET	Voltage Monitoring 1/Comparator A1 Voltage Change Detection Flag 0: Not detected 1: Vdet1 passage detection	Voltage Monitoring 1 Voltage Change Detection Flag 0: Not detected 1: Vdet1 passage detection
	LVD1MON	Voltage Monitoring 1/Comparator A1 Signal Monitor Flag 0: VCC < Vdet1 1: VCC ≥ Vdet1 or LVD1MON is disabled	Voltage Monitoring 1 Signal Monitor Flag 0: VCC < Vdet1 1: VCC ≥ Vdet1 or LVD1MON circuit is disabled

Register Symbol	Bit Symbol	RX210	RX230 and RX231
LVD2CR1	LVD2IDTSEL [1:0]	Voltage Monitoring 2/Comparator A2 Interrupt/ELC Event Generation Condition Select b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Do not set	Voltage Monitoring 2 Interrupt ELC Event Generation Condition Select b1 b0 0 0: When VCC or the CMPA2 pin ≥ Vdet2 (rise) is detected 0 1: When VCC or the CMPA2 pin < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited
	LVD2IRQSEL	Voltage Monitoring 2/Comparator A2 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt	Voltage Monitoring 2 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt
LVD2SR	LVD2DET	Voltage Monitoring 2/Comparator A2 Voltage Change Detection Flag 0: Not detected 1: Vdet2 passage detection	Voltage Monitoring 2 Voltage Change Detection Flag 0: Not detected 1: Vdet2 passage detection
	LVD2MON	Voltage Monitoring 2/Comparator A2 Signal Monitor Flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled	Voltage Monitoring 2 Signal Monitor Flag 0: VCC or the CMPA2 pin < Vdet2 1: VCC or the CMPA2 pin ≥ Vdet2 or LVD2MON is disabled
LVCMPCR	EXVREFINP1	Comparator A1 reference voltage external input select	Reserved
	EXVCCINP1	Comparator A1 comparison voltage external input select	Reserved
	EXVREFINP2	Comparator A2 reference voltage external input select	Reserved
	LVD1E	Voltage Detection 1/Comparator A1 Enable 0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	Voltage Detection 1 Enable 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled
	LVD2E	Voltage Detection 2/Comparator A2 Enable 0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit enabled	Voltage Detection 2 Enable 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled

Register Symbol	Bit Symbol	RX210	RX230 and RX231
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select (standard voltage while the voltage is dropped) 0000: 4.15 V 0001: 4.00 V 0010: 3.85 V 0011: 3.70 V 0100: 3.55 V 0101: 3.40 V 0110: 3.25 V 0111: 3.10 V 1000: 2.95 V 1001: 2.80 V 1010: 2.65 V 1011: 2.50 V 1100: 2.35 V 1101: 2.20 V 1110: 2.05 V 1111: 1.90 V	Voltage detection 1 level select (standard voltage while the voltage is dropped) 0000: 4.29 V 0001: 4.14 V 0010: 4.02 V 0011: 3.84 V 0100: 3.10 V 0101: 3.00 V 0110: 2.90 V 0111: 2.79 V 1000: 2.68 V 1001: 2.58 V 1010: 2.48 V 1011: 2.20 V 1100: 1.96 V 1101: 1.86 V — —
LVDLVLR	RX230, RX231: LVD2LVL[1:0] RX210: LVD2LVL[3:0]	Voltage detection 2 level select (standard voltage while the voltage is dropped) • When LVCMPCR.EXVCCINP2 = 0 (VCC select) ([3:0]) 0000: 4.15 V 0001: 4.00 V 0010: 3.85 V 0011: 3.70 V 0100: 3.55 V 0101: 3.40 V 0110: 3.25 V 0111: 3.10 V 1000: 2.95 V 1001: 2.80 V 1010: 2.65 V 1011: 2.50 V 1100: 2.35 V 1101: 2.20 V 1110: 2.05 V 1111: 1.90 V • When LVCMPCR.EXVCCINP2 = 1 (CMPA2 pin select) ([3:0]) 0001: 1.33V	Voltage detection 2 level select (standard voltage while the voltage is dropped) ([1:0]) 00: 4.29 V 01: 4.14 V 10: 4.02 V 11: 3.84 V
LVD1CR0	LVD1RIE	Voltage Monitoring 1/Comparator A1 Interrupt/Reset Enable 0: Disabled 1: Enabled	Voltage Monitoring 1 Interrupt/Reset Enable 0: Disabled 1: Enabled

Register Symbol	Bit Symbol	RX210	RX230 and RX231
	LVD1DFDIS	Voltage monitoring 1/comparator A1 digital filter disable mode select	Reserved
	LVD1CMPE	Voltage Monitoring 1 Circuit/Comparator A1 Comparison Result Output Enable 0: Voltage monitoring 1 circuit comparison results output disable 1: Voltage monitoring 1 circuit comparison results output enable	Voltage Monitoring 1 Circuit Comparison Result Output Enable 0: Voltage monitoring 1 circuit comparison results output disabled 1: Voltage monitoring 1 circuit comparison results output enabled
	LVD1FSAMP [1:0]	Sampling clock select	Reserved
	LVD1RI	Voltage Monitoring 1 Circuit/Comparator A1 Mode Select 0: Voltage monitoring 1 interrupt enabled when Vdet1 is crossed 1: Voltage monitoring 1 reset enabled when the voltage falls to and below Vdet1	Voltage Monitoring 1 Circuit Mode Select 0: Voltage monitoring 1 interrupt occurs when the voltage passes Vdet1 1: Voltage monitoring 1 reset occurs when the voltage falls below Vdet1
	LVD1RN	Voltage Monitoring 1/Comparator A1 Reset Negation Select 0: Negation follows a stabilization time (tLVD1) after VCC > Vdet1 is detected. 1: Negation follows a stabilization time (tLVD1) after assertion of the LVD1 reset.	Voltage Monitoring 1 Reset Negation Select 0: Negation follows a stabilization time (tLVD1) after VCC > Vdet1 is detected. 1: Negation follows a stabilization time (tLVD1) after assertion of the voltage monitoring 1 reset.
LVD2CR0	LVD2RIE	Voltage Monitoring 2/Comparator A2 Interrupt/Reset Enable 0: Disabled 1: Enabled	Voltage Monitoring 2 Interrupt/Reset Enable 0: Disabled 1: Enabled
	LVD2DFDIS	Voltage monitoring 2/comparator A2 digital filter disable mode select	Reserved
	LVD2CMPE	Voltage Monitoring 2 Circuit/Comparator A2 Comparison Result Output Enable 0: Voltage monitoring 2 circuit comparison results output disable 1: Voltage monitoring 2 circuit comparison results output enable	Voltage Monitoring 2 Circuit Comparison Result Output Enable 0: Voltage monitoring 2 circuit comparison results output disabled 1: Voltage monitoring 2 circuit comparison results output enabled
	LVD2FSAMP [1:0]	Sampling clock select	Reserved

Register Symbol	Bit Symbol	RX210	RX230 and RX231
	LVD2RI	Voltage Monitoring 2 Circuit/Comparator A2 Mode Select 0: Voltage monitoring 2 interrupt enabled when Vdet2 is crossed 1: Voltage monitoring 2 reset enabled when the voltage falls to and below Vdet2	Voltage Monitoring 2 Circuit Mode Select 0: Voltage monitoring 2 interrupt occurs when the voltage passes Vdet2 1: Voltage monitoring 2 reset occurs when the voltage falls below Vdet2
	LVD1RN	Voltage Monitoring 2/Comparator A2 Reset Negation Select 0: Negation follows a stabilization time (tLVD2) after VCC > Vdet2 is detected. 1: Negation follows a stabilization time (tLVD2) after assertion of the LVD2 reset.	Voltage Monitoring 2 Reset Negation Select 0: Negation follows a stabilization time (tLVD2) after VCC or the CMPA2 pin > Vdet2 is detected. 1: Negation follows a stabilization time (tLVD2) after assertion of the voltage monitoring 2 reset.

4.4.7 Clock Generation Circuit

Table 4.18 lists the differences in the clock generation circuit. Table 4.19 lists the differences in I/O registers related to clock generation circuit.

Table 4.18 Differences in the Clock Generation Circuit

Item	RX210	RX230 and RX231
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB and PCLKD) to be supplied to peripheral modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
	—	• Generates the USB clock (UCLK) to be supplied to the USB.*
	—	• Generates the CAN clock (CANMCLK) to be supplied to the RSCAN.*
	—	• Generates the SSI clock (SSISCK) to be supplied to the SSI.*
	—	• Generates the LPT clock (LPTCLK) to be supplied to the LPT

Item	RX210	RX230 and RX231
Operating frequencies	ICLK: 50 MHz (max.) — PCLKB: 32 MHz (max.) PCLKD: 50 MHz (max.) FCLK: 4 MHz to 32 MHz (When P/E) BCLK: 25 MHz (max.) BCLK pin output: 12.5 MHz (max.) CACCLK: Same as frequency of each oscillator RTCSCLK: 32.768 kHz IWDTCLK: 125 kHz — — — —	ICLK: 54 MHz (max.) PCLKA: 54 MHz (max.) PCLKB: 32 MHz (max.) PCLKD: 54 MHz (max.) FCLK: 1 to 32 MHz (When P/E) BCLK: 32 MHz (max.) BCLK pin output: 16 MHz (max.) CACCLK: Same frequency as each oscillator RTCSCLK: 32.768 kHz IWDTCLK: 15 kHz UCLK: 48 MHz* CANCLK: 20 MHz (max.)* SSISCK: 20 MHz (max.)* LPTCLK: Same as clock of selected oscillator
Main clock oscillator	1 MHz to 20 MHz	1 MHz to 20 MHz (VCC ≥ 2.4 V) 1 MHz to 8 MHz (VCC < 2.4 V)
PLL circuit	• Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25 • VCO oscillation frequency: 50 MHz to 100 MHz	• Frequency multiplication ratio: Selectable from 4 to 13.5 (increments of 0.5) • VCO oscillation frequency: 24 MHz to 54 MHz (VCC ≥ 2.4 V)
Clocks that cannot be set to no division when using the PLL circuit	ICLK, BCLK, FCLK, PCLKB, PCLKD	None
USB-dedicated PLL circuit	Not available	Available*
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz, 36.864 MHz, 40 MHz, 50 MHz • HOCO power supply control	• Oscillation frequency: 32 MHz and 54 MHz —
Low-speed on-chip oscillator (LOCO)	125 kHz	4 MHz
IWDT-dedicated on-chip oscillator	125 kHz	15 kHz

Note: * Available on the RX231 Group only. Not implemented on the RX230 Group.

Table 4.19 Differences in I/O Registers Related to Clock Generation Circuit

Register Symbol	Bit Symbol	RX210	RX230 and RX231
SCKCR	PCKA[3:0]	Reserved	Peripheral module clock A (PCLKA) select
SCKCR3	CKSEL[2:0]	Clock Source Select 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator*1 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit	Clock Source Select 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit
VRCR	—	Voltage regulator control register	Not available
PLLCR	STC	Frequency multiplication factor select ([4:0]) 00111: ×8 — 01001: ×10 — 01011: ×12 — — — 01111: ×16 — — — 10011: ×20 — — — 10111: ×24 11000: ×25 — —	Frequency multiplication factor select ([5:0]) 000111: ×4 001000: ×4.5 001001: ×5 001010: ×5.5 001011: ×6 001100: ×6.5 001101: ×7 001110: ×7.5 001111: ×8 010000: ×8.5 010001: ×9 010010: ×9.5 010011: ×10 010100: ×10.5 010101: ×11 010110: ×11.5 010111: ×12 011000: ×12.5 011001: ×13 011010: ×13.5
UPLLCR	—	Not available	USB-dedicated PLL control register*2
UPLLCR2	—	Not available	USB-dedicated PLL control register 2*2
HOCOCR2	HCFRQ[1:0]	HOCO frequency setting 00: 32 MHz 01: 36.864 MHz 10: 40 MHz 11: 50 MHz	HOCO frequency setting 00: 32 MHz — — 11: 54 MHz
OSCOVFSR	—	Not available	Oscillation stabilization flag register
LOCOTRR	LOCOTRD [4:0]	Not available	Low-speed on-chip oscillator trimming register
ILOCOTRR	ILOCOTRD [4:0]	Not available	IWDT-dedicated on-chip oscillator trimming register
HOCOTRRn (n = 0 or 3)	HOCOTRD [5:0]	Not available	High-speed on-chip oscillator trimming register

Register Symbol	Bit Symbol	RX210	RX230 and RX231
MOFCR	MODRV [2:0]	Main clock oscillator drive capability switch	Reserved
	MODRV2 [1:0]	Main clock oscillator drive capability switch 2 01: 1 MHz to 8 MHz 10: 8.1 MHz to 15.9 MHz 11: 16 MHz to 20 MHz	—
	MODRV21	—	Main clock oscillator drive capability switch VCC ≥ 2.4 V 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited
HOCOPCR	—	High-speed on-chip oscillator power supply control register	Not available
PLLPCR*2	—	PLL power control register	Not available
CKOCR	—	Not available	CLKOUT output control register
MEMWAIT	—	Not available	Memory wait cycle setting register

Notes: 1. This can be selected in chip version B and C. This setting is not available in chip version A.
2. This register is available only in chip version B. Chip version A and C do not have this register.

4.4.8 Clock Frequency Accuracy Measurement Circuit

Table 4.20 lists the differences in clock frequency accuracy measurement circuit. Table 4.21 lists the differences in I/O registers related to the clock frequency accuracy measurement circuit.

Table 4.20 Differences in Clock Frequency Accuracy Measurement Circuit

Item	RX210	RX230 and RX231
Measurement target clocks	• Main clock* Sub-clock HOCO clock LOCO clock IWDTCLK clock —	Main clock Sub-clock HOCO clock LOCO clock IWDTCLK clock Peripheral module clock B (PCLKB)
Measurement reference clocks	• Main clock* Sub-clock HOCO clock LOCO clock IWDTCLK clock —	Main clock Sub-clock HOCO clock LOCO clock IWDTCLK clock Peripheral module clock B (PCLKB)

Note: * This can be selected in chip version B and C. This setting is not available in chip version A.

Table 4.21 Differences in I/O Registers Related to the Clock Frequency Accuracy Measurement Circuit

Item		RX210	RX230 and RX231
CACR1	FMCS[2:0]	Frequency measurement clock select 000: Main clock* 001: Sub-clock 010: HOCO clock 011: LOCO clock 100: IWDTCLK clock —	Measurement target clock select 000: Main clock 001: Sub-clock 010: HOCO clock 011: LOCO clock 100: IWDTCLK clock 101: Peripheral module clock B (PCLKB)
CACR2	RSCS[2:0]	Reference signal generation clock select 000: Main clock* 001: Sub-clock 010: HOCO clock 011: LOCO clock 100: IWDTCLK clock —	Measurement reference clock select 000: Main clock 001: Sub-clock 010: HOCO clock 011: LOCO clock 100: IWDTCLK clock 101: Peripheral module clock B (PCLKB)

Note: * This can be selected in chip version B and C. This setting is not available in chip version A.

4.4.9 Low Power Consumption

Table 4.22 lists the differences in low power consumption,Table 4.23 to Table 4.27 shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 4.28 lists the differences in I/O registers related to low power consumption.

Table 4.22 Differences in Low Power Consumption Functions

Item	RX210	RX230 and RX231
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).
Low power consumption modes	Sleep mode All-module clock stop mode Software standby mode Deep software standby mode	Sleep mode Deep sleep mode Software standby mode —
Function for lower operating power consumption	Seven operating power control modes High-speed operating mode Middle-speed operating mode 1A Middle-speed operating mode 1B Middle-speed operating mode 2A* Middle-speed operating mode 2B* Low-speed operating mode 1 Low-speed operating mode 2	Three operating power control modes High-speed operating mode Middle-speed operating mode — — — — Low-speed operating mode

Note: * This mode is available only in chip version B. Chip version A and C do not have this mode.

Table 4.23 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX230 and RX231
	Sleep Mode	Sleep Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
USB-dedicated PLL	—	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	Operating possible (Retained)	—
RAM (0000 0000h to 0000 FFFFh)	—	Operating possible (Retained)
DMAC	—	Operating possible
DTC	—	Operating possible
Flash memory	Operating	Operating
Watchdog timer (WDT)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 4.24 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (All-Module Clock Stop Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX230 and RX231
	All-Module Clock Stop Mode	All-Module Clock Stop Mode
Entry trigger	Control register + instruction	—
Exit trigger	Interrupt	—
After exiting from each mode, CPU begins from	Interrupt handling	—
Main clock oscillator	Operating possible	—
Sub-clock oscillator	Operating possible	—
High-speed on-chip oscillator	Operating possible	—
Low-speed on-chip oscillator	Operating possible	—
IWDT-dedicated on-chip oscillator	Operating possible	—
PLL	Operating possible	—
USB-dedicated PLL	—	—
CPU	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	Stopped (Retained)	—
RAM (0000 0000h to 0000 FFFFh)	—	—
DMAC	—	—
DTC	—	—
Flash memory	Stopped (Retained)	—
Watchdog timer (WDT)	Stopped (Retained)	—
Independent watchdog timer (IWDT)	Operating possible	—
Realtime clock (RTC)	Operating possible	—
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	—
Low power timer (LPT)	—	—
Voltage detection circuit (LVD)	Operating possible	—
Power-on reset circuit	Operating	—
Peripheral modules	Stopped (Retained)	—
I/O ports	Retained	—
RTCOUT	—	—
CLKOUT	—	—
Comparator B	—	—

Table 4.25 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX230 and RX231
	Software Standby Mode	Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Stopped	Stopped
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Stopped
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Stopped	Stopped
USB-dedicated PLL	—	Stopped
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	Stopped (Retained)	—
RAM (0000 0000h to 0000 FFFFh)	—	Stopped (Retained)
DMAC	—	Stopped (Retained)
DTC	—	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
Watchdog timer (WDT)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Retained)	Stopped (Retained)
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 4.26 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX230 and RX231
	Deep Software Standby Mode	Deep Software Standby Mode
Entry trigger	Control register + instruction	—
Exit trigger	Interrupt	—
After exiting from each mode, CPU begins from	Interrupt handling	—
Main clock oscillator	Stopped	—
Sub-clock oscillator	Operating possible	—
High-speed on-chip oscillator	Stopped	—
Low-speed on-chip oscillator	Stopped	—
IWDT-dedicated on-chip oscillator	Stopped (Undefined)	—
PLL	Stopped	—
USB-dedicated PLL	—	—
CPU	Stopped (Undefined)	—
RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	Stopped (Undefined)	—
RAM (0000 0000h to 0000 FFFFh)	—	—
DMAC	—	—
DTC	—	—
Flash memory	Stopped (Retained)	—
Watchdog timer (WDT)	Stopped (Undefined)	—
Independent watchdog timer (IWDT)	Stopped (Undefined)	—
Realtime clock (RTC)	Operating possible	—
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Undefined)	—
Low power timer (LPT)	—	—
Voltage detection circuit (LVD)	Operating possible	—
Power-on reset circuit	Operating	—
Peripheral modules	Stopped (Undefined)	—
I/O ports	Retained	—
RTCOUT	—	—
CLKOUT	—	—
Comparator B	—	—

Table 4.27 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX230 and RX231
	Deep Sleep Mode	Deep Sleep Mode
Entry trigger	—	Control register + instruction
Exit trigger	—	Interrupt
After exiting from each mode, CPU begins from	—	Interrupt handling
Main clock oscillator	—	Operating possible
Sub-clock oscillator	—	Operating possible
High-speed on-chip oscillator	—	Operating possible
Low-speed on-chip oscillator	—	Operating possible
IWDT-dedicated on-chip oscillator	—	Operating possible
PLL	—	Operating possible
USB-dedicated PLL	—	Operating possible
CPU	—	Stopped (Retained)
RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	—	—
RAM (0000 0000h to 0000 FFFFh)	—	Stopped (Retained)
DMAC	—	Stopped (Retained)
DTC	—	Stopped (Retained)
Flash memory	—	Stopped (Retained)
Watchdog timer (WDT)	—	Stopped (Retained)
Independent watchdog timer (IWDT)	—	Operating possible
Realtime clock (RTC)	—	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	—	Operating possible
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	—	Operating possible
Power-on reset circuit	—	Operating
Peripheral modules	—	Operating possible
I/O ports	—	Operating
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 4.28 Differences in I/O Registers Related to Low Power Consumption

Register Symbol	Bit Symbol	RX210	RX230 and RX231
SBYCR	OPE	Output port enable 0: In software standby mode or deep software standby mode, the address bus and bus control signals are set to the high-impedance state. 1: In software standby mode or deep software standby mode, the address bus and bus control signals retain the output state.	Output port enable 0: In software standby mode, the address bus and bus control signals are set to the high-impedance state. 1: In software standby mode, the address bus and bus control signals retain the output state.
	SSBY	Software standby 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed	Software standby 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed
MSTPCRA	MSTPA24	Module stop A24	Reserved
	MSTPA27	Module stop A27	Reserved
	MSTPA29	Module stop A29	Reserved
	ACSE	All-Module clock stop mode enable	Reserved
MSTPCRB	MSTPB0	Reserved	RCAN0 module stop
	MSTPB8	Temperature sensor module stop	Reserved
	MSTPB19	Reserved	USB0 module stop
	MSTPB24	Serial Communication Interface 7 Module Stop	Reserved
	MSTPB27	Serial Communication Interface 4 Module Stop	Reserved
	MSTPB28	Serial Communication Interface 3 Module Stop	Reserved
	MSTPB29	Serial Communication Interface 2 Module Stop	Reserved
MSTPCRC	MSTPC20	Reserved	IrDA module stop
	MSTPC24	Serial Communication Interface 11 Module Stop	Reserved
	MSTPC25	Serial Communication Interface 10 Module Stop	Reserved
	DSLPE	Reserved	Deep sleep mode enable
MSTPCRD	—	Not available	Module stop control register D

Register Symbol	Bit Symbol	RX210	RX230 and RX231
OPCCR	OPCM[2:0]	Operating power control mode select 000: High-speed operating mode 010: Middle-speed operating mode 1A 011: Middle-speed operating mode 1B 100: Middle-speed operating mode 2A*2 101: Middle-speed operating mode 2B*2 110: Low-speed operating mode 1 111: Low-speed operating mode 2	Operating power control mode select 000: High-speed operating mode 010: Middle-speed operating mode — — — — —
SOPCCR	SOPCM	Not available	Sub operating power control mode select 0: High-speed operating mode or middle-speed operating mode 1: Low-speed operating mode
MOSCWTCR *1	MSTS[4:0]	Main clock oscillator wait time select 00000: Wait time = 2 cycles 00001: Wait time = 4 cycles 00010: Wait time = 8 cycles 00011: Wait time = 16 cycles 00100: Wait time = 32 cycles 00101: Wait time = 256 cycles 00110: Wait time = 512 cycles 00111: Wait time = 1024 cycles 01000: Wait time = 2048 cycles 01001: Wait time = 4096 cycles 01010: Wait time = 16384 cycles 01011: Wait time = 32768 cycles 01100: Wait time = 65536 cycles 01101: Wait time = 131072 cycles 01110: Wait time = 262144 cycles 01111: Wait time = 524288 cycles	Main clock oscillator wait time 00000: Wait time = 2 cycles 00001: Wait time = 1024 cycles 00010: Wait time = 2048 cycles 00011: Wait time = 4096 cycles 00100: Wait time = 8192 cycles 00101: Wait time = 16384 cycles 00110: Wait time = 32768 cycles 00111: Wait time = 65536 cycles — — — — — — — —
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select — 001: HOCO is selected 010: Main clock oscillator is selected *3	Sleep mode return clock source select 000: LOCO is selected 001: HOCO is selected 010: Main clock oscillator is selected
SOSCWTCR	—	Sub-clock oscillator wait control register	Not available
PLLWTCR	—	PLL wait control register	Not available
HOCOWTCR2	—	HOCO wait control register 2	Not available
DPSBYCR	—	Deep standby control register	Not available
DPSIER0	—	Deep standby interrupt enable register 0	Not available
DPSIER2	—	Deep standby interrupt enable register 2	Not available
DPSIFR0	—	Deep standby interrupt flag register 0	Not available
DPSIFR2	—	Deep standby interrupt flag register 2	Not available

Register Symbol	Bit Symbol	RX210	RX230 and RX231
DPSIEGR0	—	Deep standby interrupt edge register 0	Not available
DPSIEGR2	—	Deep standby interrupt edge register 2	Not available
FHSSBYCR	—	Flash HOCO software standby control register	Not available
DPSBKRy (y = 0 to 31)	—	Deep standby backup register	Not available

Notes: 1. Descriptions for the MOSCWTCR register in the RX230 Group and RX231 Group are described in the Clock Generation Circuit section of User's Manual: Hardware.
2. This mode is available only in chip version B. Chip version A and C do not have this mode.
3. This can be selected in chip version B and C. This setting is not available in chip version A.

4.4.10 Register Write Protection Function

Table 4.29 lists the differences in register write protection function. Table 4.30 lists the differences in registers related to the register write protection function.

Table 4.29 Differences in Register Write Protection Function

Item	RX210	RX230 and RX231
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2, CKOCR, UPLLCR*, UPLLCR2*, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0,DPSIER2, DPSIFR0,DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 • Registers related to clock generation circuit: MOFCR, HOCOPCR, PLLPCR (chip version B) • Software reset register SWRR	• Register related to the operating modes: SYSCR0, SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register SWRR
PRC2 bit	VRCR	Registers related to low-power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3 bit	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR —	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR • Registers related to VBATT: VBATTCR, VBATTSR, VBTLVDICR

Note: * RX231 Group only. Not implemented on the RX230 Group.

Table 4.30 Differences in Registers Related to Register Write Protection Function

Register Symbol	Bit Symbol	RX210	RX230 and RX231
PRCR	PRC1	Protect Bit 1 Enables writing to the registers related to operating modes, low power consumption, and software reset. 0: Write disabled 1: Write enabled	Protect Bit 1 Enables writing to the registers related to operating modes, low power consumption functions, the clock generation circuit, and software reset. 0: Write disabled 1: Write enabled
	PRC2	Protect Bit 2 Enables writing to the VRCR register. 0: Write disabled 1: Write enabled	Protect Bit 2 Enables writing to the registers related to the low power timer. 0: Write disabled 1: Write enabled

4.4.11 Exception Handling

Table 4.31 lists the differences in the exception handling.

Table 4.31 Differences in the Exception Handling

Item	RX210	RX230 and RX231
Exception events	Undefined instruction exception Privileged instruction exception — — Reset Non-maskable interrupt Interrupt Unconditional trap	Undefined instruction exception Privileged instruction exception Access exceptions Floating-point exception Reset Non-maskable interrupt Interrupt Unconditional trap
Priority level	High 1: Reset 2: Non-maskable interrupt 3: Interrupt — 4: Undefined instruction exception Privileged instruction exception 5: Unconditional trap — Low — ↑	High 1: Reset 2: Non-maskable interrupt 3: Interrupt 4: Instruction-access exceptions 5: Undefined instruction exception Privileged instruction exception 6: Unconditional trap 7: Operand-access exceptions Low 8: Floating-point exception ↑
Vectors for exception events	• Fixed vector table Undefined instruction exception Privileged instruction exception — — Reset Non-maskable interrupt • Relocatable vector table (INTB) Interrupts (excluding fast interrupt) Unconditional trap • Fast interrupt vector register (FINTV) Interrupt (fast interrupt)	• Exception table register (EXTB) Undefined instruction exception Privileged instruction exception Access exceptions Floating-point exception Reset Non-maskable interrupt • Interrupt vector table (INTB) Interrupts (excluding fast interrupt) Unconditional trap • Fast interrupt vector register (FINTV) Interrupt (fast interrupt)

4.4.12 Interrupt Controller

Table 4.32 lists the differences in the interrupt controller. Table 4.33 lists the differences in registers related to the interrupt controller. Table 4.34 lists the differences in the interrupt vector table.

Table 4.32 Differences in the Interrupt Controller

Item	RX210	RX230 and RX231
Non-maskable interrupts	NMI pin interrupt Oscillation stop detection interrupt WDT underflow/refresh error IWDT underflow/refresh error Voltage monitoring 1 interrupt Voltage monitoring 2 interrupt —	NMI pin interrupt Oscillation stop detection interrupt WDT underflow/refresh error IWDT underflow/refresh error Voltage monitoring 1 interrupt Voltage monitoring 2 interrupt VBATT voltage monitoring interrupt
Return from power-down modes	• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ interrupts, TMR interrupts, or RTC alarm/periodic interrupts. • Software standby mode: Return is initiated by non-maskable interrupts, IRQ interrupts, or RTC alarm/periodic interrupts.	• Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. — • Software standby mode: Return is initiated by non-maskable interrupts, IRQ interrupts, or RTC alarm/periodic interrupts.

Table 4.33 Differences in Registers Related to the Interrupt Controller

Register Symbol	Bit Symbol	RX210	RX230 and RX231
NMISR	VBATST	Reserved	VBATT voltage monitoring interrupt status flag
NMIER	VBATEN	Reserved	VBATT voltage monitoring interrupt enable
NMICLR	VBATCLR	Reserved	VBAT clear

Headings in Table 4.34 indicate as follows.

Vector No.: Vector number for the interrupt
RX210/RX230 and RX231: RX210 Group/RX230 Group and RX231 Group
Source of interrupt request generation: Name of the source for generation of the interrupt request
Name: Name of the interrupt
Interrupt detection: “Edge” or “level” as the method for detection of the interrupt
CPU interrupt: “○” in this column indicates that the source can be used for the CPU interrupt.
DTC activation: “○” in this column indicates that the source can be used for DTC activation.
DMAC activation: “○” in this column indicates that the source can be used for DMAC activation.
sstb return: “○” in this column indicates that the source can be used for return from software-standby mode.
IER: IER register and bit corresponding to the vector number
IPR: IPR register corresponding to the interrupt source
DTCER: DTCER register corresponding to the DTC activation source

Table 4.34 Differences in the Interrupt Vector Table

Vector No.	RX210/ RX230 and RX231	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	IER	IPR	DTCER
21	RX210	FCU	FIFERR	Level	○	×	×	×	IER02.IEN5	IPR001	—
	RX230 RX231	—	Reserved	—	×				—	—	
36	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	USB0	D0FIFO0	Edge	○	○	○		IER04.IEN4	IPR036	DTCER036
37	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	USB0	D1FIFO0	Edge	○	○	○		IER04.IEN5	IPR037	DTCER037
38	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	USB0	USBI0	Edge	○	×	×		IER04.IEN6	IPR038	
40	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	SDHI	SBFAI	Edge	○	○	○		IER05.IEN0	IPR040	DTCER040
41	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	SDHI	CDETI	Level	○				IER05.IEN1	IPR041	
42	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	SDHI	CACI	Level	○				IER05.IEN2	IPR042	
43	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	SDHI	SDACI	Level	○				IER05.IEN3	IPR043	
52	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	CAN	COMFRXINT	Edge	○	○	○		IER06.IEN4	IPR052	DTCER052
53	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	CAN	RXFINT	Level	○				IER06.IEN5	IPR053	
54	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	CAN	TXINT	Level	○				IER06.IEN6	IPR054	
55	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	CAN	CHERRINT	Level	○				IER06.IEN7	IPR055	
56	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	CAN	GLERRINT	Level	○				IER07.IEN0	IPR056	
60	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	CTSU	CTSUWR	Edge	○	○	○		IER07.IEN4	IPR060	DTCER060

Vector No.	RX210/ RX230 and RX231	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	IER	IPR	DTCER
61	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	CTSU	CTSURD	Edge	○	○	○		IER07.IEN5	IPR060	DTCER061
62	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	CTSU	CTSUFN	Edge	○				IER07.IEN6	IPR060	
80	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	ELC	ELSR8I	Edge	○			○	IER0A.IEN0	IPR080	—
90	RX210 RX230	—	Reserved	—	×	×	×	×	—	—	—
	RX231	USB	USBR0	Level	○			○	IER0B.IEN2	IPR090	
91	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	VBATT	BVTLVDI	Edge	○			○	IER0B.IEN3	IPR091	
104	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	CMPB1	CMPB2	Edge	○	○	○		IER0D.IEN0	IPR104	DTCER104
105	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	CMPB1	CMPB3	Edge	○	○	○		IER0D.IEN1	IPR105	DTCER105
108	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	SSI0	SSIF0	Level	○				IER0D.IEN4	IPR108	
109	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	SSI0	SSIRXI0	Edge	○	○	○		IER0D.IEN5	IPR108	DTCER109
110	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	SSI0	SSITXI0	Edge	○	○	○		IER0D.IEN6	IPR108	DTCER110
111	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	Secure	RD	Edge	○	○	○		IER0D.IEN7	IPR111	DTCER111
112	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	Secure	WR	Edge	○	○	○		IER0E.IEN0	IPR111	DTCER112
113	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	Secure	Error	Edge	○				IER0E.IEN1	IPR113	
142	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU0	TGI0A	Edge	○	○	○		IER11.IEN6	IPR142	DTCER142

Vector No.	RX210/ RX230 and RX231	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	IER	IPR	DTCER
143	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU0	TGI0B	Edge	○	○			IER11.IEN7	IPR142	DTCER143
144	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU0	TGI0C	Edge	○	○			IER12.IEN0	IPR142	DTCER144
145	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU0	TGI0D	Edge	○	○			IER12.IEN1	IPR142	DTCER145
146	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU0	TCI0V	Edge	○	×			IER12.IEN2	IPR146	
147	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU1	TGI1A	Edge	○	○	○		IER12.IEN3	IPR147	DTCER147
148	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU1	TGI1B	Edge	○	○			IER12.IEN4	IPR147	DTCER148
149	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU1	TCI1V	Edge	○				IER12.IEN5	IPR149	
150	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU1	TCI1U	Edge	○				IER12.IEN6	IPR149	
150	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU1	TCI1U	Edge	○				IER12.IEN6	IPR149	
151	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU2	TGI2A	Edge	○	○	○		IER12.IEN7	IPR151	DTCER151
152	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU2	TGI2B	Edge	○	○			IER13.IEN0	IPR151	DTCER152
153	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU2	TCI2V	Edge	○				IER13.IEN1	IPR153	
154	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU2	TCI2U	Edge	○				IER13.IEN2	IPR153	
155	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU3	TGI3A	Edge	○	○	○		IER13.IEN3	IPR155	DTCER155

Vector No.	RX210/ RX230 and RX231	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	DMAC Activation	sstb Return	IER	IPR	DTCER
156	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU3	TGI3B	Edge	○	○			IER13.IEN4	IPR155	DTCER156
157	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU3	TGI3C	Edge	○	○			IER13.IEN5	IPR155	DTCER157
158	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU3	TGI3D	Edge	○	○			IER13.IEN6	IPR155	DTCER158
159	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU3	TCI3V	Edge	○				IER13.IEN7	IPR159	
160	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU4	TGI4A	Edge	○	○	○		IER14.IEN0	IPR160	DTCER160
161	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU4	TGI4B	Edge	○	○			IER14.IEN1	IPR160	DTCER161
162	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU4	TCI4V	Edge	○				IER14.IEN2	IPR162	
163	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU4	TCI4U	Edge	○				IER14.IEN3	IPR162	
164	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU5	TGI5A	Edge	○	○	○		IER14.IEN4	IPR164	DTCER164
165	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU5	TGI5B	Edge	○	○			IER14.IEN5	IPR164	DTCER165
166	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU5	TCI5V	Edge	○				IER14.IEN6	IPR166	
167	RX210	—	Reserved	—	×	×	×	×	—	—	—
	RX230 RX231	TPU5	TCI5U	Edge	○				IER14.IEN7	IPR166	

4.4.13 Buses

Table 4.35 lists the differences in buses. Table 4.36 lists the difference in the I/O register related to buses.

Table 4.35 Differences in Buses

Item	RX210	RX230 and RX231
Internal peripheral bus 3	Not available	Connected to peripheral modules (USB0, RSCAN, CTSU) Operates in synchronization with the peripheral-module clock (PCLKB)
Internal peripheral bus 4	Not available	Connected to peripheral modules (MTU2) Operates in synchronization with the peripheral-module clock (PCLKA)

Table 4.36 Difference in the I/O Register Related to Buses

Register Symbol	Bit Symbol	RX210	RX230 and RX231
BUSPRI	BPHB[1:0]	Reserved	Internal peripheral bus 4 priority control

4.4.14 Data Transfer Controller

Table 4.37 lists the differences in registers related to the Data Transfer Controller.

Table 4.37 Differences in I/O Registers Related to the Data Transfer Controller

Register Symbol	Bit Symbol	RX210	RX230 and RX231
DTCVBR	—	DTC Vector Base Register The DTCVBR register is used to set the base address for calculating the address to which the DTC vector is allocated. Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 12 bits are reserved and the values are fixed to 0. Write 0 to the lower 12 bits if necessary. It can be set in the range of 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h in 4-Kbyte units.	DTC Vector Base Register The DTCVBR register is used to set the base address for calculating the address to which the DTC vector is allocated. Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 10 bits are reserved and the values are fixed to 0. Write 0 to the lower 10 bits if necessary. It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-Kbyte units.

4.4.15 Event Link Controller

Table 4.38 lists the differences in the event link controller. Table 4.39 lists the differences in the ELSRn register. Table 4.40 lists the differences in values for the ELSRn register.

Table 4.38 Differences in the Event Link Controller

Item	RX210	RX230 and RX231
Event link function	59 types of event signals can be directly connected to modules. • The operation of timer modules can be selected when an event is input to the timer module. • Event link operation is possible for ports B and E.	63 types of event signals can be directly connected to modules. • The operation of timer modules can be selected when an event is input to the timer module. • Event link operation is possible for port B and port E.

Table 4.39 Differences in the ELSRn Register

Register Symbol	Peripheral Function (Module)	RX210	RX230 and RX231
ELSR1	MTU1	○	○
ELSR2	MTU2	○	○
ELSR3	MTU3	○	○
ELSR4	MTU4	○	○
ELSR7	CMT1	○	○
ELSR8	ICU (LPT-dedicated interrupt)	—	○
ELSR10	TMR0	○	○
ELSR12	TMR2	○	○
ELSR14	CTSU	—	○
ELSR15	12-bit A/D converter	○	○
ELSR16	DA0	○	○
ELSR18	ICU (Interrupt 1)	○	○
ELSR19	ICU (Interrupt 2)	○	○
ELSR20	Output port group 1	○	○
ELSR21	Output port group 2	○	○
ELSR22	Input port group 1	○	○
ELSR23	Input port group 2	○	○
ELSR24	Single port 0	○	○
ELSR25	Single port 1	○	○
ELSR26	Single port 2	○	○
ELSR27	Single port 3	○	○
ELSR28	Clock source switching to LOCO	○	○
ELSR29	POE	○	○

Table 4.40 Differences in Values for the ELSRn Register

Setting Value	RX210	RX231	Event Type
08h	○	○	MTU1 compare match 1A
09h	○	○	MTU1 compare match 1B
0Ah	○	○	MTU1 overflow

Setting Value	RX210	RX231	Event Type
0Bh	○	○	MTU1 underflow
0Ch	○	○	MTU2 compare match 2A
0Dh	○	○	MTU2 compare match 2B
0Eh	○	○	MTU2 overflow
0Fh	○	○	MTU2 underflow
10h	○	○	MTU3 compare match 3A
11h	○	○	MTU3 compare match 3B
12h	○	○	MTU3 compare match 3C
13h	○	○	MTU3 compare match 3D
14h	○	○	MTU3 overflow
15h	○	○	MTU4 compare match 4A
16h	○	○	MTU4 compare match 4B
17h	○	○	MTU4 compare match 4C
18h	○	○	MTU4 compare match 4D
19h	○	○	MTU4 overflow
1Ah	○	○	MTU4 underflow
1Fh	○	○	CMT1 compare match 1
22h	○	○	TMR0 compare match A0
23h	○	○	TMR0 compare match B0
24h	○	○	TMR0 overflow
28h	○	○	TMR2 compare match A2
29h	○	○	TMR2 compare match B2
2Ah	○	○	TMR2 overflow
2Eh	○	○	RTC cycle
31h	○	○	IWDT underflow or refresh error
32h	—	○	LPT compare match
34h	—	○	ADC comparison condition met
35h	—	○	ADC comparison condition not met
3Ah	○	○	SCI5 error (receive error or error signal detection)
3Bh	○	○	SCI5 receive data full
3Ch	○	○	SCI5 transmit data empty
3Dh	○	○	SCI5 transmit end
4Eh	○	○	RIIC0 communication error or event generation
4Fh	○	○	RIIC0 receive data full
50h	○	○	RIIC0 transmit data empty
51h	○	○	RIIC0 transmit end
52h	○	○	RSPI0 error (mode fault, overrun, or parity error)
53h	○	○	RSPI0 idle
54h	○	○	RSPI0 receive data full
55h	○	○	RSPI0 transmit data empty
56h	○	○	RSPI0 transmit end (except during clock synchronous operation in slave mode)
58h	○	○	A/D conversion end of 12-bit A/D converter
59h	○	○	Comparison result change of comparator B0
5Ah	○	○	Comparison result change of comparator B0/B1
5Bh	○	○	LVD1 voltage detection
5Ch	○	○	LVD2 voltage detection
5Dh	○	○	DMAC0 transfer end

Setting Value	RX210	RX231	Event Type
5Eh	○	○	DMAC1 transfer end
5Fh	○	○	DMAC2 transfer end
60h	○	○	DMAC3 transfer end
61h	○	○	DTC transfer end
62h	○	○	Oscillation stop detection of clock generation circuit
63h	○	○	Input edge detection of input port group 1
64h	○	○	Input edge detection of input port group 2
65h	○	○	Input edge detection of single input port 0
66h	○	○	Input edge detection of single input port 1
67h	○	○	Input edge detection of single input port 2
68h	○	○	Input edge detection of single input port 3
69h	○	○	Software event
6Ah	—	○	DOC data operation condition met signal

Table 4.41 Differences in I/O Registers Related to Event Link Controller

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ELOPC	LPTMD[1:0]	Reserved	LPT operation select bits

4.4.16 I/O Ports

Table 4.42 to Table 4.44 shows a Comparative Listing of Specifications of I/O Ports, and Table 4.45 lists the differences in general I/O ports. Table 4.46 lists the differences in I/O registers related to I/O ports.

Table 4.42 Comparative Listing of Specifications of I/O Ports (100 Pins)

Port	RX210	RX230 and RX231
PORT0	P03、P05、P07	P03、P05、P07
PORT1	P12～P17	P12～P17
PORT2	P20～P27	P20～P27
PORT3	P30～P37	P30～P37
PORT4	P40～P47	P40～P47
PORT5	P50～P55	P50～P55
PORTA	PA0～PA7	PA0～PA7
PORTB	PB0～PB7	PB0～PB7
PORTC	PC0～PC7	PC0～PC7
PORTD	PD0～PD7	PD0～PD7
PORTE	PE0～PE7	PE0～PE7
PORTH	PH0～PH3	PH0～PH3
PORTJ	PJ1、PJ3	PJ3

Table 4.43 Comparative Listing of Specifications of I/O Ports (64 Pins)

Port	RX210	RX230 and RX231
PORT0	P03、P05	P03、P05
PORT1	P14～P17	P14～P17
PORT2	P26、P27	P26、P27
PORT3	P30～P32、P35～P37	P30、P31、P35～P37
PORT4	P40～P44、P46	P40～P44、P46
PORT5	P54、P55	P54、P55
PORTA	PA0、PA1、PA3、PA4、PA6	PA0、PA1、PA3、PA4、PA6
PORTB	PB0、PB1、PB3、PB5～PB7	PB0、PB1、PB3、PB5～PB7
PORTC	PC2～PC7	PC2～PC7
PORTD	Not provided	Not provided
PORTE	PE0～PE5	PE0～PE5
PORTH	PH0～PH3	PH0～PH3
PORTJ	Not provided	Not provided

Table 4.44 Comparative Listing of Specifications of I/O Ports (48 Pins)

Port	RX210	RX230 and RX231
PORT0	Not provided	Not provided
PORT1	P14～P17	P14～P17
PORT2	P26、P27	P26、P27
PORT3	P30、P31、P35～P37	P30、P31、P35～P37
PORT4	P40～P42、P46	P40～P42、P46
PORT5	Not provided	Not provided
PORTA	PA1、PA3、PA4、PA6	PA1、PA3、PA4、PA6
PORTB	PB0、PB1、PB3、PB5	PB0、PB1、PB3、PB5
PORTC	PC4～PC7	PC4～PC7
PORTD	Not provided	Not provided
PORTE	PE1～PE4	PE1～PE4
PORTH	PH0～PH3	PH0～PH3
PORTJ	Not provided	Not provided

Table 4.45 Differences in General I/O Ports

Item	Port Symbol	RX210	RX230	RX231
Ports	PORTH	PH0, PH1, PH2, PH3	PH0, PH1, PH2, PH3	No I/O port
	PORTJ	PJ1, PJ3	—, PJ3	
Open drain output	PORT5	P50 to P52, P54, PJ3 Not available	P50 to P52, P54, PJ3 Available	
Drive Capacity Switching	PORT3	P36, P37 Available	P36, P37 Not available	
5 V tolerant	PORT1	P17* Available	P17 Available	
	PORT3	P30 to P32 Not available	P30 to P32 Not available	
	PORTB	PB5 Not available	PB5 Available	
PORTC used as an 8-bit general I/O port	—	Not available	• 64-pin package PB6 and PB7 can be used as PC0 and PC1, respectively. • 48-pin package PB0, PB1, PB3, and PB5 can be used as PC0, PC1, PC2, and PC3, respectively.	

Note: * Chip version B and C support 5 V tolerance. Chip version A does not support 5 V tolerance.

Table 4.46 Differences in I/O Registers Related to I/O Ports

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ODR0	B2, B3	Pm1 Output Type Select • P01, P21, P31, P51, P61, P81, P91, PA1, PB1, PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z	Pm1 Output Type Select • P21, P31, P51, PA1, PB1, PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z
PSRA	—	Not available	Port switching register A (for the 64-pin package)
PSRB	—	Not available	Port switching register B (for the 48-pin package)

4.4.17 Multi-Function Pin Controller

Table 4.47 shows a comparative listing of functions assigned to each multiplexed pin, and Table 4.48 lists the differences in I/O registers related to the multi-function pin controller.

"√" indicates pin implemented, "×" indicates pin not implemented, "-" indicates pin function not implemented, Grey hatching indicates pin function not implemented.

Table 4.47 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Module/Function	Pin Functions	Allocation Port	RX210 100-pin	RX210 64-pin	RX210 48-pin	RX230 and RX231 100-pin	RX230 and RX231 64-pin	RX230 and RX231 48-pin
Interrupt	NMI(input)	P35	○	○	○	○	○	○
	IRQ0-DS(input)	P30	○	○	○			
	IRQ0(input)	P30	—	—	—	○	○	○
		PD0	○	×	×	○	×	×
		PH1*2	○	○	○	○	○	○
	IRQ1-DS(input)	P31	○	○	○			
	IRQ1(input)	P31	—	—	—	○	○	○
		PD1	○	×	×	○	×	×
		PH2*2	○	○	○	○	○	○
	IRQ2-DS(input)	P32	○	○	×			
	IRQ2(input)	P32	—	—	—	○	×	×
		P12	○	×	×	○	×	×
		PD2	○	×	×	○	×	×
	IRQ3-DS(input)	P33	○	×	×			
	IRQ3(input)	P33	—	—	—	○	×	×
		P13	○	×	×	○	×	×
		PD3	○	×	×	○	×	×
	IRQ4-DS(input)	PB1	○	○	○			
	IRQ4(input)	PB1	—	—	—	○	○	○
		P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PD4	○	×	×	○	×	×
	IRQ5-DS(input)	PA4	○	○	○			
	IRQ5(input)	PA4	—	—	—	○	○	○
		P15	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
		PE5	○	○	×	○	○	×
	IRQ6-DS(input)	PA3	○	○	○			
	IRQ6(input)	PA3	—	—	—	○	○	○
		P16	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
		PE6	○	×	×	○	×	×
	IRQ7-DS(input)	PE2	○	○	○			
	IRQ7(input)	PE2	—	—	—	○	○	○
		P17	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
		PE7	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX210 100-pin	RX210 64-pin	RX210 48-pin	RX230 and RX231 100-pin	RX230 and RX231 64-pin	RX230 and RX231 48-pin
Clock generation circuit	CLKOUT (output)	PE3				○	○	○
		PE4				○	○	○
Multi-function timer unit 2	MTIOC0A(input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
	MTIOC0B(input/output)	P13	○	×	×	○	×	×
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C(input/output)	P32	○	○	×	○	×	×
		PB1	○	○	○	○	○	○
	MTIOC0D(input/output)	P33	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
	MTIOC1A(input/output)	P20	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIOC1B(input/output)	P21	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	MTIOC2A(input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B(input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A(input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
		PJ1	○	×	×	—	—	—
	MTIOC3B(input/output)	P17	○	○	○	○	○	○
		P22	○	×	×	○	×	×
		PB7	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
	MTIOC3C(input/output)	P16	○	○	○	○	○	○
		PC0	○	×	×	○	×	×
		PC6	○	○	○	○	○	○
		PJ3	○	×	×	○	×	×
	MTIOC3D(input/output)	P16	○	○	○	○	○	○
		P23	○	×	×	○	×	×
		PB6	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	MTIOC4A(input/output)	P24	○	×	×	○	×	×
		PA0	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
Multi-function timer unit 2	MTIOC4B(input/output)	P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
	MTIOC4C(input/output)	P25	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC4D(input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		PC3	○	○	×	○	○	×
		PD2	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIC5U(input)	PA4	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
	MTIC5V(input)	PA6	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
	MTIC5W(input)	PB0	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
	MTCLKA(input)	P14	○	○	○	○	○	○
		P24	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB(input)	P15	○	○	○	○	○	○
		P25	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC(input)	P22	○	×	×	○	×	×
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD(input)	P23	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0#(input)	PC4	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
	POE1#(input)	PB5	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
	POE2#(input)	P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PD5	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
Port output enable 2	POE3#(input)	P33	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD4	○	×	×	○	×	×
	POE8#(input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
16-bit timer pulse unit	TIOCA0(input/output)	PA0				○	○	×
	TIOCB0(input/output)	P17				○	○	○
		PA1				○	○	○
	TIOCC0(input/output)	P32				○	×	×
	TIOCD0(input/output)	P33				○	×	×
		PA3				○	○	○
	TIOCA1(input/output)	PA4				○	○	○
	TIOCB1(input/output)	P16				○	○	○
		PA5				○	×	×
	TIOCA2(input/output)	PA6				○	○	○
	TIOCB2(input/output)	P15				○	○	○
		PA7				○	×	×
	TIOCA3(input/output)	P21				○	×	×
		PB0				○	○	○
	TIOCB3(input/output)	P20				○	×	×
		PB1				○	○	○
	TIOCC3(input/output)	P22				○	×	×
		PB2				○	×	×
	TIOCD3(input/output)	P23				○	×	×
		PB3				○	○	○
	TIOCA4(input/output)	P25				○	×	×
		PB4				○	×	×
	TIOCB4(input/output)	P24				○	×	×
		PB5				○	○	○
	TIOCA5(input/output)	P13				○	×	×
		PB6				○	○	×
	TIOCB5(input/output)	P14				○	○	○
		PB7				○	○	×
	TCLKA(input)	P14				○	○	○
		PC2				○	○	×
	TCLKB(input)	P15				○	○	○
		PA3				○	○	○
		PC3				○	○	×
	TCLKC(input)	P16				○	○	○
		PB2				○	×	×
		PC0				○	×	×

Module/Function	Pin Functions	Allocation Port	RX210 100-pin	RX210 64-pin	RX210 48-pin	RX230 and RX231 100-pin	RX230 and RX231 64-pin	RX230 and RX231 48-pin
16-bit timer pulse unit	TCLKD(input)	P17				○	○	○
		PB3				○	○	○
		PC1				○	×	×
8-bit timer	TMO0(output)	P22	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PH1*2	○	○	○	○	○	○
	TMCI0(input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3*2	○	○	○	○	○	○
	TMRI0(input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2*2	○	○	○	○	○	○
	TMO1(output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1(input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1(input)	P24	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	TMO2(output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2(input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2(input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3(output)	P13	○	×	×	○	×	×
		P32	○	○	×	○	×	×
		P55	○	○	×	○	○	×
	TMCI3(input)	P27	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TMRI3(input)	P30	○	○	○	○	○	○
		P33	○	×	×	○	×	×
Serial communications interface	RXD0(input) / SMISO0(input/output) / SSCL0(input/output)	P21	○	×	×	○	×	×
	TXD0(output) / SMOSI0(input/output) / SSDA0(input/output)	P20	○	×	×	○	×	×
	SCK0(input/output)	P22	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
Serial communications interface	CTS0#(input) / RTS0#(output) / SS0#(input)	P23	○	×	×	○	×	×
	RXD1(input) / SMISO1(input/output) / SSCL1(input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1(output) / SMOSI1(input/output) / SSDA1(input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1(input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1#(input) / RTS1#(output) / SS1#(input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD5(input) / SMISO5(input/output) / SSCL5(input/output)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×
	TXD5(output) / SMOSI5(input/output) / SSDA5(input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5(input/output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC4	○	○	○	○	○	○
	CTS5#(input) / RTS5#(output) / SS5#(input)	PA6	○	○	○	○	○	○
		PC0	○	×	×	○	×	×
	RXD6(input) / SMISO6(input/output) / SSCL6(input/output)	P33	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
	TXD6(output) / SMOSI6(input/output) / SSDA6(input/output)	P32	○	○	×	○	×	×
		PB1	○	○	○	○	○	○
	SCK6(input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
	CTS6#(input) / RTS6#(output) / SS6#(input)	PB2	○	×	×	○	×	×
		PJ3	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
Serial communications interface	RXD8(input) / SMISO8(input/output) / SSCL8(input/output)	PC6	○	○	○	○	○	○
	TXD8(output) / SMOSI8(input/output) / SSDA8(input/output)	PC7	○	○	○	○	○	○
	SCK8(input/output)	PC5	○	○	○	○	○	○
	CTS8#(input) / RTS8#(output) / SS8#(input)	PC4	○	○	○	○	○	○
	RXD9(input) / SMISO9(input/output) / SSCL9(input/output)	PB6	○	○	×	○	○	×
	TXD9(output) / SMOSI9(input/output) / SSDA9(input/output)	PB7	○	○	×	○	○	×
	SCK9(input/output)	PB5	○	○	×	○	○	×
	CTS9#(input) / RTS9#(output) / SS9#(input)	PB4	○	×	×	○	×	×
	RXD12(input) / SMISO12(input/output) / SSCL12(input/output) / RXDX12(input)	PE2	○	○	○ (SMISO12 function is not available)	○	○	○ (SMISO12 function is not available)
	TXD12(output) / SMOSI12(input/output) / SSDA12(input/output) / TXDX12(output) / SIOX12(input/output)	PE1	○	○	○ (SMOSI12 function is not available)	○	○	○ (SMOSI12 function is not available)
	SCK12(input/output)	PE0	○	○	×	○	○	×
	CTS12#(input) / RTS12#(output) / SS12#(input)	PE3	○	○	○ (SS12# function is not available)	○	○	○ (SS12# function is not available)
I^2C bus interface	SCL-DS(input/output)	P16	○	○	○	○	○	○
	SCL(input/output)	P12	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
I²C bus interface	SDA-DS(input/output)	P17	○	○	○	○	○	○
	SDA(input/output)	P13	○	×	×	○	×	×
Serial peripheral interface	RSPCKA(input/output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA(input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA(input/output)	P17	○	○	○	○	○	○
		PA7	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
	SSLA0(input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1(output)	PA0	○	○	×	○	○	×
		PC0	○	×	×	○	×	×
	SSLA2(output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
	SSLA3(output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT(output)	P16	○	○	×	○	○	×
		P32	○	○	×	○	×	×
	RTCIC0(input)*1	P30	○	○	×	○	○	×
	RTCIC1(input)*1	P31	○	○	×	○	○	×
	RTCIC2(input)*1	P32	○	○	×	○	×	×
IrDA interface	IRTXD5(output)	PA4				○	○	○
		PC3				○	○	×
	IRRXD5(input)	PA2				○	×	×
		PA3				○	○	○
		PC2				○	○	×
CAN module	CRXD0(input)	P15				○	○	○
		P55				○	○	×
	CTXD0(output)	P14				○	○	○
		P54				○	○	×
Serial sound interface	SSISCK0(input/output)	P23				○	×	×
		P31				○	○	○
		PA1				○	○	○
	SSIWS0(input/output)	P21				○	×	×
		P27				○	○	○
		PA6				○	○	○
	SSITXD0(output)	P17				○	○	○
		PA4				○	○	○
	SSIRXD0(input)	P20				○	×	×
		P26				○	○	○
		PA3				○	○	○

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
Serial sound interface	AUDIO_MCLK(input)	P22				○	×	×
		P30				○	○	○
		PE3				○	○	○
SD host interface	SDHI_CLK(output)	PB1				○	○	×
	SDHI_CMD(input/output)	PB0				○	○	×
	SDHI_D0(input/output)	PC3				○	○	×
	SDHI_D1(input/output)	PB6				○	○	×
		PC4				○	○	×
	SDHI_D2(input/output)	PB7				○	○	×
	SDHI_D3(input/output)	PC2				○	○	×
	SDHI_CD(input)	PB5				○	○	×
	SDHI_WP(input)	PB3				○	○	×
USB 2.0 host/function module	USB0_VBUS(input)	P16				○	○	○
		PB5				○	○	○
	USB0_EXICEN(output)	P21				○	×	×
		PC6				×	○	○
	USB0_VBUSEN(output)	P16				○	○	○
		P24				○	×	×
		P26				×	○	○
		P32				○	×	×
	USB0_OVRCURA(input)	P14				○	○	○
	USB0_OVRCURB(input)	P16				○	○	○
		P22				○	×	×
	USB0_ID(input)	P20				○	×	×
		PC5				×	○	○
12-bit A/D converter	AN000(input)*1	P40	○	○	○	○	○	○
	AN001(input)*1	P41	○	○	○	○	○	○
	AN002(input)*1	P42	○	○	○	○	○	○
	AN003(input)*1	P43	○	○	×	○	○	×
	AN004(input)*1	P44	○	○	×	○	○	×
	AN005(input)*1	P45	○	×	×	○	×	×
	AN006(input)*1	P46	○	○	○	○	○	○
	AN007(input)*1	P47	○	×	×	○	×	×
	AN008(input)*1	PE0	○	○	×			
	AN009(input)*1	PE1	○	○	○			
	AN010(input)*1	PE2	○	○	○			
	AN011(input)*1	PE3	○	○	○			
	AN012(input)*1	PE4	○	○	○			
	AN013(input)*1	PE5	○	○	×			
	AN014(input)*1	PE6	○	×	×			
	AN015(input)*1	PE7	○	×	×			

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
12-bit A/D converter	AN016(input)*1	PE0				○	○	×
	AN017(input)*1	PE1				○	○	○
	AN018(input)*1	PE2				○	○	○
	AN019(input)*1	PE3				○	○	○
	AN020(input)	PE4				○	○	○
	AN021(input)	PE5				○	○	×
	AN022(input)	PE6				○	×	×
	AN023(input)	PE7				○	×	×
	AN024(input)	PD0				○	×	×
	AN025(input)	PD1				○	×	×
	AN026(input)	PD2				○	×	×
	AN027(input)	PD3				○	×	×
	AN028(input)	PD4				○	×	×
	AN029(input)	PD5				○	×	×
	AN030(input)	PD6				○	×	×
	AN031(input)	PD7				○	×	×
	ADTRG0#(input)	P07	○	×	×	○	×	×
		P16	○	○	○	○	○	○
		P25	○	×	×	○	×	×
D/A converter	DA0(output)*1	P03	○	○	×	○	○	×
	DA1(output)*1	P05	○	○	×	○	○	×
Clock frequency accuracy measurement circuit	CACREF(input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0*2	○	○	○	○	○	○
Comparator A	CMPA1(input)*1	PE3	○	○	○			
	CMPA2(input)*1	PE4	○	○	○	○	○	○
	CVREFA(input)*1	PA1	○	○	○			
Comparator B	CMPB0(input)*1	PE1	○	○	○	○	○	○
	CVREFB0(input)*1	PE2	○	○	○	○	○	○
	CMPB1(input)*1	PA3	○	○	○	○	○	○
	CVREFB1(input)*1	PA4	○	○	○	○	○	○
	CMPB2(input)*1	P15				○	○	○
	CVREFB2(input)*1	P14				○	○	○
	CMPB3(input)*1	P26				○	○	○
	CVREFB3(input)*1	P27				○	○	○
	CMPOB0(output)	PE5				○	○	×
	CMPOB1(output)	PB1				○	○	○
	CMPOB2(output)	P17				○	○	○
	CMPOB3(output)	P30				○	○	○
Capacitive touch sensing unit (CTSU)	TSCAP(output)	PC4				○	○	○
	TS0(output)	P34				○	×	×
	TS1(output)	P33				○	×	×
	TS2(output)	P27				○	○	○
	TS3(output)	P26				○	○	○

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
Capacitive touch sensing unit (CTSU)	TS4(output)	P25				○	×	×
	TS5(output)	P24				○	×	×
	TS6(output)	P23				○	×	×
	TS7(output)	P22				○	×	×
	TS8(output)	P21				○	×	×
	TS9(output)	P20				○	×	×
	TS12(output)	P15				○	○	○
	TS13(output)	P14				○	○	○
	TS15(output)	P55				○	○	×
	TS16(output)	P54				○	○	×
	TS17(output)	P53				○	×	×
	TS18(output)	P52				○	×	×
	TS19(output)	P51				○	×	×
	TS20(output)	P50				○	×	×
	TS22(output)	PC6				○	○	○
	TS23(output)	PC5				○	○	○
	TS27(output)	PC3				○	○	×
	TS30(output)	PC2				○	○	×
	TS33(output)	PC1				○	×	×
	TS35(output)	PC0				○	×	×
External bus*2	CS0#(output)	P24	○	×	×	○	×	×
		PC7	○	×	×	○	×	×
	CS1#(output)	P25	○	×	×	○	×	×
		PC6	○	×	×	○	×	×
	CS2#(output)	P26	○	×	×	○	×	×
		PC5	○	×	×	○	×	×
	CS3#(output)	P27	○	×	×	○	×	×
		PC4	○	×	×	○	×	×
	A0～A7(output)	PA0～PA7	○	×	×	○	×	×
	A8～A15(output)	PB0～PB7	○	×	×	○	×	×
	A16～A23(output)	PC0～PC7	○	×	×	○	×	×
	D0～D7(input/output)	PD0～PD7	○	×	×	○	×	×
	D8～D15(input/output)	PE0～PE7	○	×	×	○	×	×
	BCLK(output)	P53	○	×	×	○	×	×
	RD#(output)	P52	○	×	×	○	×	×
	WR#(output)	P50	○	×	×	○	×	×
	WR0#(output)	P50	○	×	×	○	×	×
	WR1#(output)	P51	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX210			RX230 and RX231		
			100-pin	64-pin	48-pin	100-pin	64-pin	48-pin
External bus*2	BC0#(output)	PA0	○	×	×	○	×	×
	BC1#(output)	P51	○	×	×	○	×	×
	WAIT#(input)	P51	○	×	×	○	×	×
		P55	○	×	×	○	×	×
		PC5	○	×	×	○	×	×
	ALE(output)	P54	○	×	×	○	×	×

Note 1. Select general input (by setting the Bm bits for the given pin in the PDR and PMR for the given port to 0) for the pin if this pinfunction is to be used.

Note 2. Only the products of the RX230 group have these pins.

Table 4.48 Differences in I/O Registers Related to the Multi-Function Pin Controller

Register Symbol	Bit Symbol	RX210	RX230 and RX231
P0nPFS (n = 3, 5, 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ASEL	Analog Input Function Select 0: Used other than as analog pin 1: Used as analog pin P03: DA0 (145/144/100/80/69/64 pins) P05: DA1 (145/144/100/80/69/64 pins)	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin P03: DA0 (100/64 pins) P05: DA1 (100/64 pins)
P1nPFS (n = 2 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (145/144/100/80 pins) P13: IRQ3 input switch (145/144/100/80 pins) P14: IRQ4 input switch (145/144/100/80/69/64/48 pins) P15: IRQ5 input switch (145/144/100/80/69/64/48 pins) P16: IRQ6 input switch (145/144/100/80/69/64/48 pins) P17: IRQ7 input switch (145/144/100/80/69/64/48 pins)	Interrupt Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (100 pins) P13: IRQ3 input switch (100 pins) P14: IRQ4 input switch (100/64/48 pins) P15: IRQ5 input switch (100/64/48 pins) P16: IRQ6 input switch (100/64/48 pins) P17: IRQ7 input switch (100/64/48 pins)
	ASEL	Reserved	Analog function select
P2nPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ASEL	Reserved	Analog function select
P3nPFS (n = 0 to 4)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS input switch (145/144/100/80/69/64/48 pins) P31: IRQ1-DS input switch (145/144/100/80/69/64/48 pins) P32: IRQ2-DS input switch (145/144/100/80/69/64 pins) P33: IRQ3-DS input switch (145/144/100 pins) P34: IRQ4 input switch (145/144/100/80 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 input switch (100/64/48 pins) P31: IRQ1 input switch (100/64/48 pins) P32: IRQ2 input switch (100 pins) P33: IRQ3 input switch (100 pins) P34: IRQ4 input switch (100 pins)

Register Symbol	Bit Symbol	RX210	RX230 and RX231
P4nPFS (n = 0 to 7)	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (145/144/100/80/69/64/48 pins) P41: AN001 (145/144/100/80/69/64/48 pins) P42: AN002 (145/144/100/80/69/64/48 pins) P43: AN003 (145/144/100/80/69/64 pins) P44: AN004 (145/144/100/80/69/64 pins) P45: AN005 (145/144/100/80 pins) P46: AN006 (145/144/100/80/69/64/48 pins) P47: AN007 (145/144/100/80 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (100/64/48 pins) P41: AN001 (100/64/48 pins) P42: AN002 (100/64/48 pins) P43: AN003 (100/64 pins) P44: AN004 (100/64 pins) P45: AN005 (100 pins) P46: AN006 (100/64/48 pins) P47: AN007 (100 pins)
P5nPFS (n = 0 to 2, 4 to 6) (RX210) (n = 0 to 5) (RX230 and RX231)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
P6nPFS (n = 0, 1)	-	P6n Pin Function Control Registers	Not available
P7nPFS (n = 0, 4 to 7)	-	P7n Pin Function Control Registers	Not available
P8nPFS (n = 0 to 3, 6, 7)	-	P8n Pin Function Control Registers	Not available
P9nPFS (n = 0 to 3)	-	P9n Pin Function Control Registers	Not available
PAnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6-DS input switch (145/144/100/80/69/64/48 pins) PA4: IRQ5-DS input switch (145/144/100/80/69/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 input switch (100/64/48 pins) PA4: IRQ5 input switch (100/64/48 pins)
	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PA1: CVREFA (145/144/100/80/69/64/48 pins) PA3: CMPB1 (145/144/100/80/69/64/48 pins) PA4: CVREFB1 (145/144/100/80/69/64/48 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PA3: CMPB1 (100/64/48 pins) PA4: CVREFB1 (100/64/48 pins)

Register Symbol	Bit Symbol	RX210	RX230 and RX231
PBnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4-DS (145/144/100/80/69/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/64/48 pins)
PCnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
PDnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (145/144/100/80 pins) PD1: IRQ1 input switch (145/144/100/80 pins) PD2: IRQ2 input switch (145/144/100/80 pins) PD3: IRQ3 input switch (145/144/100 pins) PD4: IRQ4 input switch (145/144/100 pins) PD5: IRQ5 input switch (145/144/100 pins) PD6: IRQ6 input switch (145/144/100 pins) PD7: IRQ7 input switch (145/144/100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (100 pins) PD1: IRQ1 input switch (100 pins) PD2: IRQ2 input switch (100 pins) PD3: IRQ3 input switch (100 pins) PD4: IRQ4 input switch (100 pins) PD5: IRQ5 input switch (100 pins) PD6: IRQ6 input switch (100 pins) PD7: IRQ7 input switch (100 pins)
	ASEL	Reserved	Analog function select
PEnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS input switch (145/144/100/80/69/64/48 pins) PE5: IRQ5 input switch (145/144/100/80/69/64 pins) PE6: IRQ6 input switch (145/144/100 pins) PE7: IRQ7 input switch (145/144/100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 input switch (100/64/48 pins) PE5: IRQ5 input switch (100/64 pins) PE6: IRQ6 input switch (100 pins) PE7: IRQ7 input switch (100 pins)

Register Symbol	Bit Symbol	RX210	RX230 and RX231
	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PE0:AN008 (145/144/100/80/69/64 pins) PE1:AN009 or CMPB0 (145/144/100/80/69/64/48 pins) PE2:AN010 or CVREFB0 (145/144/100/80/69/64/48 pins) PE3:AN011 or CMPA1 (145/144/100/80/69/64/48 pins) PE4:AN012 or CMPA2 (145/144/100/80/69/64/48 pins) PE5:AN013 (145/144/100/80/69/64 pins) PE6:AN014 (145/144/100 pins) PE7:AN015 (145/144/100 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PE0:AN016 (100/64 pins) PE1:AN017 or CMPB0 (100/64/48 pins) PE2:AN018 or CVREFB0 (100/64/48 pins) PE3:AN019 (100/64/48 pins) PE4:AN020 (100/64/48 pins) PE5:AN021 (100/64 pins) PE6:AN022 (100 pins) PE7:AN023 (100 pins)
PF5PFS	-	PF5 Pin Function Control Registers	Not available
PHnPFS (n = 0 to 3)	PSEL	Pin Function Select (PSEL[3:0]) b3 to b0	Pin Function Select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PH1: IRQ0 input switch (145/144/100/80/69/64/48 pins) PH2: IRQ1 input switch (145/144/100/80/69/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PH1: IRQ0 (100/64/48 pins) PH2: IRQ1 (100/64/48 pins)
PJnPFS (n = 1 or 3) (RX210) (n = 3) (RX230 and RX231)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
PKnPFS (n = 2 to 5)	-	PKn Pin Function Control Registers	Not available

4.4.18 Multi-Function Timer Pulse Unit 2

Table 4.49 lists the difference in multi-function timer pulse unit 2.

Table 4.49 Difference in Multi-Function Timer Pulse Unit 2

Item	RX210	RX230 and RX231
Clock source	Peripheral module clock (PCLKB)	Peripheral module clock (PCLKA)

4.4.19 Realtime Clock

Table 4.50 lists the differences in the realtime clock. Table 4.51 lists the differences in registers related to the realtime clock.

Table 4.50 Differences in the Realtime Clock

Item	RX210	RX230 and RX231
Count modes	Calendar count mode —	Calendar count mode Binary count mode
Clock output	1 Hz	1 Hz/64 Hz
Interrupts	Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt.	Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt.

Table 4.51 Differences in Registers Related to the Realtime Clock

Register Symbol	Bit Symbol	RX210	RX230 and RX231
RCR1	RTCOS	Reserved	RTCOUT output select
RCR2	CNTMD	Reserved	Count mode select
BCNT0	—	Not available	Binary counter 0
BCNT1	—	Not available	Binary counter 1
BCNT2	—	Not available	Binary counter 2
BCNT3	—	Not available	Binary counter 3
BCNT0AR	—	Not available	Binary counter 0 alarm register
BCNT1AR	—	Not available	Binary counter 1 alarm register
BCNT2AR	—	Not available	Binary counter 2 alarm register
BCNT3AR	—	Not available	Binary counter 3 alarm register
BCNT0AER	—	Not available	Binary counter 0 alarm enable register
BCNT1AER	—	Not available	Binary counter 1 alarm enable register
BCNT2AER	—	Not available	Binary counter 2 alarm enable register
BCNT3AER	—	Not available	Binary counter 3 alarm enable register
BCNT0CPy	—	Not available	BCNT0 Capture Register y (y = 0 to 2)
BCNT1CPy	—	Not available	BCNT1 Capture Register y (y = 0 to 2)
BCNT2CPy	—	Not available	BCNT2 Capture Register y (y = 0 to 2)
BCNT3CPy	—	Not available	BCNT3 Capture Register y (y = 0 to 2)

4.4.20 Independent Watchdog Timer

Table 4.52 lists the difference in the independent watchdog timer. Table 4.53 lists the differences in I/O registers related to the independent watchdog timer.

Table 4.52 Difference in the Independent Watchdog Timer

Item	RX210	RX230 and RX231
Clock source	IWDTCLK (125 kHz)	IWDTCLK (15 kHz)

Table 4.53 Differences in I/O Registers Related to the Independent Watchdog Timer

Register Symbol	Bit Symbol	RX210	RX230 and RX231
IWDTCR	TOPS[1:0]	Time-out period selection 00: 1024 cycles (03FFh) 01: 4096 cycles (0FFFh) 10: 8192 cycles (1FFFh) 11: 16384 cycles (3FFFh)	Timeout period select 00: 128 cycles (007Fh) 01: 512 cycles (01FFh) 10: 1024 cycles (03FFh) 11: 2048 cycles (07FFh)
IWDTCSTPR	SLCSTP	Sleep mode count stop control 0: Count stop is disabled 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode	Sleep-mode count stop control 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.

4.4.21 Serial Communications Interface

Table 4.54 lists the differences in the serial communications interface. Table 4.55 lists the differences in I/O registers related to the serial communications interface.

Table 4.54 Differences in the Serial Communications Interface

Item		RX210	RX230 and RX231
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Start-bit detection	Low level only	Low level or falling edge is selectable.
	Double-speed mode	Not available	Baud rate generator double-speed mode is selectable.
Bit rate modulation function		Not available	Available

Table 4.55 Differences in I/O Registers Related to the Serial Communications Interface

Register Symbol	Bit Symbol	RX210	RX230 and RX231
RDRH, RDRL, RDRHL	—	Not available	Receive data register H, L, HL
TDRH, TDRL, TDRHL	—	Not available	Transmit data register H, L, HL
SMR (SCMR.SMIF = 0)	CHR	Character length (Valid only in asynchronous mode) — — 0: Selects 8 bits as the data length 1: Selects 7 bits as the data length	Character length (Valid only in asynchronous mode) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
SSR	RDRF	Reserved	Receive Data Full Flag
	TDRE	Reserved	Transmit Data Empty Flag
SCMR	CHR1	Reserved	Character length 1
MDDR	—	Not available	Modulation duty register
SEMR	BRME	Reserved	Bit rate modulation enable
	BGDM	Reserved	Baud rate generator double-speed mode select
	RXDESEL	Reserved	Asynchronous start bit edge detection select
CR2	BCCS[1:0]	Bus collision detection clock select — 00: SCI base clock 01: SCI base clock frequency divided by 2 10: SCI base clock frequency divided by 4 11: Setting prohibited —	Bus collision detection clock select • When SEMR.BGDM = 0 or SEMR.BGDM = 1 and SMR.CKS[1:0] = a value other than 00b 00: SCI base clock 01: SCI base clock frequency divided by 2 10: SCI base clock frequency divided by 4 11: Setting prohibited • When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b 00: SCI base clock frequency divided by 2 01: SCI base clock frequency divided by 4 10: Setting prohibited 11: Setting prohibited

4.4.22 I²C Bus Interface

Table 4.56 lists the differences in registers related to the I²C bus interface.

Table 4.56 Differences in I/O Registers Related to the I2C Bus Interface

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ICMR2	TMWE	Timeout internal counter write enable	Reserved
TMOCNT	—	Timeout internal counter	Not available

4.4.23 Serial Peripheral Interface

Table 4.57 lists the difference in the serial peripheral interface. Table 4.58 lists the difference in the I/O register related to the serial peripheral interface.

Table 4.57 Difference in the Serial Peripheral Interface

Item	RX210	RX230 and RX231
RSPCK auto-stop function	Not available	Available

Table 4.58 Difference in the I/O Register Related to the Serial Peripheral Interface

Register Symbol	Bit Symbol	RX210	RX230 and RX231
SPSR	SPTEF	Reserved	Transmit Buffer Empty Flag
	SPRF	Reserved	Receive Buffer Full Flag
SPCR2	SCKASE	Reserved	RSPCK auto-stop function enable Enable

4.4.24 12-Bit A/D Converter

Table 4.59 lists the differences in the 12-bit A/D converter. Table 4.60 lists the differences in I/O registers related to the 12-bit A/D converter.

Table 4.59 Differences in the 12-Bit A/D Converter

Item	RX210	RX230 and RX231
Input channels	16 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage High-potential/low- potential reference voltage can be selected
Conversion time	1.0 μs per channel (when A/D conversion clock ADCLK = 50 MHz)	0.83 μs per channel (when A/D conversion clock ADCLK = 54 MHz)
Data registers	• 16 registers for analog input • 1 register for A/D-converted data duplication in double trigger mode — • 1 register for temperature sensor output • 1 register for internal reference voltage — • The results of A/D conversion are stored in 12-bit A/D data registers. • In addition mode, A/D conversion results are added and the added value is stored in A/D data registers as 14-bit data. • A/D conversion data of one selected analog input channel is stored into A/D data register y when conversion is started by the first trigger and into the duplication register when started by the second trigger.	• 24 registers for analog input • 1 register for A/D-converted data duplication in double trigger mode • 2 registers for A/D-converted data duplication during extended operation in double trigger mode • 1 register for temperature sensor output • 1 register for internal reference voltage • 1 register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • In A/D-converted value addition/average mode, A/D conversion results are added and the added value is stored in the A/D data registers in the number of bits for conversion accuracy + 2 bits*. • The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.
Operating modes	• Single scan mode • Continuous scan mode • Group scan mode	• Single scan mode • Continuous scan mode • Group scan mode • Group scan mode (when group A is given priority)

Item	RX210	RX230 and RX231
Conditions for A/D conversion start	• Software trigger • Synchronous trigger • Trigger by MTU, ELC, or temperature sensor • Asynchronous trigger A/D conversion can be triggered from the ADTRG0# pin.	• Software trigger • Synchronous trigger • Trigger by the MTU, ELC, and TPU • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (0.25 V ≤ analog voltage input ≤ AVCC0 - 0.25 V) • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode • Analog input disconnection detection assist • Double trigger mode (duplication of A/D conversion data) — —	— — • Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (Discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Compare function (window A and window B) • 16 ring buffers when the compare function is used
Event link function	• An ELC event can be generated on completion of scans except for group B scan in group scan mode. — — • A/D conversion can be started by the trigger from ELC.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.

Note: * The number of extended bits during addition differs depending on the A/D conversion accuracy and the addition count.
2-bit extension: A/D conversion accuracy = 1-time to 4-time conversion (addition zero to three times)
4-bit extension: A/D conversion accuracy = 16-time conversion in 12-bit mode (addition 15 times)

Table 4.60 Differences in I/O Registers Related to the 12-Bit A/D Converter

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ADDRy	—	A/D data registers y (y = 0 to 15)	A/D data registers y (y = 0 to 7, 16 to 31)
ADCSR	DBLANS [4:0]	A/D Conversion Data Duplication Channel Select	Double Trigger Channel Select
		00000: AN000	00000: AN000
		00001: AN001	00001: AN001
		00010: AN002	00010: AN002
		00011: AN003	00011: AN003
		00100: AN004	00100: AN004
		00101: AN005	00101: AN005
		00110: AN006	00110: AN006
		00111: AN007	00111: AN007
		01000: AN008	—
		01001: AN009	—
		01010: AN010	—
		01011: AN011	—
		01100: AN012	—
		01101: AN013	—
		01110: AN014	—
		01111: AN015	—
		—	10000: AN016
		—	10001: AN017
		—	10010: AN018
		—	10011: AN019
		—	10100: AN020
		—	10101: AN021
		—	10110: AN022
		—	10111: AN023
		—	11000: AN024
		—	11001: AN025
		—	11010: AN026
		—	11011: AN027
		—	11100: AN028
		—	11101: AN029
		—	11110: AN030
		—	11111: AN031
	ADHSC	Reserved	A/D conversion select
ADANSA	—	A/D channel select register A	Not available
ADANSA0	ANSA0[7:0]	Not available	A/D channel select register A0
ADANSA1	ANSA1 [15:0]	Not available	A/D channel select register A1
ADANSB	ANSB[15:0]	A/D channel select register B	Not available
ADANSB0	ANSB0[7:0]	Not available	A/D channel select register B0
ADANSB1	ANSB1 [15:0]	Not available	A/D channel select register B1
ADADS	ADS[15:0]	A/D-converted value addition mode select register	Not available

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ADADS0	ADS0[7:0]	Not available	A/D-converted value addition/average function select register 0
ADADS1	ADS1[15:0]	Not available	A/D-converted value addition/average function select register 1
ADADC	ADC	Addition count select ([1:0]) 00: 1-time conversion (no addition; same as normal conversion) 01: 2-time conversion (addition once) 10: 3-time conversion (addition twice) 11: 4-time conversion (addition three times)	Addition count select ([2:0]) 000: 1-time conversion (no addition; same as normal conversion) 001: 2-time conversion (addition once) 010: 3-time conversion (addition twice) 011: 4-time conversion (addition three times) 101: 16-time conversion (addition 15 times)
	AVEE	Reserved	Average mode enable
ADSTRGR	TRSB	A/D conversion start trigger select for group B ([3:0]) 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN 0110: TRG4AN 0111: TRG4BN 1000: TRG4ABN 1001: Trigger from the ELC —* —* —	A/D conversion start trigger select for group B ([5:0]) 000001: TRG0AN 000010: TRG0BN 000011: TRGAN 000100: TRG0EN 000101: TRG0FN 000110: TRG4AN 000111: TRG4BN 001000: TRG4ABN 001001: Trigger from ELC 001101: TRGAN1 001110: TRG4ABN1 111111: No trigger selected
	TRSA	A/D conversion start trigger select ([3:0]) 0000: ADTRG0# 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN 0110: TRG4AN 0111: TRG4BN 1000: TRG4ABN 1001: ELC —* —* 1010: Trigger from temperature sensor	A/D conversion start trigger select ([5:0]) 000000: ADTRG0# 000001: TRG0AN 000010: TRG0BN 000011: TRGAN 000100: TRG0EN 000101: TRG0FN 000110: TRG4AN 000111: TRG4BN 001000: TRG4ABN 001001: Trigger from ELC 001101: TRGAN1 001110: TRG4ABN1 — 111111: No trigger selected

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ADEXICR	TSSAD	Reserved	Temperature sensor output A/D converted value addition/average mode select
	OCSAD	Internal reference voltage A/D converted value addition mode select	Internal reference voltage A/D converted value addition/average mode select
	TSS (RX210) TSSA (RX231)	Temperature sensor output A/D conversion select	Temperature sensor output A/D conversion select
	OCS (RX210) OCSA (RX231)	Internal reference voltage A/D conversion select	Internal reference voltage A/D conversion select
ADSHCR	—	A/D sample and hold circuit control register	Not available
ADELCCR	—	Not available	A/D event link control register
ADGSPCR	—	Not available	A/D group scan priority control register
ADCMPCR	—	Not available	A/D compare control register
ADCMPANSR0	—	Not available	A/D compare function window A channel select register 0
ADCMPANSR1	—	Not available	A/D compare function window A channel select register 1
ADCMPANSER	—	Not available	A/D compare function window A extended input select register
ADCMPLR0	—	Not available	A/D compare function window A comparison condition setting register 0
ADCMPLR1	—	Not available	A/D compare function window A comparison condition setting register 1
ADCMPLER	—	Not available	A/D compare function window A extended input comparison condition setting register
ADCMPDR0	—	Not available	A/D compare function window A lower-side level setting register
ADCMPDR1	—	Not available	A/D compare function window A upper-side level setting register
ADCMPSR0	—	Not available	A/D compare function window A channel status register 0
ADCMPSR1	—	Not available	A/D compare function window A channel status register 1
ADCMPSER	—	Not available	A/D compare function window A extended input channel status register
ADHVREFCNT	—	Not available	A/D high-potential/low-potential reference voltage control register
ADWINMON	—	Not available	A/D compare function window A/B status monitor register

Register Symbol	Bit Symbol	RX210	RX230 and RX231
ADCMPBNSR	—	Not available	A/D compare function window B channel select register
ADWINLLB	—	Not available	A/D compare function window B lower-side level setting register
ADWINULB	—	Not available	A/D compare function window B upper-side level setting register
ADCMPBSR	—	Not available	A/D compare function window B status register
ADBUFn (n = 0 to 15)	—	Not available	A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	Not available	A/D data storage buffer enable register
ADBUFPTR	—	Not available	A/D data storage buffer pointer register

Note: * The trigger presents only in products with 144 or more pins.

4.4.25 12-Bit D/A Converter

Table 4.61 lists the differences in the 12-bit D/A converter. Table 4.62 lists the differences in I/O registers related to the 12-bit D/A converter.

Table 4.61 Differences in the 12-Bit D/A Converter

Item	RX210	RX230 and RX231
Resolution	10 bits	12 bits
Output channels	Two channels	Two channels
Conversion time	1.0 μs per channel (when A/D conversion clock ADCLK = 50 MHz)	0.83 μs per channel (when A/D conversion clock ADCLK = 54 MHz)
Countermeasure against mutual interference between analog modules	Not available	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter. Therefore, degradation of A/D conversion accuracy caused by interference is reduced by controlling the 12-bit D/A converter inrush current generation timing with the enable signal.
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function (input)	DA0 conversion can be started when an event signal is input.	D/A0 conversion can be started when an event signal is input.

Table 4.62 Differences in I/O Registers Related to the 12-Bit D/A Converter

Register Symbol	Bit Symbol	RX210	RX230 and RX231
DADRm (m = 0 or 1)	—	D/A data register m (m = 0 or 1) 10 bits are valid for both left and right aligned data.	D/A data register m (m = 0 or 1) 12 bits are valid for both left and right aligned data.
DACR	DAE	D/A enable	Not available
DAADSCR	—	Not available	D/A A/D synchronous start control register
DAVREFCR	—	Not available	D/A VREF control register

4.4.26 Temperature Sensor

Table 4.63 lists the difference in the temperature sensor. Table 4.64 lists the difference in the register related to the temperature sensor.

Table 4.63 Difference in the Temperature Sensor

Item	RX210	RX230 and RX231
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA).	The temperature sensor outputs a voltage to the 12-bit A/D converter via a gain amplifier.
Power consumption reduction function	Module stop state can be set.	Not available

Table 4.64 Difference in the Register Related to the Temperature Sensor

Register Symbol	Bit Symbol	RX210	RX230 and RX231
TSCR	—	Temperature sensor control register	Not available

4.4.27 Comparator B

Table 4.65 lists the differences in comparator B. Table 4.66 lists the differences in the I/O registers related to the comparator B.

Table 4.65 Differences in Comparator B

Item	RX210	RX230 and RX231
Analog input voltage	Input voltage to the CMPBn pin (n = 0 or 1)	Input voltage to the CMPBn pin (n = 0 to 3)
Reference input voltage	Input voltage to the CVREFBn pin (n = 0 or 1)	Input voltage to the CVREFBn pin (n = 0 to 3) or internal reference voltage
Comparison result	Read from the CPBFLG.CPBiOUT flag (i = 0 or 1)	Read from the CPBFLG.CPBnOUT flag (n = 0 to 3) The comparison result can be output to the CMPOBn pin (n = 0 to 3).
Interrupt request generation timing	When comparator B0 comparison result changes When comparator B1 comparison result changes	When comparator B0 comparison result changes When comparator B1 comparison result changes When comparator B2 comparison result changes When comparator B3 comparison result changes
Event generation timing to ELC	When comparator B0 comparison result changes When comparator B0 or comparator B1 comparison result changes	When comparator B0 comparison result changes When comparator B0 or comparator B1 comparison result changes
Selectable functions	• Digital filter function Whether to use the digital filter can be selected. The sampling frequency can be selected. — — —	• Digital filter function Whether to use the digital filter can be selected. The sampling frequency can be selected. • Reference input voltage CVREFn pin input or internal reference voltage (generated internally) can be selected (n = 0 to 3). • Window function Whether to enable or disable the window function (low-side reference (VRFL)) < CMPBn (n = 0 to 3) < high-side reference (VRFH)) can be selected. • Comparator B response speed High-speed mode/low-speed mode can be selected.

Table 4.66 Differences in the I/O Registers Related to the Comparator B

Register Symbol	Bit Symbol	RX210	RX230 and RX231
CPB1CNT1	—	Not available	Comparator B1 control register 1
CPBCNT2	—	Not available	Comparator B control register 2
CPB1CNT2	—	Not available	Comparator B1 control register 2
CPBFLG	CPB0OUT	Comparator B0 monitor flag — 0: CMPB0 < CVREFB0 1: CMPB0 > CVREFB0 —	Comparator B0 monitor flag • When the window function is disabled 0: CMPB0 < CVREFB0, CMPB0 < internal reference voltage, or comparator B0 operation disabled 1: CMPB0 > CVREFB0, or CMPB0 > internal reference voltage • When the window function is enabled 0: CMPB0 < low-side reference (VRFL), CMPB0 > high-side reference (VRFH), or comparator B0 operation disabled 1: Low-side reference (VRFL) < CMPB0 < high-side reference (VRFH)
	CPB1OUT	Comparator B1 monitor flag — 0: CMPB1 < CVREFB1 1: CMPB1 > CVREFB1 —	Comparator B1 monitor flag • When the window function is disabled 0: CMPB1 < CVREFB1, CMPB1 < internal reference voltage, or comparator B1 operation disabled 1: CMPB1 > CVREFB1, or CMPB1 > internal reference voltage • When the window function is enabled 0: CMPB1 < low-side reference (VRFL), CMPB1 > high-side reference (VRFH), or comparator B1 operation disabled 1: Low-side reference (VRFL) < CMPB1 < high-side reference (VRFH)
CPB1FLG	—	Not available	Comparator B1 flag register
CPB1INT	—	Not available	Comparator B1 interrupt control register
CPB1F	—	Not available	Comparator B1 filter select register
CPBMD	—	Not available	Comparator B mode select register
CPB1MD	—	Not available	Comparator B1 mode select register
CPBREF	—	Not available	Comparator B reference input voltage select register

Register Symbol	Bit Symbol	RX210	RX230 and RX231
CPB1REF	—	Not available	Comparator B1 reference input voltage select register
CPBOCR	—	Not available	Comparator B output control register
CPB1OCR	—	Not available	Comparator B1 output control register

4.4.28 Data Operation Circuit

Table 4.67 lists the differences in the data operation circuit.

Table 4.67 Differences in the Data Operation Circuit

Item	RX210	RX230 and RX231
Data operation function	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Lower power consumption function	Module stop state can be set.	Module stop state can be set.
Interrupts	• The condition selected by the DOCR.DCSEL bit being met • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h
Event link function (output)	—	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

4.4.29 ROM (flash memory for code storage)

Table 4.68 lists the differences in the flash memory.

Refer to User's Manual: Hardware listed in 5. Reference documents for details on the flash memory specifications of the RX210 Group, RX230 Group, and RX231 Group.

Table 4.68 Differences in the Flash Memory

Item	RX210	RX230 and RX231
Memory space	User area: Up to 1024 Kbytes Data area: 8 Kbytes User boot area: 16 Kbytes	User area: Up to 256 Kbytes (RX230) Up to 512 Kbytes (RX231) Data area: 8 Kbytes —
Value after erase	ROM: FFh E2 DataFlash: Undefined	ROM: FFh E2 DataFlash: FFh
Units of programming and erasure	• Units of programming User area: 2, 8, or 128 bytes Data area: 2 or 8 bytes User boot area: 2, 8, or 128 bytes • Units of erasure User area: In block units Data area: 128 bytes User boot area: 16 Kbytes	• Units of programming User area: 8 bytes Data area: 1 byte — • Units of erasure User area: In block units Data area: In block units —
On-board programming	• Boot mode SCI1 is used for reprogramming FINE is used for reprogramming — • User boot mode • Single-chip mode	• Boot mode SCI1 is used for reprogramming FINE is used for reprogramming USB0 is used for reprogramming — • Single-chip mode
Interrupts	FIFERR and FRDYI interrupts	FRDYI interrupt
Protection	• Protection by setting the I/O registers related to the flash memory • Lock bit protection (only in the user area) —	• Protection by setting the I/O register related to the flash memory — • Area protection
Start-up program protection	Not available	Available
ROM (flash memory for code storage) characteristics	• Reprogramming/erasure cycle [Chip version A] 1,000 times (min.) [Chip versions B and C] 10,000 times (min.) • Data hold time [Chip version A] 1,000 times/10 years (min.) [Chip versions B and C] 1,000 times/30 years (min.) 10,000 times/ 1 year (min.)	• Reprogramming/erasure cycle — 1,000 times (min.) — • Data hold time — 1,000 times/ 20 years (min.) —

Item	RX210	RX230 and RX231
E2 DataFlash characteristics (flash memory for data storage)	• Reprogramming/erasure cycle 100,000 times (min.) — • Data hold time [Chip version A] 100,000 times/10 years (min.) [Chip versions B and C] 100,000 times/30 years (min.)	• Reprogramming/erasure cycle 100,000 times (min.) 1,000,000 times (typ.) • Data hold time — 10,000 times/ 20 years (min.) 100,000 times/ 5 years (min.) 1,000,000 times/ 1 year (typ.) —

Note: RX231 Group only. Not implemented on the RX230 Group.

4.4.30 E2 DataFlash Memory (flash memory for data storage)

Table 4.69 shows a comparative overview of the flash memory (Data flash) specifications.

Table 4.69 Comparative Overview of Flash Memory (Data Flash) Specifications

Item	RX210	RX230 and RX231
Memory capacity	8 Kbytes	8 Kbytes
Value after erasure	Undefined	FFh
Block configuration	Block: 128 bytes	Block: 1Kbytes
Number of blocks	64	8

4.4.31 Package (LFQFP48/64/100 only)

There are some differences in the outline drawing of the LFQFP48, LFQFP64, LQFP100 package, so please be careful when designing the board.

For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 4.70 Comparison of package codes

Item	RX210	RX230 and RX231
48 pin LFQFP	PLQP0048KB-A	PLQP0048KB-B
64 pin LFQFP	PLQP0064KB-A	PLQP0064KB-C
100 pin LFQFP	PLQP0100KB-A	PLQP0100KB-B

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ0150)
RX230 Group and RX231 Group User's Manual: Hardware Rev.1.20 (R01UH0496EJ0120)
The latest versions can be downloaded from the Renesas Electronics website.

On-Chip Debugging Emulator

E1/E20 Emulator Additional Document for User's Manual (RX User System Design) (R20UT0399EJ)
The latest version can be downloaded from the Renesas Electronics website.

Complier

RX Family C/C++ Compiler CC-RX V2.03.00 User's Manual (R20UT3248EJ)
The latest version can be downloaded from the Renesas Electronics website.

Application Note

RX231 Group Application Note Initial Setting (R01AN2185EJ)
Migration Design Guide between RX Families: Package Dimensions Difference (R01AN4591EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The technical updates issued after each referenced user manual are not reflected in this application note, so obtain latest version from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug 27, 2015	-	First edition issued
1.10	May. 8, 2019	Whole	Confirmed the contents of the description again (Addition of description mistake etc.)
		35	Add memory map comparison of address space
		39	Add area comparison of option setting memory
		50	Add Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode
		59	Add differences in registers related to register write protection function
		60	Add comparison of exception handling
		72	Add comparative listing of functions assigned to each multiplexed pin
		83	Add comparison of pin function control register
		101	Add comparison of data operation circuit
		103	Add comparison of flash memory (Data Flash)
		104	Add differences in package external form

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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