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April 1st, 2010
Renesas Electronics Corporation

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M16C/Tiny Series

Memory to Memory DMA Transfer

1. Abstract

The following are steps for changing both source address and destination address to transfer data from memory to another. The DMA transfer utilizes the workings that assign a higher priority to the DMA0 transfer if transfer requests simultaneously occur in two DMA channels.

Use the following peripheral functions:
- Timer mode of timer A
- Two DMAC channels
- One-byte temporary RAM (address 0400_{16})

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

This program can be used for the other M16C Families which have the same SFR (Special Function Register) as the one in the M16C/26, M16C/26A, M16C/28, M16C/29 However, since some functions may be modified such as added functions, check it in a manual. Execute sufficient evaluation when using this application note.

3. Explain of Example Usage

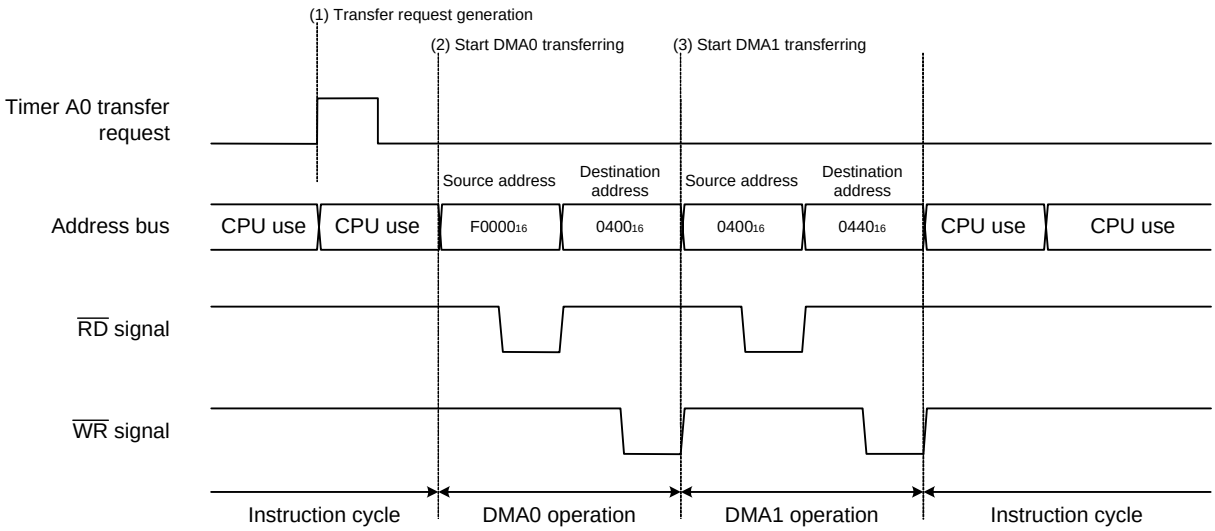
3.1 Specifications

(1) Transfer the content of memory extending over 128 bytes from address $F0000_{16}$ to a 128-byte area starting from address 0440_{16}. Transfer the content every time a timer A0 interrupt request occurs.
(2) Use DMA0 for a transfer from the source to temporary RAM, and DMA1 for a transfer from temporary RAM to the destination.

3.2 Operation

(1) A timer A interrupt request occurs. Though both a DMA0 transfer request and a DMA1 transfer request occur simultaneously, the former is executed first.
(2) DMA0 receives a transfer request and transfers data from the source to the temporary RAM. At this time, the source address is incremented.
(3) Next, DMA1 receives a transfer request and transfers data involved from temporary RAM to the destination. At this time, the destination address is incremented.

Figure 1 shows the operation timing, Figure 2 shows the block diagram.



Note 1: The DMA0 operation and DMA1 operation are not necessarily executed in succession due to the a cycle steal operation.
Note 2: The instruction cycle varies from instruction to instruction.
Note 3: Since the parts of the $\overline{RD}$ and $\overline{WR}$ signals shown in short-dash lines vary in step with writing to the internal RAM, waveforms are not output to the $\overline{RD}$ and $\overline{WR}$ pins.

Figure 1. Operation Timing of Memory to Memory DMA Transfer

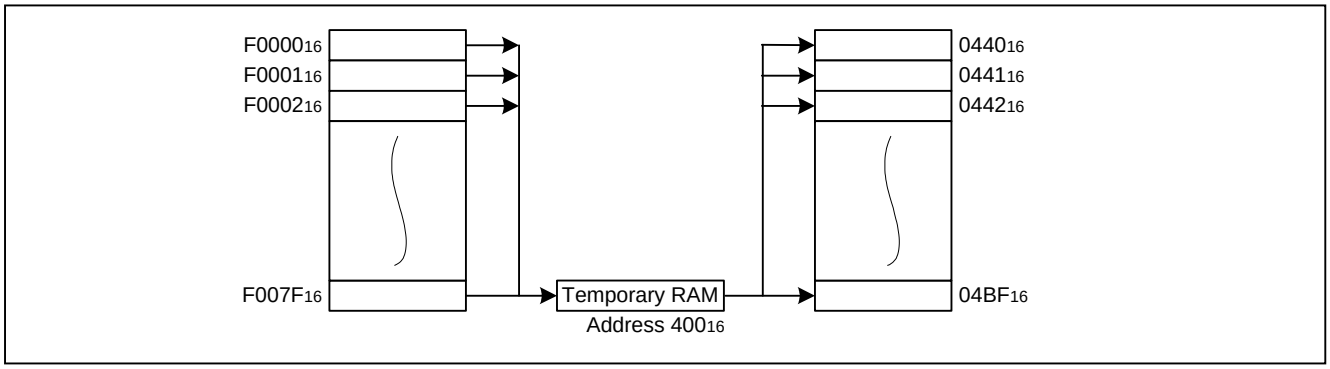


Figure 2. Block Diagram of Memory to Memory DMA Transfer

3.3 Register Setting

To enable the operation defined in "Section 3. Operation of A/D Converter", the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/26 Group hardware manual, M16C/26A Group hardware manual, M16C/28 Group hardware manual, M16C/29 Group hardware manual.

(1) Setting timer A0 mode register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0 0

TMOD1,TMOD0 Operation Mode Select Bit
00: Selection of timer mode

MR0 Pulse Output Function Select Bit
0: Pulse is not output (TA0OUT pin is a normal port pin)

MR2,MR1 Gate Function Select Bit
00 : Gate function not available
01 : (TA0IN pin is a normal port pin)

MR3 Set to "0" in timer mode

TCK1,TCK0 Count Source Select Bit
00 : f1 or f2
01 : f8
10 : f32
11 : fC32

b7	b6	Count source	Count source period f(XIN): 20MHz f(XCIN): 32.768kHz
0	0	f1 (Note 1)	50ns
0	0	f2 (Note 1)	100ns
0	1	f8	400ns
1	0	f32	1600ns
1	1	fC32	976.56µs

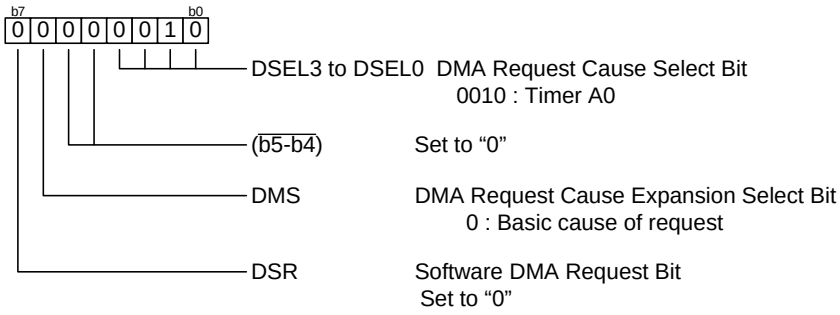
Note 1: Count source is f2 if PCLK0 bit in the PCLKR register is "0", f1 if PCLK0 bit in the PCLKR register is "1".

(2) Setting timer A0 register

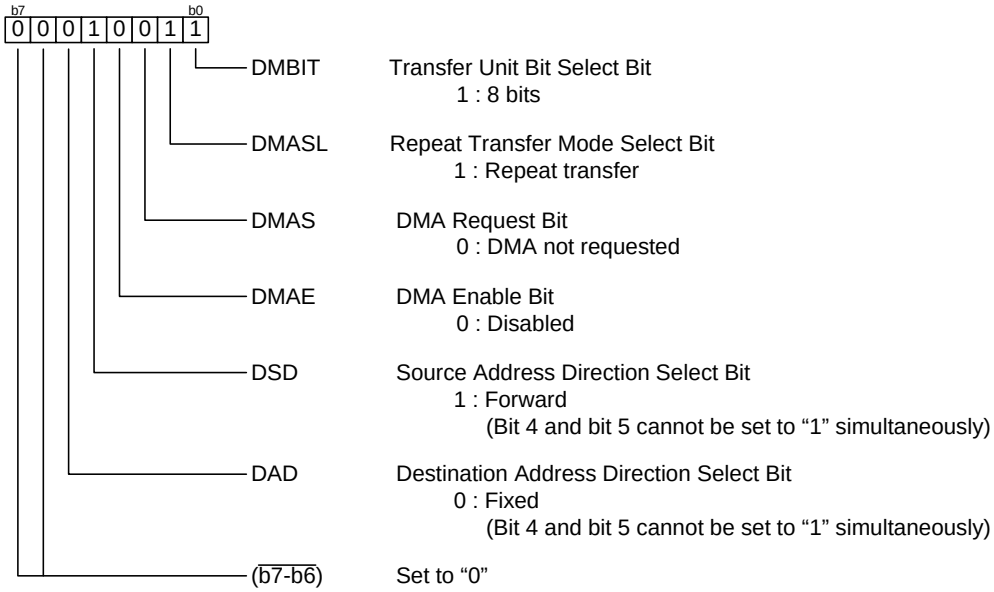
(b15) b7 | (b8) b0 | b7 b0
4E16 | 1F16

Can be set to 000016 to FFFF16

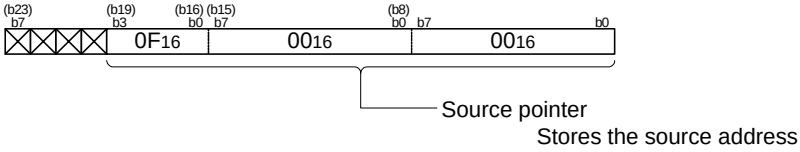
(3) Setting DMA0 request cause select register



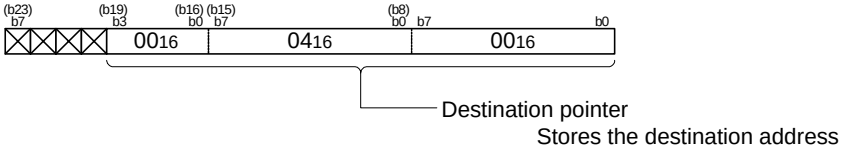
(4) Setting DMA0 control register



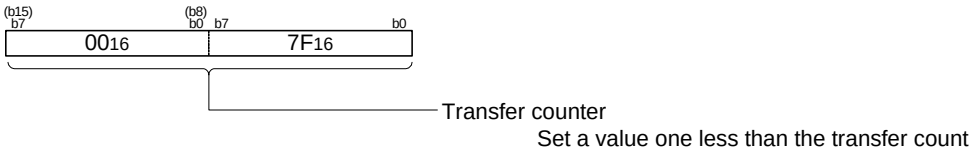
(5) Setting DMA0 source pointer



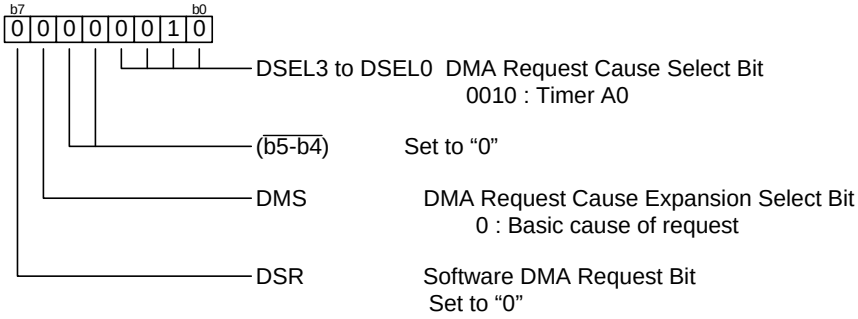
(6) Setting DMA0 destination pointer



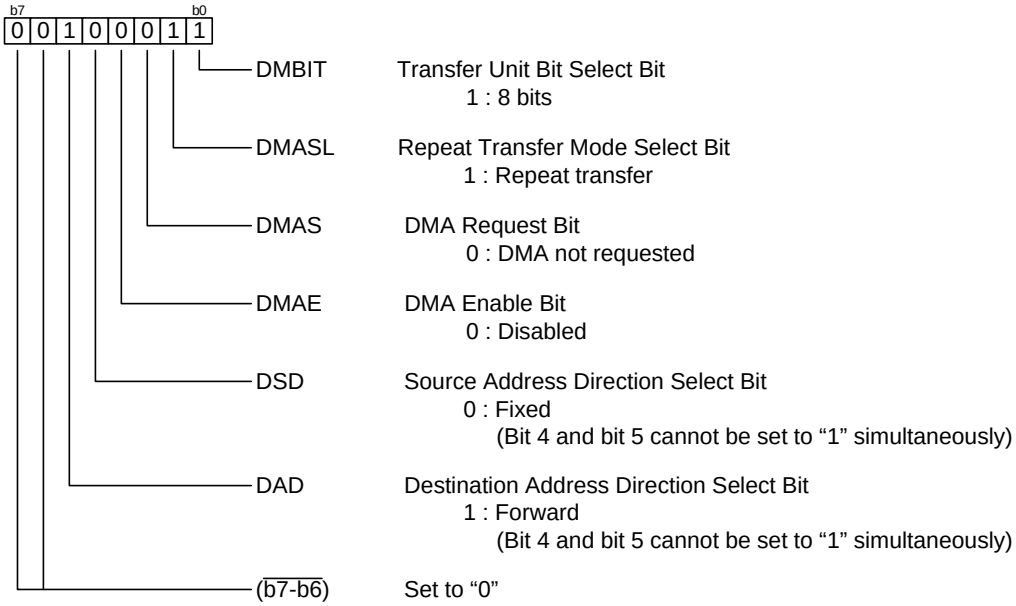
(7) Setting DMA0 transfer counter



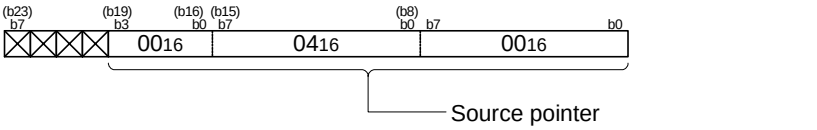
(8) Setting DMA1 request cause select register



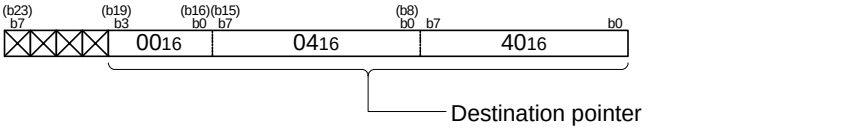
(9) Setting DMA1 control register



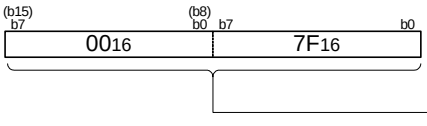
(10) Setting DMA1 source pointer



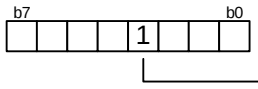
(11) Setting DMA1 destination pointer



(12) Setting DMAi transfer counter

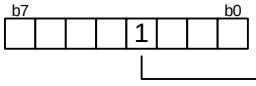


(13) DMA enable (Setting DMA0 control register)



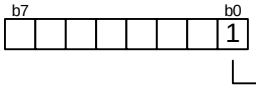
DMAE DMA Enable Bit
1 : Enabled

(14) DMA enable (Setting DMA1 control register)



DMAE DMA Enable Bit
1 : Enabled

(15) Setting count start flag



TA0S Timer A0 Count Start Flag

4. Sample Program

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Aplicatoin of DMAC                         *
 *               (Memory to Memory DMA transfer)            *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/***************************
 *   include file          *
 ***************************/
#include "sfr28.h"

/***************************
 *   Function Definition   *
 ***************************/
voidtimerA0_init(void);

/*************************************
 * Global variable declaration       *
 *************************************/
const static char src_data[] = {
    0x01,0x02,0x03,0x04,0x05,0x06,0x07,0x08,0x09,0x0a,0x0b,0x0c,0x0d,0x0e,0x0f,0x10,
    0x11,0x12,0x13,0x14,0x15,0x16,0x17,0x18,0x19,0x1a,0x1b,0x1c,0x1d,0x1e,0x1f,0x20,
    0x21,0x22,0x23,0x24,0x25,0x26,0x27,0x28,0x29,0x2a,0x2b,0x2c,0x2d,0x2e,0x2f,0x30,
    0x31,0x32,0x33,0x34,0x35,0x36,0x37,0x38,0x39,0x3a,0x3b,0x3c,0x3d,0x3e,0x3f,0x40,
    0x41,0x42,0x43,0x44,0x45,0x46,0x47,0x48,0x49,0x4a,0x4b,0x4c,0x4d,0x4e,0x4f,0x50,
    0x51,0x52,0x53,0x54,0x55,0x56,0x57,0x58,0x59,0x5a,0x5b,0x5c,0x5d,0x5e,0x5f,0x60,
    0x61,0x62,0x63,0x64,0x65,0x66,0x67,0x68,0x69,0x6a,0x6b,0x6c,0x6d,0x6e,0x6f,0x70,
    0x71,0x72,0x73,0x74,0x75,0x76,0x77,0x78,0x79,0x7a,0x7b,0x7c,0x7d,0x7e,0x7f,0x80};

unsigned short   tmp;

#pragma ADDRESS dst_data 0440h
unsigned short   dst_data [128];

/***************************
 *   main                  *
 ***************************/

void main(void) {

    timerA0_init();

    dm0ic = 0;

    dm0sl = 0x02;  /* Setting DMA0 request cause select register
                DMA request cause select bit is selected to timer A0
            */

    dm0con = 0x13;   /*  Setting DMA0 control register
                         Transfer unit bit select bit is selected to 8 bit
                         Repeat transfer mode select bit is selected to repeat transfer
                         DMA request bit is set to DMA not request
                         DMA enable bit is set to disable
                         Source address direction select bit is set to forward
                         Destination address direction select bit is set to fixed
            */

    sar0_addr.byte.low  = (char)(&src_data);      /* Setting DMA0 source pointer */
    sar0_addr.byte.mid  = (char)((unsigned long)(&src_data) >> 8 );
    sar0_addr.byte.high = (char)((unsigned long)(&src_data) >> 16 );
    dar0_addr.byte.low  = (char)(&tmp);           /* Setting DMA0 destination pointer */
    dar0_addr.byte.mid  = (char)((unsigned long)(&tmp) >> 8 );
    dar0_addr.byte.high = (char)((unsigned long)(&tmp) >> 16 );
    tcr0 = 128-1;        /* Setting DMA0 transfer counter */

    dm1ic = 0;

    dm1sl = 0x02;  /*    Setting DMA0 request cause select register
                         DMA request cause select bit is selected to timer A0
```

```
            */

    dm1con = 0x23;   /*  Setting DMA0 control register
                         Transfer unit bit select bit is selected to 8 bit
                         Repeat transfer mode select bit is selected to repeat transfer
                         DMA request bit is set to DMA not request
                         DMA enable bit is set to disable
                         Source address direction select bit is set to fixed
                         Destination address direction select bit is set to forward
                     */

    sar1_addr.byte.low  = (char)(&tmp);          /* Setting DMA0 source pointer */
    sar1_addr.byte.mid  = (char)((unsigned long)(&tmp) >> 8 );
    sar1_addr.byte.high = (char)((unsigned long)(&tmp) >> 16 );
    dar1_addr.byte.low  = (char)(&dst_data);     /* Setting DMA0 destination pointer */
    dar1_addr.byte.mid  = (char)((unsigned long)(&dst_data) >> 8 );
    dar1_addr.byte.high = (char)((unsigned long)(&dst_data) >> 16 );
    tcr1 = 128-1;        /* Setting DMA0 transfer counter */

    dmae_dm0con = 1; /* DMA enabled */
    dmae_dm1con = 1; /* DMA enabled */

    ta0s = 1;            /* timer A0 start */

    while (1) {
    }
}

void timerA0_init() {

    ta0ic = 0;

    ta0mr = 0x00;        /*  Timer A0 mode register
                             Selection of tiemr mode
                             Pulse is not output (TA0OUT pin is normal pin)
                             Gate function is not available (TA0OUT pin is normal pin)
                             Cout source is f1
                         */

    ta0 = 20000-1;       /* 1msec @20MHz */
}
```

5. Reference

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Hardware Manual

M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual
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		Page	Summary
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