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M66592

Guidelines for board design (Preliminary)

Notice : This is not a final specification. Some parametric items are subject to change.

Contents

1. Summary

This document states the guidelines for USB2.0 Hi-Speed board design.

2. Introduction

The examples of application explained in this document apply to the following ASSP.

- USB device : M66592FP/WG

3. Cautions in designing the board

3.1 USB transmission lines

The USB transmission line indicates the pattern that connects the USB connector and the M66592FP/WG.
The USB2.0 has three communication modes; Hi-Speed, Full-Speed and Low-Speed modes.
The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission lines must be designed as a high-frequency circuit. Impedance control is required for the USB transmission lines.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance 90Ω (±15%).
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. As for the details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB receptacle to the M66592. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 100 mm and the difference between the pattern lengths for D+ and D- is less than 2.5 mm for generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more.
- Do not allocate other signal lines near the USB transmission line. Particularly lines of heavily fluctuating signals, such as clock and data bus lines, must be allocated far from the USB transmission line.
- Allocate the USB transmission line on the same layer without passing it through a through hole.
- Do not bend the USB transmission line at acute angles (right angles). Bend it gently.
- It is recommended to be guard-ringed the clock, reset, read, write and chip select signals with ground.
- When a resistance is connected to the USB transmission lines, allocate the part near the USB transmission lines. The connecting wire must be as short as possible.

3.2 Power supply and ground pattern

- The M66592FP/WG has following VDD and GND;
- Power supply for Analog Block : AFEA15V(1.5V), AFEA33V(3.3V)
  Power supply for Digital Block : AFED15V(1.5V), AFED33V(3.3V), VDD(1.5V), VIF(1.8V or 3.3V)
- Ground for Analog Block : AFEA15G, AFEA33G
- Ground for Digital Block : AFED15G, AFED33G, DGND
- It is recommended to separate power supplies and ground patterns into digital and analog.
- VIF of the M66592FP/WG should be same voltage with the voltage of the MCU bus interface. VIF supplies power to the lines connected with a MCU which controls the M66592FP/GW.
- Connect the power supplies and grounds firmly on wide areas. Refer to Figure 2 “GND” on page 7.
- Tantalum solid electrolytic capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as capacitors for power supplies.
- Aluminum electrolytic capacitors affect the jitter value during measurement of EYEdiagram. Use the capacitors after sufficiently designing and testing them.

3.3 Oscillation

- Allocate an oscillation circuit near XIN and XOUT of the USB device. It is recommended to guard-ring XIN and XOUT with ground.
- Customers should contact the oscillator manufacturer for the optimal oscillation circuit parameters applicable to their system.

3.4 Reset

- It is recommended to be guard-ringed the reset signal with ground. For resetting, a reset IC is recommended.

3.5 VBUS

- The USB specification recommends that a capacitor (1.0 ~ 10.0μF) should be mounted on VBUS to absorb flyback voltage generated when the USB cable is connected and disconnected. Please consider to mount a capacitor according to the capacitance of the VBUS line.

3.6 Non-connected pins

- Please refer to “Table 1.2 example of not used pins” of M66592 Datasheet (REJ03F0111).

3.7 REFRIN pin

- Allocate the reference resistor, 5.6kohm±1%, between REFRIN-pin and AFEA33G.
- Allocate the reference resistor as close as possible to M66592.
- REFRIN-pin, the reference resistor and AFEA33G should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for REFRIN-pin and AFEA33G. Then the pattern should be connected to the analog ground. The pattern should be designed avoiding the potential for common impedance between REFRIN and other signals.
- To prevent cross talk, High frequently switching signals like DP, DM, clocks, and control signals for Addresses and Data, should not be placed near by the reference resistor, and their patterns should neither get across nor go side by side with the wiring pattern between the reference resistor and REFRIN-pin.
- Wiring pattern between the reference resistor and REFRIN-pin should be guard-ringed with ground.

4. M66592 utility board M3A-0038G01

An example is shown below using the utility board M3A-0038G01 on which the M66592FP/WG has been mounted.
The package of the M66592FP is 64pin LQFP and a the package of the M66592WG is 64pin FBGA.
The M3A-0038G01 is a size of 70 mm × 80 mm × 1.6 mm and used in combination with the evaluation board M3A-0033. The M3A-0038G01 cannot operate by itself. It is possible to connect it with other boards depending on the connector specifications.
The outline of the specifications is shown as follows:

- USB device : M66592FP/WG
- Oscillation frequency : 24MHz
- Transmission speed : 480Mbps
- Board name : M3A-0038G01 (Control MCU Board M3A-0033)

4.1 USB transmission lines

The M3A-0038G01 uses a glass epoxy 4-layer board (FR4), and the USB transmission lines are passed through the first layer of the board. The pattern width is 0.35 mm, and the pattern pitch is 0.23 mm. The second layer is a ground layer, the third is a power supply layer, and the fourth is a signal and analog ground layer.

4.2 Power supply and ground pattern

The power supplies and ground patterns are separated into digital and analog.
Table 1 and Table 2 show the classifications of power supplies and grounds in the M3A-0038G01.

Table 1 Classification of M3A-0038G01power supplies

M66592 Pin name	Classification of M3A-0038G01power supplies (O indicates that these pins are connected.)			
	Analog power supply (AFEA33V)	Digital power supply 1 (AFED33V)	Digital power supply 2 (VDD)	Interface power supply (VIF)
AFEA15V			O	
AFED15V			O	
AFEA33V	O			
AFED33V		O		
VDD			O	
VIF		O (at 3.3V)		O (at 1.8V)

- Each power supply pin is provided with a 0.01µF ceramic capacitor.

Table 2 Classification of M3A-0038G01 grounds

M66592 Pin name	Classification of M3A-0038G01 grounds	
	Analog ground (AGND)	Digital ground (DGND)
AFEA15G		O
AFED15G		O
AFEA33G	O (GND of the oscillation circuit) (Reference resistor)	
AFED33G		O
DGND		O

- All the digital grounds (DGND) are solid ground plane except the areas near the USB connector on the second layer. Refer to the following Figure 1.
- The analog ground (AGND) is allocated on the fourth layer. The analog ground has almost the same shape as the analog power supply (AFEA33V) on the third layer. Refer to the following Figure 2.
- The metallic case of the USB connector is connected to the chassis ground (FGND). The chassis ground can be disconnected from the digital ground (solid ground plane) and used independently by pattern cutting of the jumper JP5 at the rear.

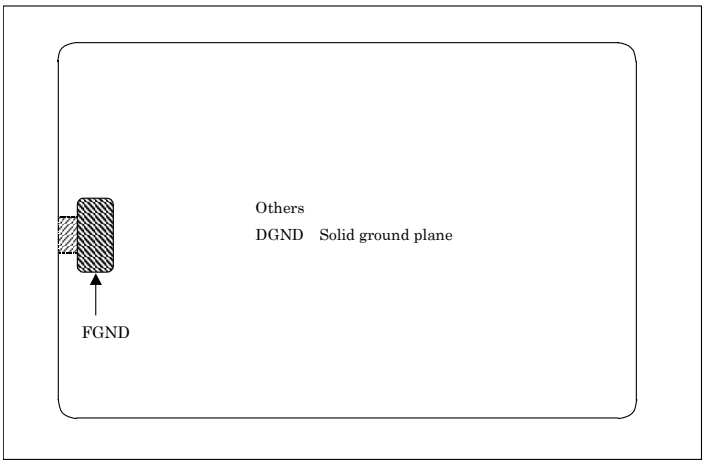

Figure 1 M3A-0038G01 second layer

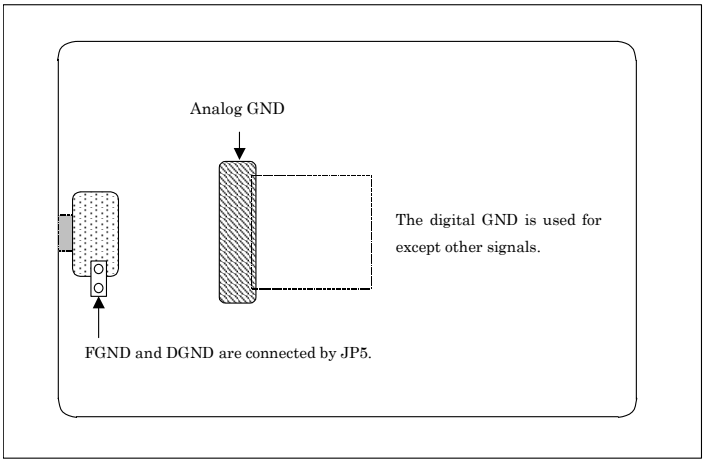

Figure 2 M3A-0038G01 fourth layer

4.3 Oscillation

The oscillation circuit of the M3A-0038G01 has a pattern on which one of the crystal oscillators made by Daishinku Corp. can be mounted among the DSX321G (or DSX630G) at 12MHz, 24MHz or 48MHz.

4.4 Reset

A 0.1μF capacitor is connected between the reset pin and ground to prevent operation errors in the M3A-0038G01.

4.5 VBUS

A 1.0μF chip monolithic ceramic capacitor is mounted between VBUS and ground in the M3A-0038G01.

4.6 Measures against EMI and measures against surge

The M3A-0038G01 provides the following pattern on the USB transmission line as an experimental pattern fort and measures against EMI measures against surge.

- Common mode choke coil(L2) : DLW21HN900SQ2 (Murata Manufacturing Co., Ltd.)
  (When the coil is mounted, the wire for L2 foot pattern should be cut.
- ESD protection diode(U2) : HZM6.2Z4MFA / HZM6.8Z4MFA (RENESAS)

Note: Though the influence on the eye diagram of these parts has been confirmed, please fully evaluate other influences in user system.

5. Reference document

- Datasheet : M66592 datasheet
- Universal Serial Bus Specification Revision 2.0 April 27,2000

6. Web site information and technical support

- Renesas USB Device : http://www.renesas.com/en/usb
- Technical support : http://www.renesas.com/eng/contact/index.html

REVISION HISTORY	M66592 Guidelines for board design

Rev.	Date	Description	
		Page	Summary
1.00	18 Feb., 2005	–	First edition issued

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