M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups
Serial Interface: Using High Speed Communication when Performing Clock Synchronous Slave Reception with DMAC

Abstract

This document describes the method of slave reception in clock synchronous serial I/O mode using high speed communication with DMAC for the M16C Group.

When the clock synchronous serial I/O mode is in slave reception mode, and continuous reception mode is used, data may not be received correctly when the transmit/receive clock becomes high speed. When communicating in high speed, data can be received correctly using DMAC instead of continuous receive mode.

Products

MCUs: M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

In this application note, the clock synchronous serial I/O mode, and two channels of DMAC are used. Data is received continually 1 byte at a time, until all 256 bytes of data are received. Continuous receive mode is not used. Write dummy data to the UiTB register, and read the received data from the UiRB register using DMAC.

If continuous receive mode is used, when the transmit/receive clock becomes high speed, the read timing for the UiRB register may not adhere to the notes in section 1.1 Notes on Clock Synchronous Serial I/O Mode, thus data may not be received correctly (refer to Figure 1.1). In using DMAC for communication, even if the transmit/receive clock operates in high speed, data can be received correctly (refer to Figure 1.2).

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Timing Diagram of Continuous Receive Mode, and Figure 1.2 shows Timing Diagram of Continuous Data Reception with DMAC.

Table 1.1   Peripheral Functions and Their Applications

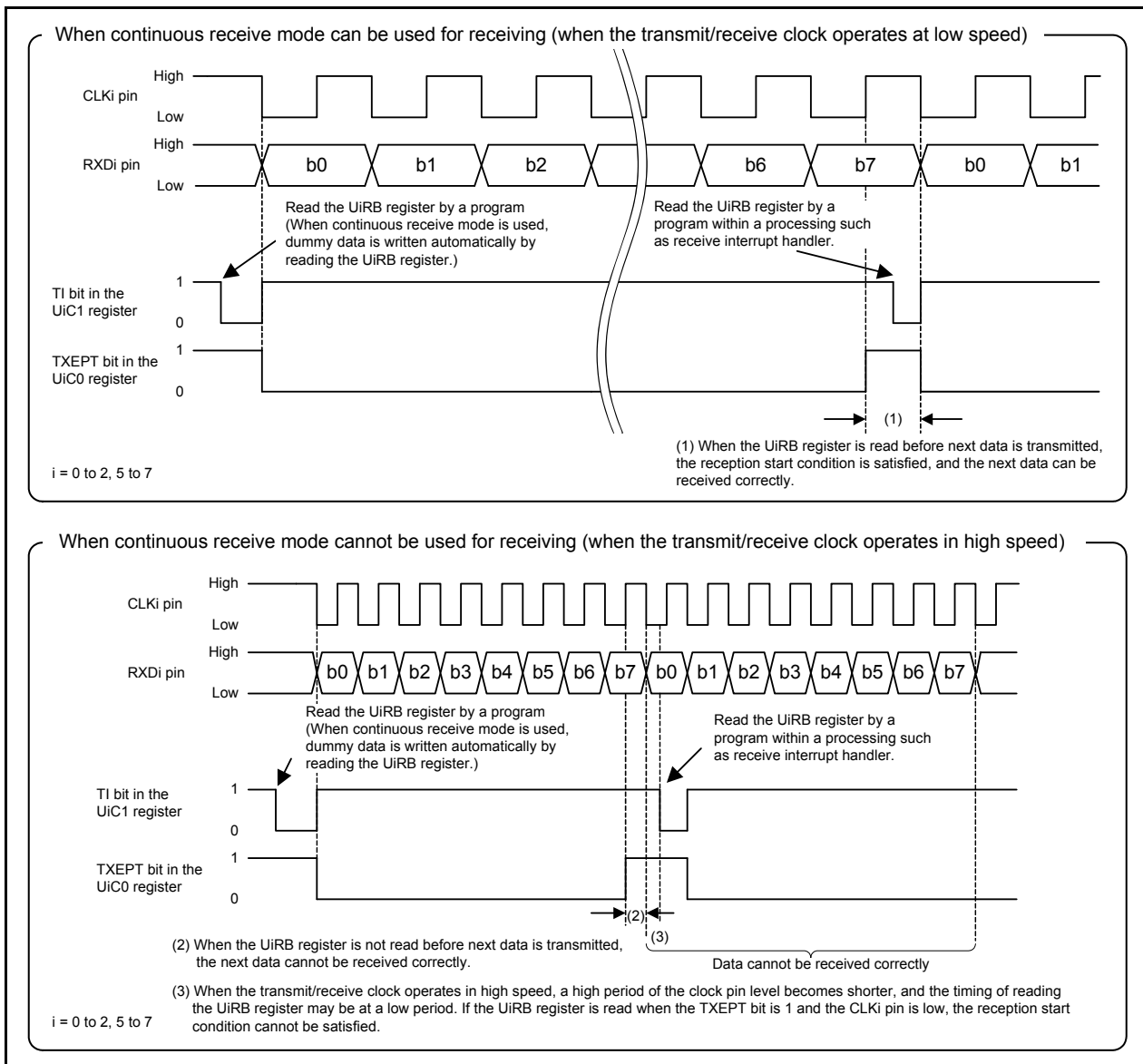| Peripheral Function	Application
Serial interface (UART0)	Receiving data
DMAC (DMA0)	Writing dummy data
DMAC (DMA1)	Reading received data

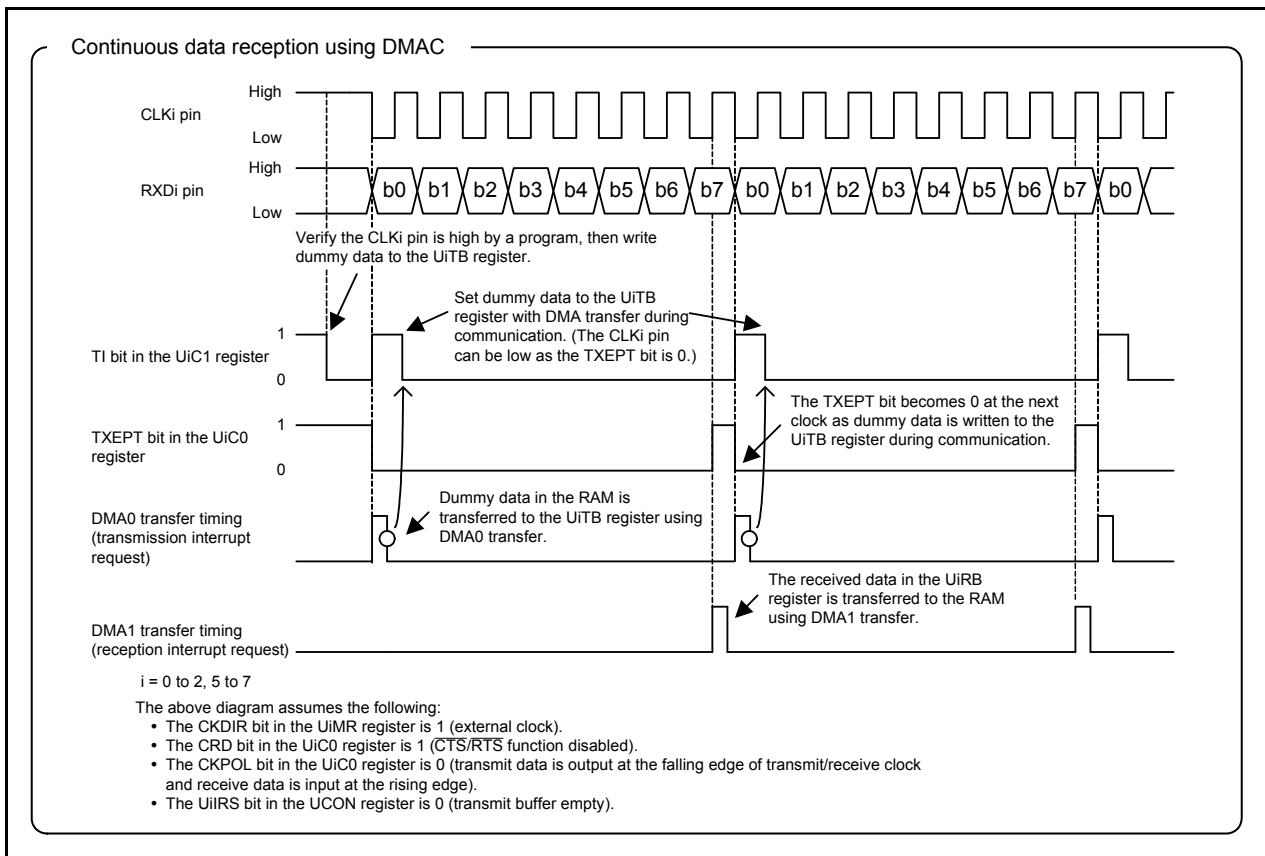**Figure 1.1   Timing Diagram of Continuous Receive Mode**

Figure 1.2   Timing Diagram of Continuous Data Reception with DMAC

1.1   Notes on Clock Synchronous Serial I/O Mode

This section describes notes on clock synchronous serial I/O mode for the M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups.

When starting transmission/reception while an external clock is selected, and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), the reception start condition must be met when the level of an external clock is the following:

- When the CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge), an external clock is high.
- When the CKPOL bit in the UiC0 register is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge), an external clock is low.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1   Operation Confirmation Conditions

Item	Contents
MCU used	M16C/65 Group
Operating frequencies	• XIN Clock: 8 MHz • CPU clock: 32 MHz (PLL clock: divided by 2, multiplied by 8)
Operating voltage	5 V (available between 3.3 to 5 V)
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09
C compiler	Renesas Electronics Corporation M16C Series/R8C Family C Compiler V.5.45 Release 01
	Compile options -c -finfo -dir "$(CONFIGDIR)" (The default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Software

The sample code uses a combination of UART0 clock synchronous I/O mode, DMAC0, and DMAC1 to receive a total of 256 bytes of data.

Table 3.1 to Table 3.3 list the settings for UART0, DMAC0, and DMAC1.

Table 3.1   UART0 Setting Conditions

Item	Setting
Operation mode	Clock synchronous serial I/O mode
Transmit/receive clock	External clock
CTS/RTS function	Disabled
CLK polarity selection	Transmit data is output at the falling edge of the transmit/receive clock and receive data is input at the rising edge.
Bit order	LSB first
Transmit interrupt source	Transmit buffer empty (TI = 1)
Continuous receive mode	Disabled

Table 3.2   DMAC0 Setting Conditions

Item	Setting
Transfer unit	8 bits
Transfer mode	Single transfer
Transfer source address (RAM address) direction	Fixed
Transfer destination address (the address of U0TB register) direction	Fixed
DMA request source	UART0 transmission
Number of transfers	255

Table 3.3   DMAC1 Setting Conditions

Item	Setting
Transfer unit	8 bits
Transfer mode	Single transfer
Transfer source address (the address of the U0RB register) direction	Fixed
Transfer destination address (RAM address) direction	Forward
DMA request source	UART0 reception
Number of transfers	256

3.1   Operation Overview

(1) Setting the reception start condition
Set the RE bit in the U0C1 register to 1 (reception enabled), and the TE bit to 1 (transmission enabled). Verify the CLK0 pin is high by a program, then write dummy data to the U0TB register.

(2) Starting DMA0 transfer
When the data in the U0TB register is transferred to the transmit register, the TI bit in the U0C1 register becomes 1 (no data present in U0TB register), and the TXEPT bit in the U0C0 register becomes 0 (data present in transmit register). Then the DMA0 transfer is started by a UART0 transmit interrupt request, and dummy data is transferred to the U0TB register from the RAM.

(3) Setting the reception start condition during transmitting (when TXEPT = 0)
When dummy data is written to the U0TB register by the DMA0 transfer, the TI bit becomes 0 (data present in UiTB register). (1.1 Notes on Clock Synchronous Serial I/O Mode does not apply to this case as the TXEPT bit is 0.)

(4) Starting DMA1 transfer
When the reception is completed, the RI bit in the U0C1 register becomes 1 (data present in U0RB register). Then the DMA1 transfer is started by the UART0 receive interrupt request, and the received data is transferred from the U0RB register to the RAM. Repeat steps (2) to (4) until a total of 256 bytes of data is received.

(5) When 256-byte data reception is completed
When the total of 256 bytes of data is received, the receive operation is not performed for the subsequent data.

Figure 3.1 shows the Timing Diagram.
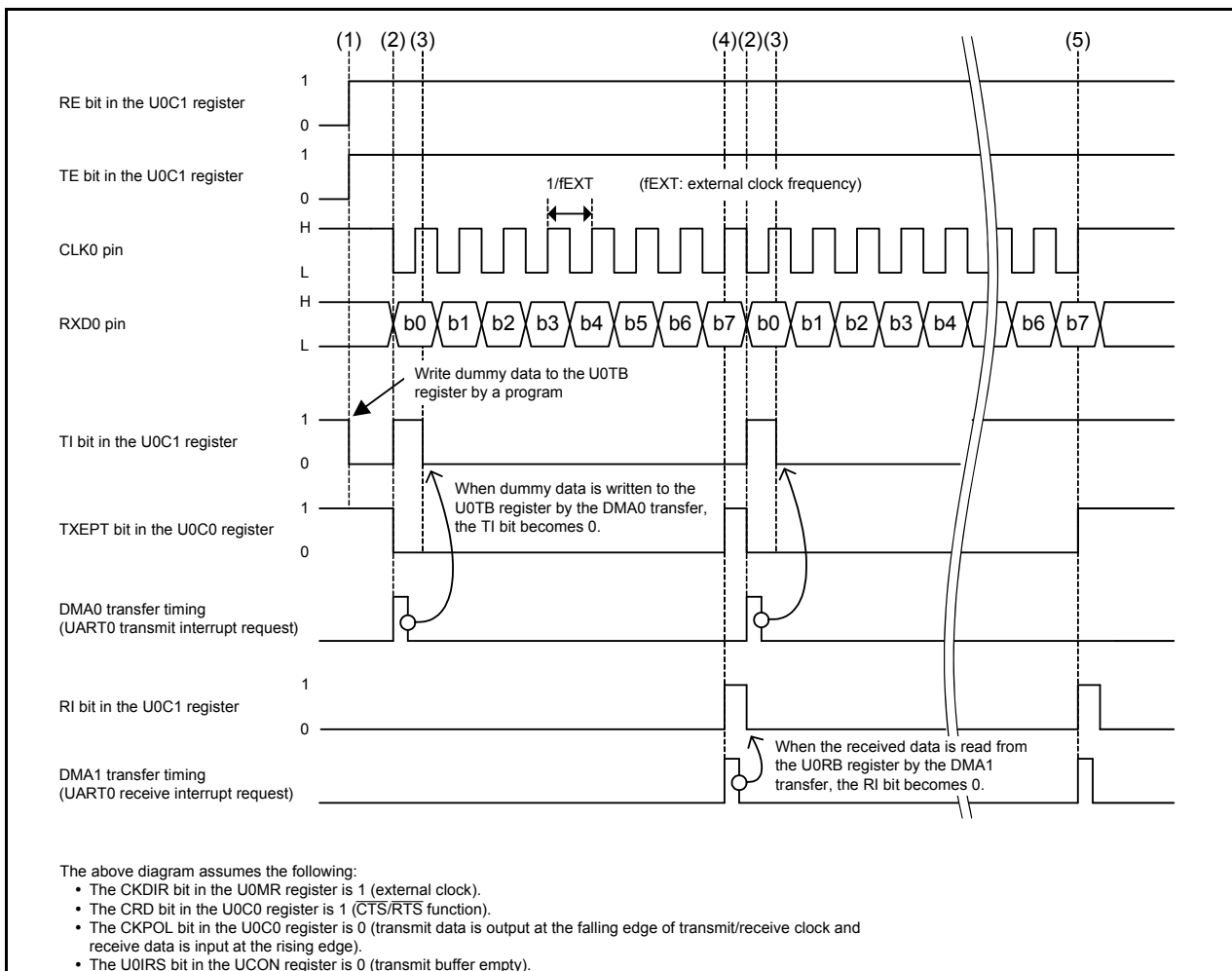
Figure 3.1   Timing Diagram

3.2 Required Memory Size

Table 3.4 lists the Required Memory Size.

Table 3.4 Required Memory Size

Memory Used	Size	Remarks
ROM	229 bytes	In the r01an0732_src module
RAM	257 bytes	In the r01an0732_src module
Maximum user stack usage	14 bytes	
Maximum interrupt stack usage	0 bytes	

The required memory size varies depending on the C compiler version and compile options.

3.3 Constant

Table 3.5 lists the Constant Used in the Sample Code.

Table 3.5 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
DUMMY_DATA	FFh	Dummy data

3.4 Variables

Table 3.6 lists the Global Variables.

Table 3.6 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	trn_data	Transmitted data	peripheral_init
unsigned char	rcv_data[256]	For received data storage	main, peripheral_init

3.5 Functions

Table 3.7 lists the Functions.

Table 3.7 Functions

Function Name	Outline
mcu_init	CPU initialization
peripheral_init	Peripheral function initialization

3.6 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	CPU initialization
Header	None
Declaration	void mcu_init(void)
Description	Set the PLL clock divided by 2, and multiplied by 8 as the CPU clock.
Argument	None
Returned value	None
Remark	

peripheral_init	
Outline	Peripheral function initialization
Header	None
Declaration	void peripheral_init(void)
Description	Initialize UART0, DMAC0, and DMAC1.
Argument	None
Returned value	None
Remark	

3.7 Flowcharts

3.7.1 Main Processing

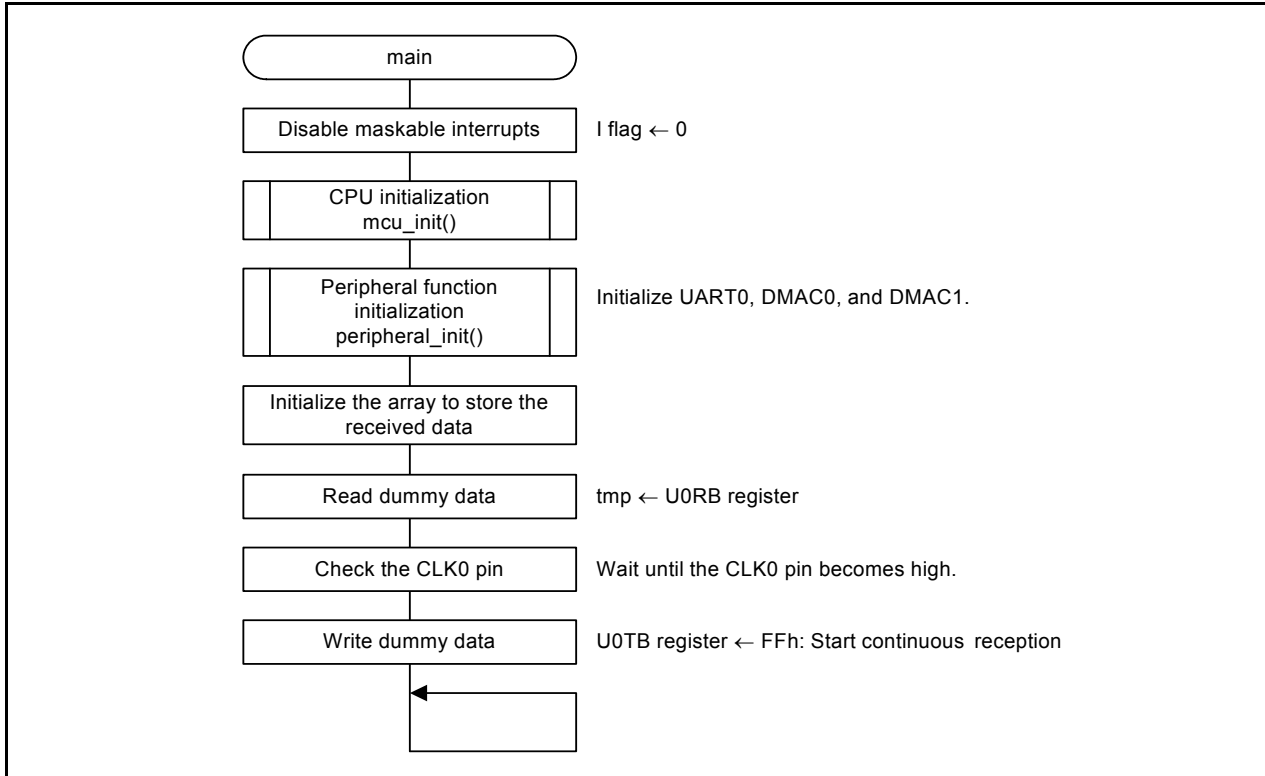Figure 3.2 shows the Main Processing.

Figure 3.2   Main Processing

3.7.2 Peripheral Function Initialization

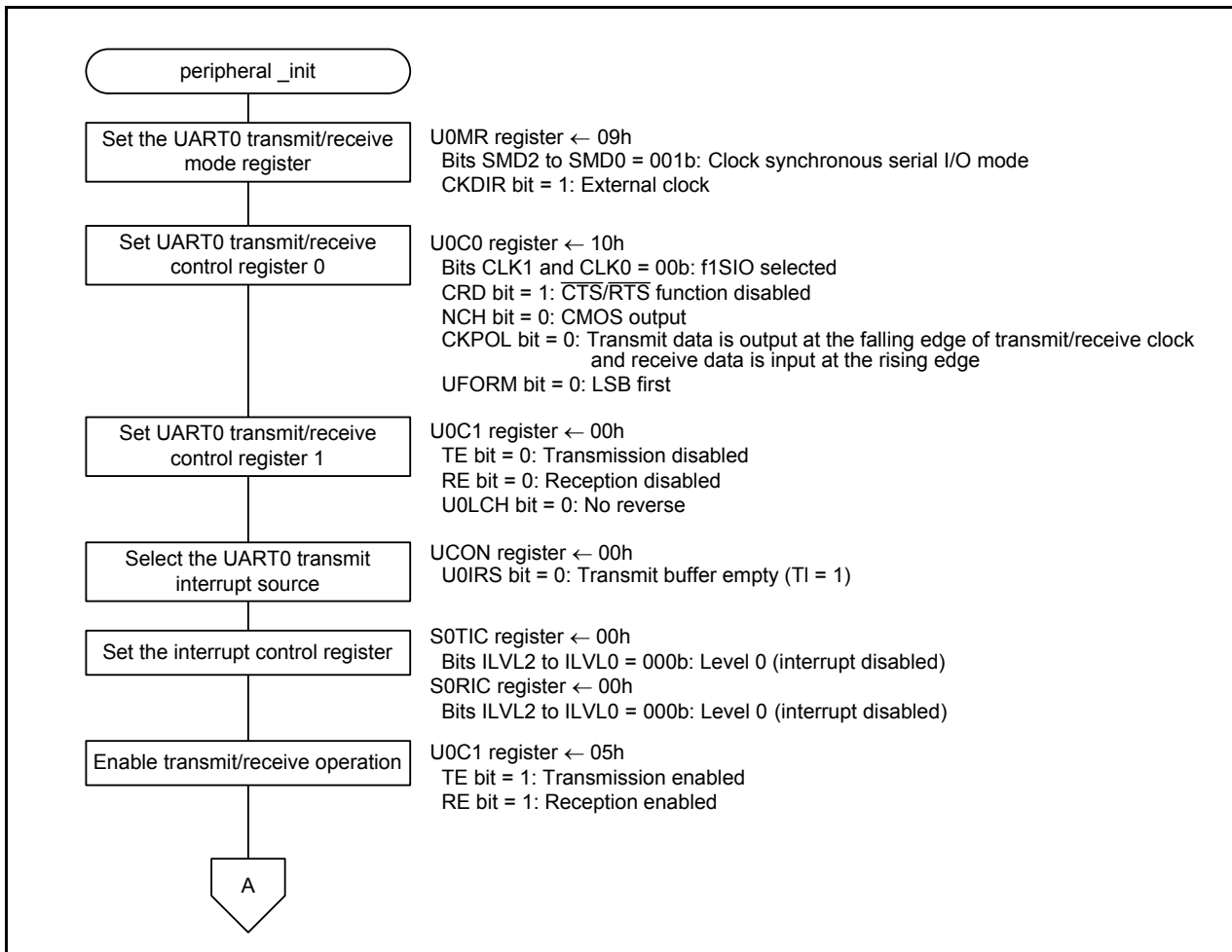Figure 3.3 and Figure 3.4 show Peripheral Function Initialization.

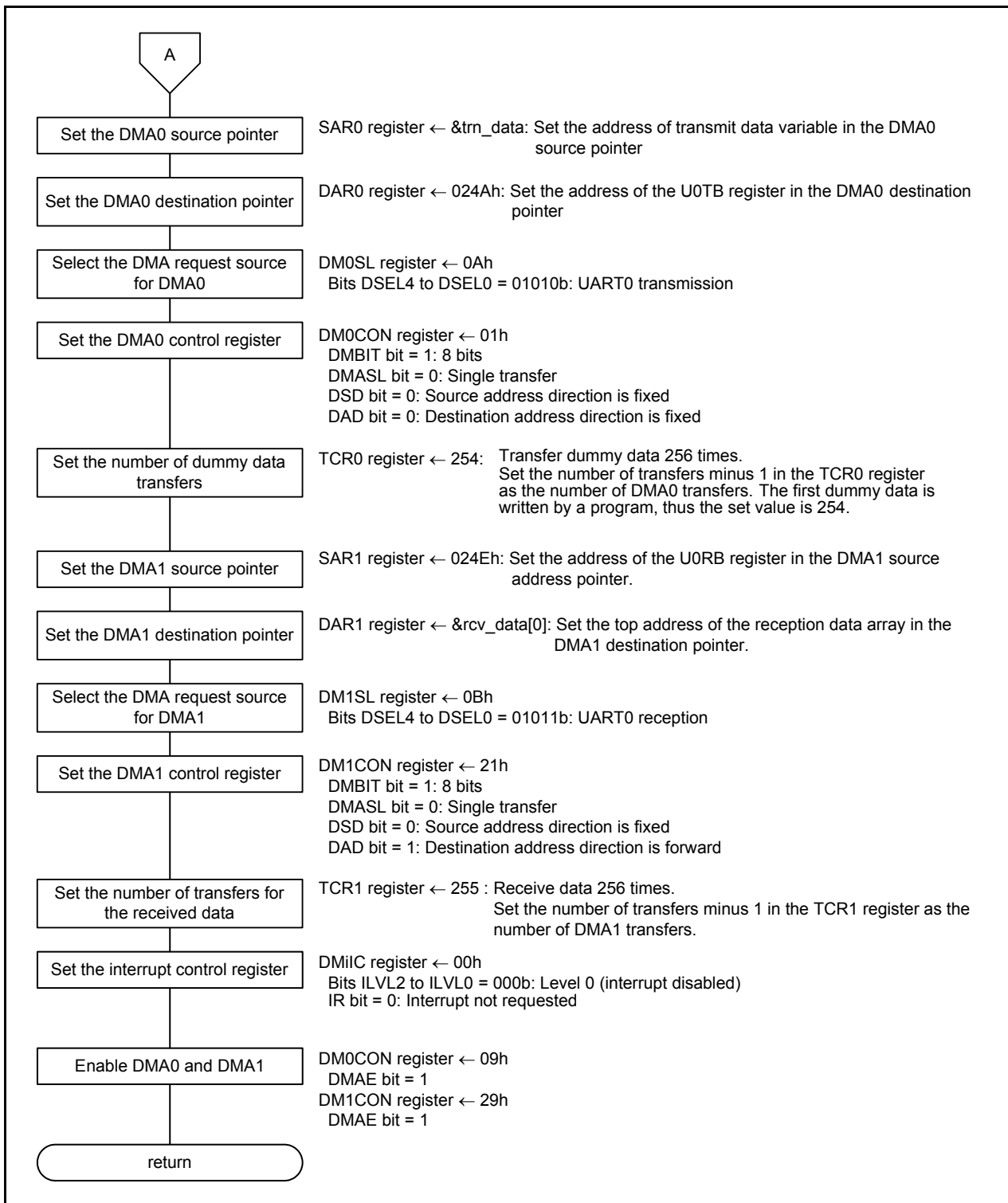**Figure 3.3   Peripheral Function Initialization (1/2)**

```
        ┌───┐
        │ A │
        └─┬─┘
          ▼
```

| Set the DMA0 source pointer | SAR0 register ← &trn_data: Set the address of transmit data variable in the DMA0 source pointer |

| Set the DMA0 destination pointer | DAR0 register ← 024Ah: Set the address of the U0TB register in the DMA0 destination pointer |

| Select the DMA request source for DMA0 | DM0SL register ← 0Ah
  Bits DSEL4 to DSEL0 = 01010b: UART0 transmission |

| Set the DMA0 control register | DM0CON register ← 01h
  DMBIT bit = 1: 8 bits
  DMASL bit = 0: Single transfer
  DSD bit = 0: Source address direction is fixed
  DAD bit = 0: Destination address direction is fixed |

| Set the number of dummy data transfers | TCR0 register ← 254: Transfer dummy data 256 times.
Set the number of transfers minus 1 in the TCR0 register as the number of DMA0 transfers. The first dummy data is written by a program, thus the set value is 254. |

| Set the DMA1 source pointer | SAR1 register ← 024Eh: Set the address of the U0RB register in the DMA1 source address pointer. |

| Set the DMA1 destination pointer | DAR1 register ← &rcv_data[0]: Set the top address of the reception data array in the DMA1 destination pointer. |

| Select the DMA request source for DMA1 | DM1SL register ← 0Bh
  Bits DSEL4 to DSEL0 = 01011b: UART0 reception |

| Set the DMA1 control register | DM1CON register ← 21h
  DMBIT bit = 1: 8 bits
  DMASL bit = 0: Single transfer
  DSD bit = 0: Source address direction is fixed
  DAD bit = 1: Destination address direction is forward |

| Set the number of transfers for the received data | TCR1 register ← 255 : Receive data 256 times.
  Set the number of transfers minus 1 in the TCR1 register as the number of DMA1 transfers. |

| Set the interrupt control register | DMiIC register ← 00h
  Bits ILVL2 to ILVL0 = 000b: Level 0 (interrupt disabled)
  IR bit = 0: Interrupt not requested |

| Enable DMA0 and DMA1 | DM0CON register ← 09h
  DMAE bit = 1
DM1CON register ← 29h
  DMAE bit = 1 |

```
   (  return  )
```

Figure 3.4   Peripheral Function Initialization (2/2)

4. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

5. Reference Documents

M16C/63 Group User's Manual: Hardware Rev. 2.00
M16C/64A Group User's Manual: Hardware Rev. 2.00
M16C/64C Group User's Manual: Hardware Rev. 1.00
M16C/65 Group User's Manual: Hardware Rev. 2.00
M16C/65C Group User's Manual: Hardware Rev. 1.00
M16C/6C Group User's Manual: Hardware Rev. 2.00
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev. 1.10
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev. 1.10
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev. 1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series/R8C Series C Compiler Package V.5.45
C Compiler User's Manual Rev. 2.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, and 57 Groups Serial Interface: Using High Speed Communication when Performing Clock Synchronous Slave Reception with DMAC

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 30, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

    Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

    — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

    The state of the product is undefined at the moment when power is supplied.

    — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

    Access to reserved addresses is prohibited.

    — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

    After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

    — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

    Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

    — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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