RENESAS

M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups
Operation of Serial I/O (Reception in UART Mode)

1. Abstract

In receiving data in UART mode, choose functions from those listed in Table 3.1. Operations of the marked items are described below. The examples are explained below using the M16C/65 Group.

2. Introduction

This application note is applied to the following MCUs:

MCU(s): M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen functions

Table 3.1   Chosen Functions

Item	Set-up		Item	Set-up	
Clock prior to division select	✓	f1	Data logic select function	✓	No reverse
		fOCO-F			Reverse
Peripheral clock	✓	f1SIO	TXD, RXD I/O polarity reverse bit	✓	No reverse
		f2SIO			Reverse
Transfer clock source	✓	Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	Separate $\overline{CTS}/\overline{RTS}$ pins [1]	✓	Shared pin
		External clock (CLKi pin)			Separated
$\overline{RTS}$ function	✓	$\overline{RTS}$ function enabled			
		$\overline{RTS}$ function disable			

Note:
1. This function separates $\overline{CTS0}/\overline{RTS0}$, outputs $\overline{RTS0}$ from the P6_0 pin, and inputs $\overline{CTS0}$ from the P6_4 pin. When this function is selected, UART1 $\overline{CTS}/\overline{RTS}$ function can not be utilized. Set the UART1 $\overline{CTS}/\overline{RTS}$ disable bit to "1".

4. Operation

(1) Setting the receive enable bit to "1" readies data-receivable status. At this time, output from the $\overline{RTSi}$ pin goes to "L" level to inform the transmission side that the receivable status is ready.

(2) When the first bit (the start bit) of reception data is received from the RxDi pin, output from the $\overline{RTS}$ goes to "H" level. Then, data is received, bit by bit, in sequence: LSB, ···, MSB, and stop bit(s).

(3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. At this time, the receive complete flag goes to "1" to indicate that the reception is completed, the UARTi receive interrupt request bit goes to "1".

(4) When the lower-order byte of the UARTi buffer register is read, the receive complete flag goes to "0", and output from the $\overline{RTS}$ pin goes to "L" level.
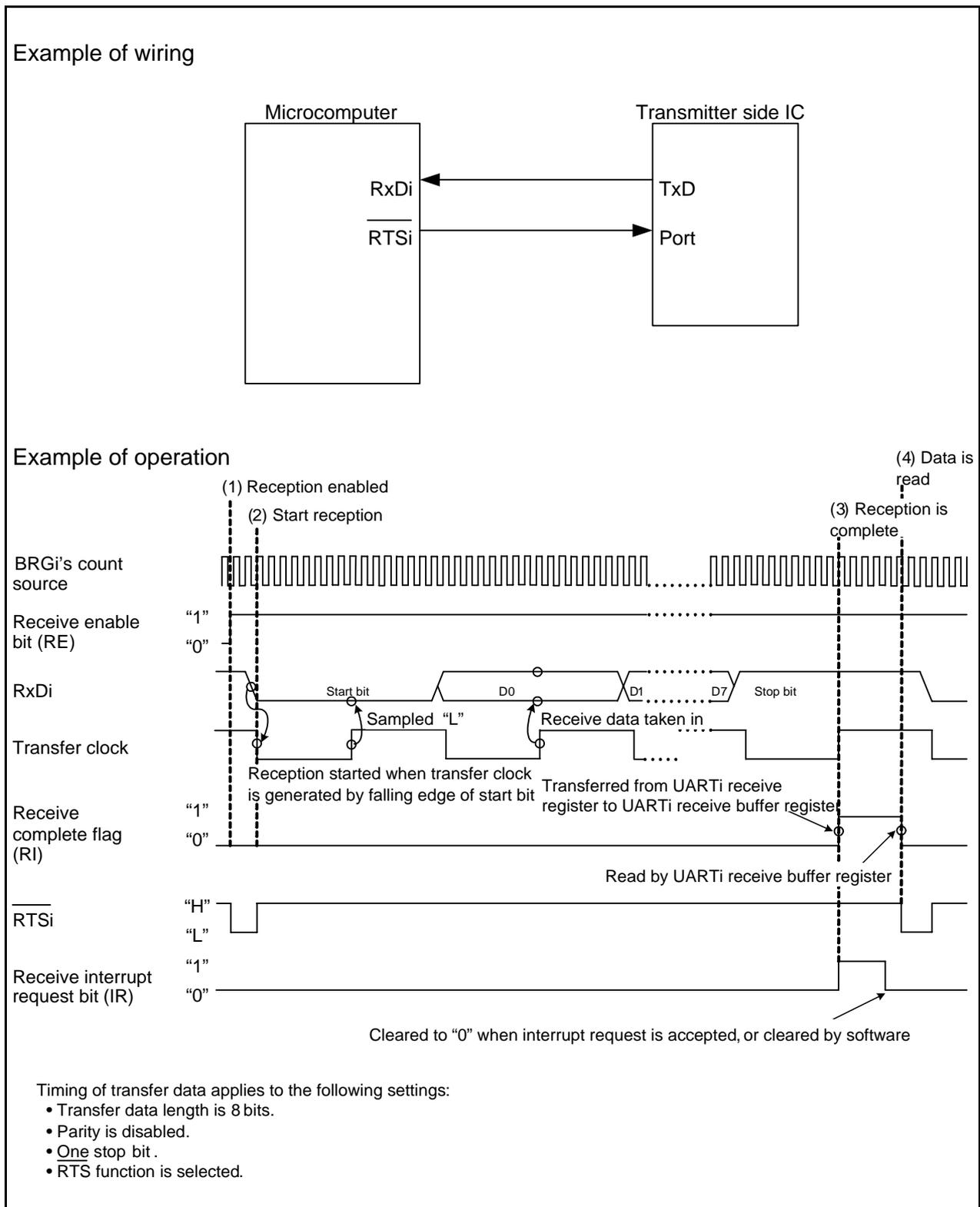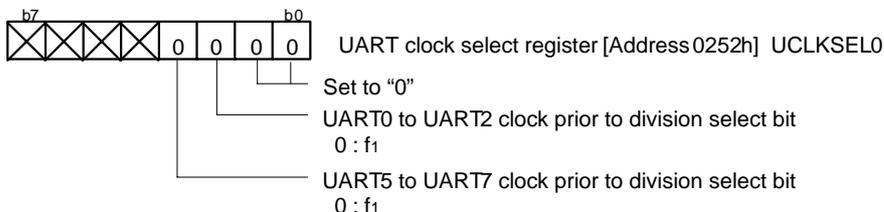
Figure 4.1 shows the operation timing.

Figure 4.1   Operation Timing of Reception in UART Mode
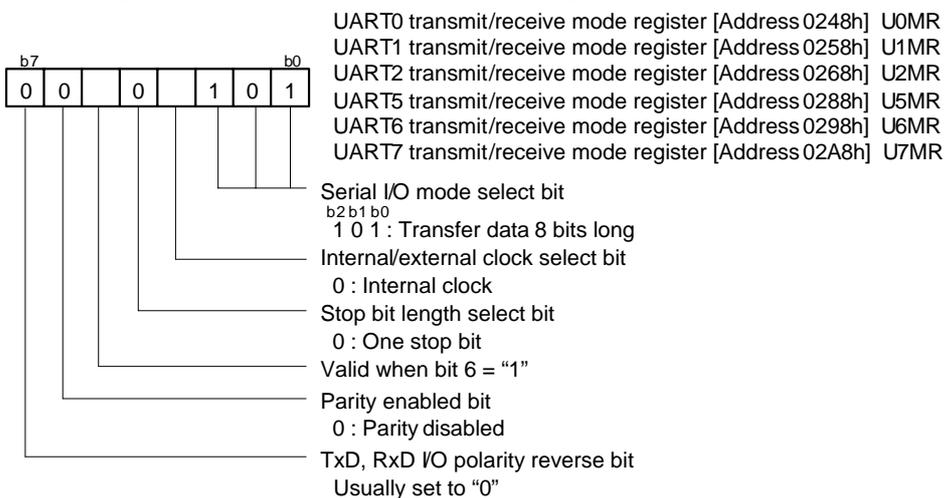
5. Set-up Procedure

Setting UART clock select register

(Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.)
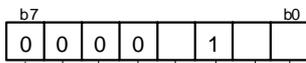
```
b7                    b0
☒☒☒☒ 0 0 0 0     UART clock select register [Address 0252h]  UCLKSEL0
```

Set to "0"

UART0 to UART2 clock prior to division select bit
  0 : f_1

UART5 to UART7 clock prior to division select bit
  0 : f_1

Note: Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.

Setting UARTi transmit/receive mode register (i = 0 to 2, 5 to 7)

UART0 transmit/receive mode register [Address 0248h] U0MR
UART1 transmit/receive mode register [Address 0258h] U1MR
UART2 transmit/receive mode register [Address 0268h] U2MR
UART5 transmit/receive mode register [Address 0288h] U5MR
UART6 transmit/receive mode register [Address 0298h] U6MR
UART7 transmit/receive mode register [Address 02A8h] U7MR

```
b7                    b0
0 0  0  1 0 1
```

Serial I/O mode select bit
  b2 b1 b0
  1 0 1 : Transfer data 8 bits long

Internal/external clock select bit
  0 : Internal clock

Stop bit length select bit
  0 : One stop bit

Valid when bit 6 = "1"

Parity enabled bit
  0 : Parity disabled

TxD, RxD I/O polarity reverse bit
  Usually set to "0"

Setting UARTi transmit/receive control register (i = 0 to 2, 5 to 7)

UART0 transmit/ receive control register [Address 024Ch] U0C0
UART1 transmit/ receive control register [Address 025Ch] U1C0
UART2 transmit/ receive control register [Address 026Ch] U2C0
UART5 transmit/ receive control register [Address 028Ch] U5C0
UART6 transmit/ receive control register [Address 029Ch] U6C0
UART7 transmit/ receive control register [Address 02ACh] U7C0

b7 | | | | | | | b0
0 | 0 | 0 | 0 | | 1 | |

UiBRG count source select bit
b1 b0
0 0 : f_{1SIO} or f_{2SIO} is selected (Note1)
0 1 : f_{8SIO} is selected
1 0 : f_{32SIO} is selected
1 1 : Do not set to this value

CTS/RTS function select bit (Valid when bit 4 = "0")
1 : RTS function is selected (Note2)

Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (transmission completed)

CTS/RTS disable bit
0 : CTS/RTS function enabled

Data output select bit
0 : Pins TXDi/SDAi and SCLi are CMOS output
1 : Pins TXDi/SDAi and SCLi are N-channel open-drain output
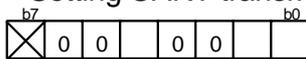
Must always be "0" in UART mode

Transfer format select bit
0 : LSB first

Note 1: When the PCLK1 bit in the PCLKR register is "1", the selected clock source is f_{1SIO}. When the PCLK1 bit is "0", the selected clock source is f_{2SIO}.
Note 2: Set the corresponding port direction register to "1" (output mode).

Setting UART transmit/receive control register 2

b7 | | | | | | | b0
☒ | 0 | 0 | | 0 | 0 | |

UART transmit/receive control register 2 [Address 0250h] UCON

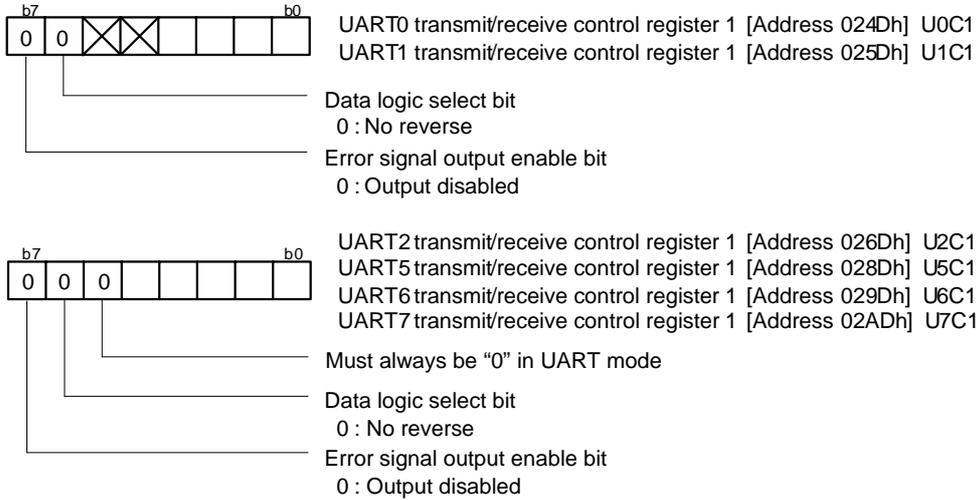Must always be "0" in UART mode

Must always be "0" in UART mode

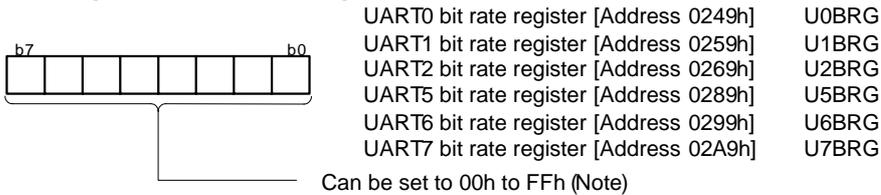Invalid in UART mode

Must always be "0" in UART mode

Separate UART0 CTS/RTS bit
0 : CTS/RTS shared pin

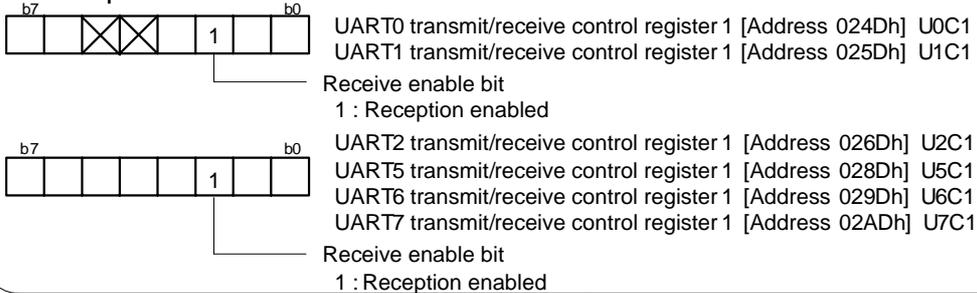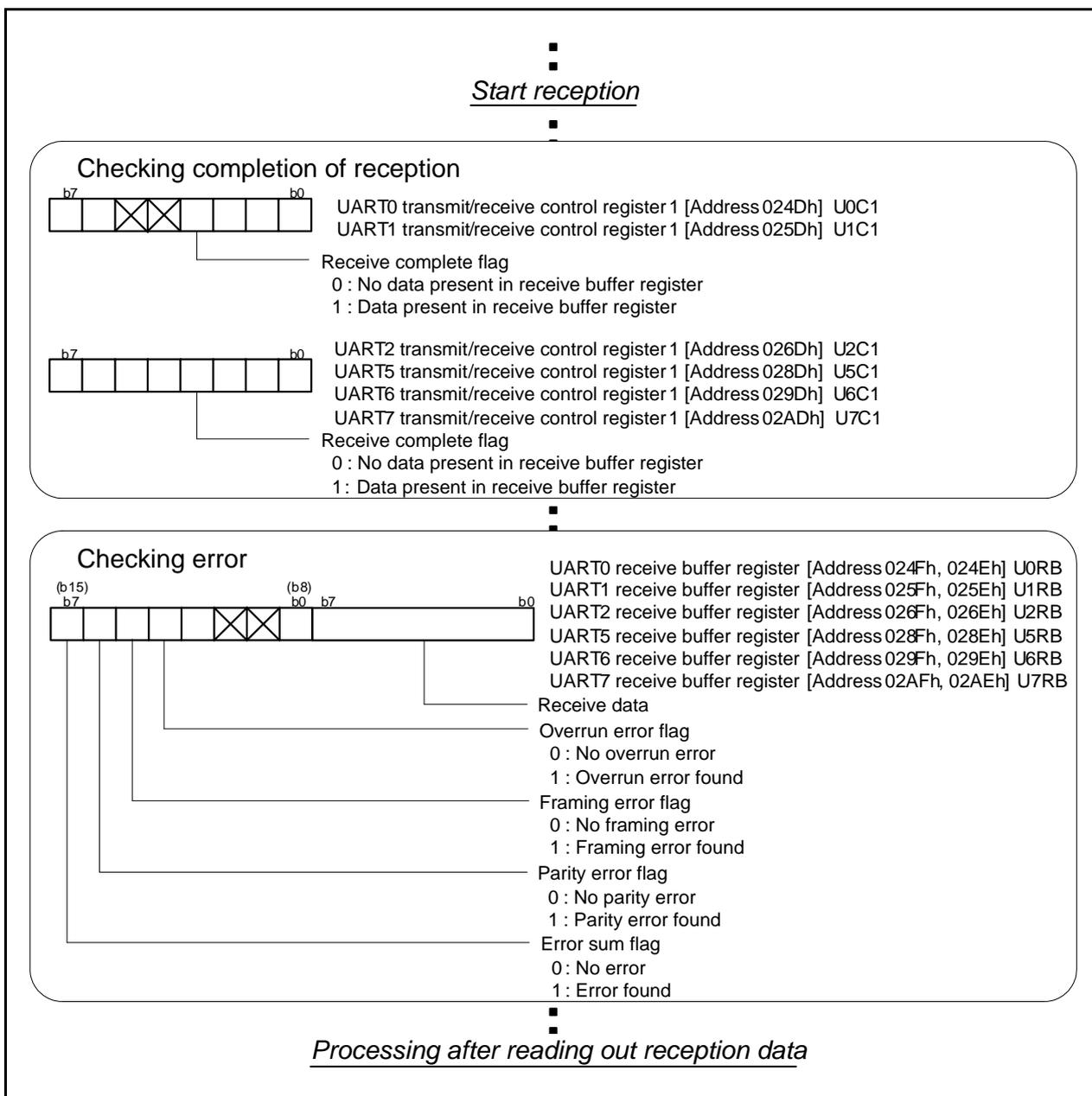Setting UARTi transmit/receive control register 1 (i = 0 to 2, 5 to 7)

UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Data logic select bit
 0 : No reverse

Error signal output enable bit
 0 : Output disabled

UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Must always be "0" in UART mode

Data logic select bit
 0 : No reverse

Error signal output enable bit
 0 : Output disabled

Setting UARTi bit rate register (i = 0 to 2, 5 to 7)

UART0 bit rate register [Address 0249h]   U0BRG
UART1 bit rate register [Address 0259h]   U1BRG
UART2 bit rate register [Address 0269h]   U2BRG
UART5 bit rate register [Address 0289h]   U5BRG
UART6 bit rate register [Address 0299h]   U6BRG
UART7 bit rate register [Address 02A9h]   U7BRG

Can be set to 00h to FFh (Note)

Note : Write to the UiBRG register while serial interface is neither transmitting nor receiving. Use MOV instruction to write to the UiBRG register Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.

Reception enabled

UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Receive enable bit
 1 : Reception enabled

UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Receive enable bit
 1 : Reception enabled

Start reception

Checking completion of reception

b7 ⬛⬛ b0

UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Receive complete flag
  0 : No data present in receive buffer register
  1 : Data present in receive buffer register

b7 b0

UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Receive complete flag
  0 : No data present in receive buffer register
  1 : Data present in receive buffer register

Checking error

(b15)
b7   (b8)
b0 b7   b0

UART0 receive buffer register [Address 024Fh, 024Eh] U0RB
UART1 receive buffer register [Address 025Fh, 025Eh] U1RB
UART2 receive buffer register [Address 026Fh, 026Eh] U2RB
UART5 receive buffer register [Address 028Fh, 028Eh] U5RB
UART6 receive buffer register [Address 029Fh, 029Eh] U6RB
UART7 receive buffer register [Address 02AFh, 02AEh] U7RB

Receive data

Overrun error flag
  0 : No overrun error
  1 : Overrun error found

Framing error flag
  0 : No framing error
  1 : Framing error found

Parity error flag
  0 : No parity error
  1 : Parity error found

Error sum flag
  0 : No error
  1 : Error found

Processing after reading out reception data

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.2.00
M16C/64A Group User's Manual: Hardware Rev.2.00
M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65 Group User's Manual: Hardware Rev.2.00
M16C/65C Group User's Manual: Hardware Rev.1.00
M16C/6C Group User's Manual: Hardware Rev.2.00
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev.1.10
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev.1.00
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

Renesas Electronics website
http://www.renesas.com/

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Revision History	M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups Operation of Serial I/O (Reception in UART Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 30, 2009	—	First edition issued
1.01	Apr. 28, 2011	—	Add: M16C/63, M16C/64A, M16C/64C, M16C/65C, M16C/6C, M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/5M, and M16C/57

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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