M16C/63, 64A, 64C, 65, 65C, and 6C Groups

Flash Memory Security System

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Abstract

This document describes the flash memory security system for the M16C/63, 64A, 64C, 65, 65C, and 6C Groups. This document describes setting methods to restrict accesses for program, read, and erase operations in standard serial I/O mode and parallel I/O mode of flash memory rewrite mode.
In this document, the internal flash memory is referred to simply as flash memory.

Products

M16C/63, 64A, 64C, 65, 65C, and 6C Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Access to the flash memory can be restricted according to use. Table 1.1 lists Adding Security During Software Development and Table 1.2 lists Adding Security During Mass Production.
Refer to 3.4 “Security when Using User Boot Mode” for details on using the user boot.

Table 1.1 Adding Security During Software Development (1, 2)

Security Level	Purpose	Serial Programmer		Parallel Programmer		Reference
		Read	Program	Read	Program	
None	Development has priority. Anyone can access the flash memory.	✓	✓	✓	✓	3.1.1 “No Security”
Low	Simple security is required. If the ID code is lost, all data in the flash memory can be erased with a serial programmer.	◆	◆	✓	✓	3.1.2 “Security Level 1”

Notes:
1. ✓: Available, ◆: Available when the ID code is ready.
2. The user boot can be started even if the ID code is “Protect”.

Table 1.2 Adding Security During Mass Production (1, 2)

Security Level	Purpose	Serial Programmer		Parallel Programmer		Reference
		Read	Program	Read	Program	
Low ↕ High	Only those who know the ID can access the flash memory.	◆	◆	×	×	3.1.3 “Security Level 2”
	No one can read the flash memory. The flash memory can be updated.	×	◆	×	×	3.1.4 “Security Level 3”
	All accesses to the flash memory by programmers are disabled.	×	×	×	×	3.1.5 “Security Level 4”

Notes:
1. ◆: Available when the ID code is ready., ×: Not available
2. The user boot can be started even if the ID code is “Protect”.

2. Reference Application Notes

Application notes associated with this application note are listed below. Refer to these application notes for additional information.

- M16C/63 Group High-performance Embedded Workshop Start-up Program in C (R01AN0042EJ)
- M16C/64A Group High-performance Embedded Workshop Start-up Program in C (R01AN0044EJ)
- M16C/65 Group High-performance Embedded Workshop Start-up Program in C (R01AN0045EJ)
- M16C/65C Group High-performance Embedded Workshop Start-up Program in C (R01AN0046EJ)
- M16C/6C Group High-performance Embedded Workshop Start-up Program in C (R01AN0047EJ)

3. Peripheral Functions

3.1 Flash Memory Security

This section describes the settings for each security level, and their advantages and disadvantages. Refer to 3.2 “ID Code Setting” and 3.3 “ROM Code Protect Setting” for details on setting the ID code and ROM code protect.

3.1.1 No Security

No restrictions are placed on accessing the flash memory with a serial or parallel programmers. Table 3.1 lists the Settings and Table 3.2 lists the Advantage and Disadvantage.

Table 3.1 Settings

ID Code	ROM Code Protect
FFFFFFFFFFFFFFh (default value)	No setting required

Table 3.2 Advantage and Disadvantage

Advantage	Disadvantage
The ID code does not need to be managed.	Anyone can access to the flash memory with a serial or a parallel programmer. Therefore the flash memory may be read, programmed, or erased anytime.

3.1.2 Security Level 1

Access to the flash memory with a serial programmer is restricted to those who know the ID code. Access to the flash memory with a parallel programmer is not restricted.
Table 3.3 lists the Settings and Table 3.4 lists the Advantages and Disadvantages.

Table 3.3 Settings

ID Code	ROM Code Protect
Arbitrary ID (except for “Protect” and “ALeRASE”)	No setting required

Table 3.4 Advantages and Disadvantages

Advantage	Disadvantage
• Only those who know the ID code can access the flash memory. • If the ID code is lost, all data in the flash memory can be erased using the forced erase function including the ID code area. • The flash memory can be accessed with a parallel programmer.	• After data in the flash memory is erased with the forced erase function, the flash memory may be programmed. • Anyone can access the flash memory with a parallel programmer. Therefore the flash memory may be read, programmed, or erased anytime.

3.1.3 Security Level 2

Access to the flash memory with a serial programmer is restricted to those who know the ID code. Access to the flash memory with a parallel programmer is disabled.
Table 3.5 lists the Settings and Table 3.6 lists the Advantages and Disadvantage.

Table 3.5 Settings

ID Code	ROM Code Protect
Arbitrary ID (except for “Protect” and “ALeRASE”)	Setting required

Table 3.6 Advantages and Disadvantage

Advantage	Disadvantage
• Access to the flash memory with a serial programmer is not permitted without the ID code. • The forced erase function is disabled.	If the ID code is lost, access to the flash memory is not permitted.

3.1.4 Security Level 3

When the ID code for accessing the flash memory with a serial programmer is validated, all data in the flash memory is erased and read access is disabled. Access with a parallel programer is also disabled.
Table 3.7 lists the Settings and Table 3.8 lists the Advantages and Disadvantages.

Table 3.7 Settings

ID Code	ROM Code Protect
“ALeRASE”	Setting required

Table 3.8 Advantages and Disadvantages

Advantage	Disadvantage
• When accessing the flash memory with a serial programmer, all data in the flash memory is erased. As a result, the flash memory cannot be read. • Management of the ID code is not required as it is predefined.	• Even the developer cannot read the flash memory as all data in the flash memory is erased when accessing it with a serial programmer. • The flash memory may be programmed after it is erased with the forced erase function.

3.1.5 Security Level 4

Access to the flash memory with serial and parallel programmers is disabled.
Table 3.9 lists the Settings and Table 3.10 lists the Advantages and Disadvantage.

Table 3.9 Settings

ID Code	ROM Code Protect
“Protect”	Setting required

Table 3.10 Advantages and Disadvantage

Advantage	Disadvantage
• Accessing the flash memory with a serial or a parallel programmer is disabled. As a result, the flash memory cannot be read, programmed, or erased. • The forced erase function is disabled.	The flash memory cannot be programmed at all.

3.2 ID Code Setting

The ID code is 7-byte data stored in 1-byte units, in the addresses, in the following order: 0FFFDFh, 0FFFE3h, 0FFFEBh, 0FFFEFh, 0FFFF3h, 0FFFF7h, and 0FFFFBh (ID code storage address). The ID code can be set by writing the program with the ID code setting in these addresses. Set arbitrary values in the ID code storage address. Select the C source startup Application in the High-performance Embedded Workshop (HEW), and create a new project workspace to generate a fvector.c file. fvector.c has setting codes for the ID code.

Figure 3.1 shows the Setting Code for the ID Code Created in fvector.c.

fvector.c uses the extended function directive command “.id”. The 7-byte ID code set in the ID code storage address can be described using the extended function directive command “.id”.

“FFFFFFFFFFFFFFh” is set as the default ID code value. Change the default value to change the ID code setting.

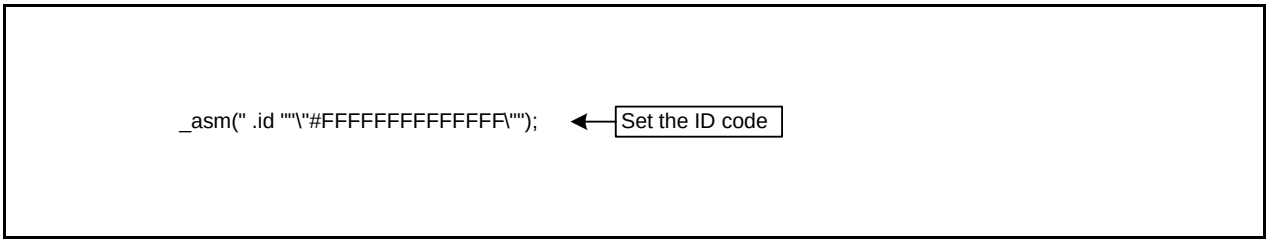

Figure 3.1 Setting Code for the ID Code Created in fvector.c

3.3 ROM Code Protect Setting

The ROM code protect can be set with bits ROMCP1 and ROMCR in the optional function select 1 address (OFS1). To enable the ROM code protect, set the ROMCP1 bit to 0 and the ROMCR bit to 1 in the OFS1 address. The OFS1 address is not a special function register (SFR), thus it cannot be rewritten by a program. Write appropriate values to the OFS1 address when writing a program to the flash memory. Select the C source startup Application in the HEW, and create a new project workspace to generate a fvector.c file. fvector.c has setting codes for the OFS1 address.

Figure 3.2 shows the Setting Code for the OFS1 Address Created in fvector.c.

fvector.c uses the extended function directive command “.ofsreg”. 1-byte code set in the OFS1 address can be described using the extended function directive command “.ofsreg”.

“FFh” is set as the default value. Change the default value to enable or disable the ROM code protect.

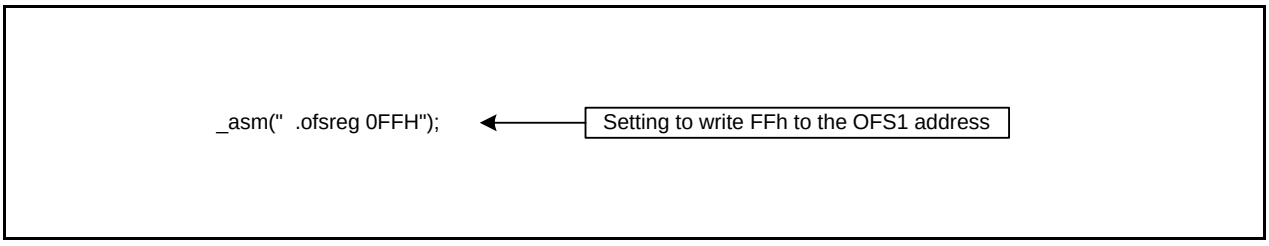

Figure 3.2 Setting Code for the OFS1 Address Created in fvector.c

3.4 Security when Using User Boot Mode

When using user boot mode, the ID code is not determined as shown in Figure 3.3 “Mode Determination”. Thus the security setting with the ID code or the ROM code protect is not valid, and the security described in 1. “Specifications” is not available, either.

Set security for user boot mode using the user boot program.

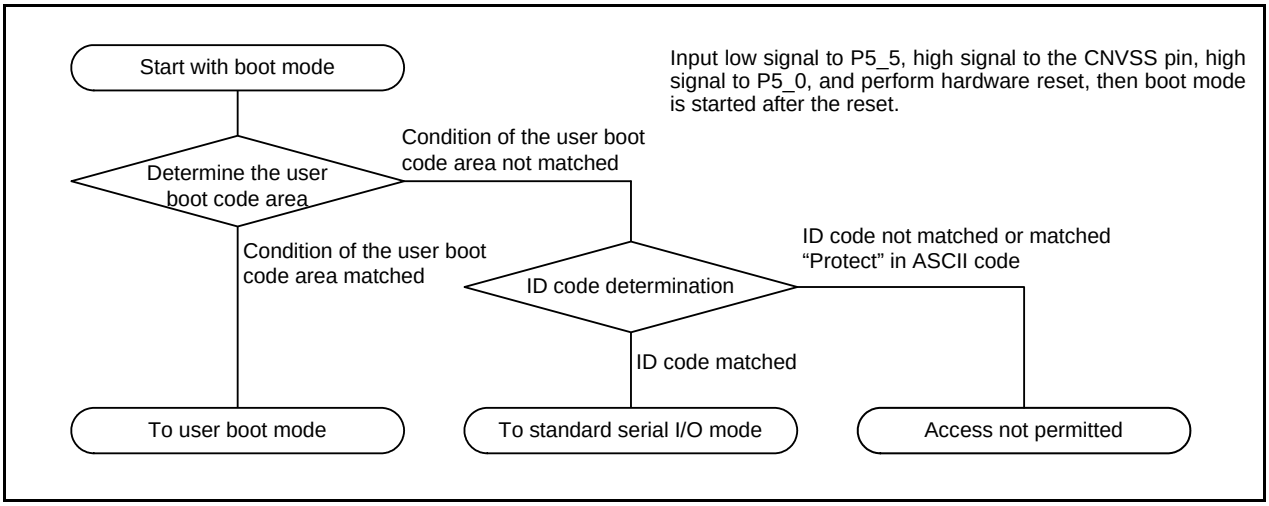

Figure 3.3 Mode Determination

4. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.2.00
M16C/64A Group User's Manual: Hardware Rev.2.00
M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65 Group User's Manual: Hardware Rev.2.00
M16C/65C Group User's Manual: Hardware Rev.1.00
M16C/6C Group User's Manual: Hardware Rev.2.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	M16C/63, 64A, 64C, 65, 65C, and 6C Groups Flash Memory Security System

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 31, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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