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April 1st, 2010
Renesas Electronics Corporation

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H8SX Family

Little–Big Endian Conversion by Bus Controller

Introduction

Little endian data is converted into big endian data using the bus controller.

Target Device

H8SX/1653

Contents

1. Specifications

- Figure 1 shows a block diagram of little–big endian conversion.
- Little endian data is converted into big endian data using the bus controller.
- Area 3 (SRAM) is set up as a little endian area.

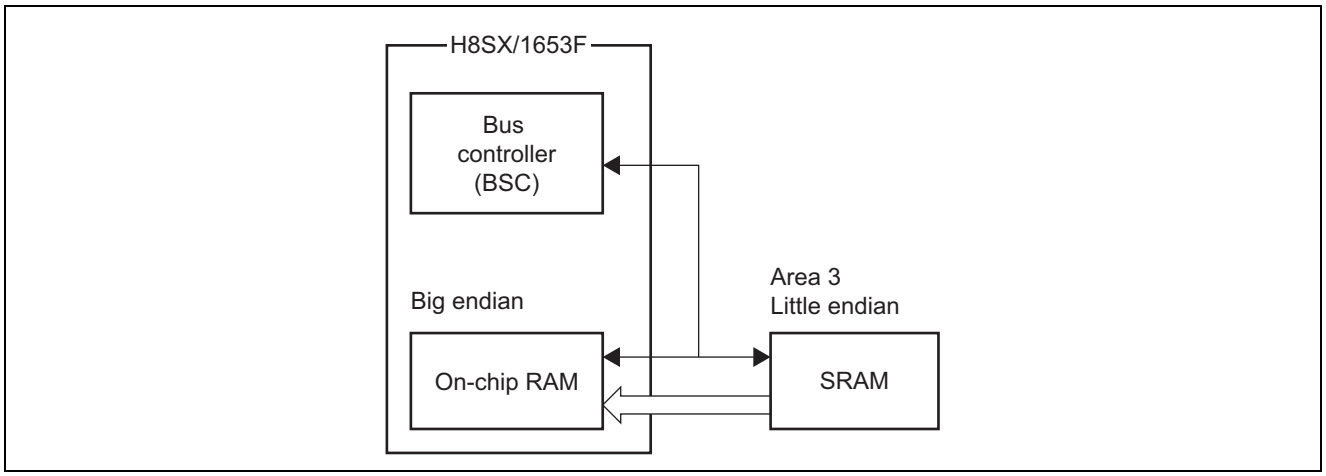


Figure 1 Little–Big Endian Conversion

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 16 MHz System clock (Iϕ): 32 MHz Peripheral module clock (Pϕ): 32 MHz External bus clock (Bϕ): 32 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'C00000	BCS3	Little endian area
H'FF2000	B	Non-initialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of the bus controller. The register for endian conversion in the bus controller is described below.

- Endian control register (ENDIANCR)
  Selects the endian format for each area of the external address space. In this sample task, the little endian data in area 3 is converted into big endian data.

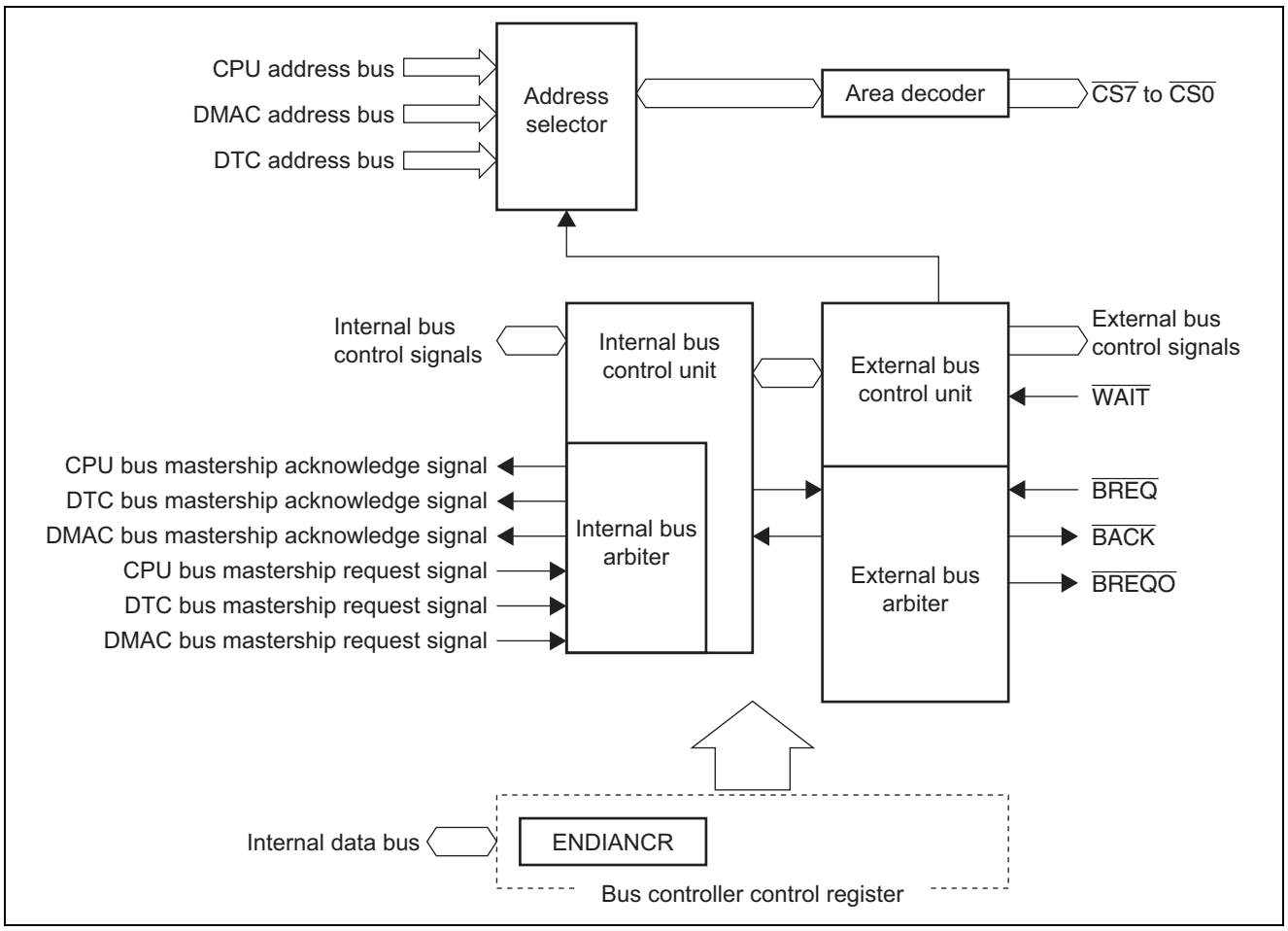


Figure 2 Block Diagram of Bus Controller

4. Description of Operation

4.1 Endian and Data Alignment

Data sizes for the CPU and other internal bus masters are byte, word, and longword. The bus controller has a data alignment function, and controls whether the upper-byte data bus (D15 to D8) or lower-byte data bus (D7 to D0) is used according to the bus specifications for the area being accessed (8-bit access space or 16-bit access space), the data size, and endian format when accessing an external address space.

(1) **8-Bit Access Space**

With the 8-bit access space, the lowest-byte data bus (D7 to D0) is always used for access. The amount of data that can be accessed at a time is one byte: a word access is performed as two byte accesses, and a longword access as four byte accesses.

Figures 3 and 4 illustrate the data alignment control for the 8-bit access space. Figure 3 shows the data alignment when big endian is specified. Figure 4 shows the data alignment when little endian is specified.

Access Size	Access Address	Access Count	Bus Cycle	Data Size	Data Bus D15 D8 D7 D0
Byte	n	1	1st	Byte	7 0
Word	n	2	1st	Word	15 8
			2nd	Byte	7 0
Longword	n	4	1st	Word	31 24
			2nd	Word	23 16
			3rd	Word	15 8
			4th	Byte	7 0

Figure 3 Access Sizes and Data Alignment Control for 8-Bit Access Space (Big Endian)

Access Size	Access Address	Access Count	Bus Cycle	Data Size	Data Bus D15 D8 D7 D0
Byte	n	1	1st	Byte	7 0
Word	n	2	1st	Byte	7 0
			2nd	Byte	15 8
Longword	n	4	1st	Byte	7 0
			2nd	Byte	15 8
			3rd	Byte	23 16
			4th	Byte	31 24

Figure 4 Access Sizes and Data Alignment Control for 8-Bit Access Space (Little Endian)

(2) **16-Bit Access Space**

With the 16-bit access space, the upper-byte data bus (D15 to D8) and lower-byte data bus (D7 to D0) are used for accesses. The amount of data that can be accessed at one time is one byte or one word.

Figures 5 and 6 illustrate data alignment control for the 16-bit access space. Figure 5 shows the data alignment when big endian is specified. Figure 6 shows the data alignment when little endian is specified.

In big endian, byte access to an even address is performed by using the upper-byte data bus and byte access to an odd address is performed by using the lowest-byte data bus.

In little endian, byte access to an even address is performed by using the lowest-byte data bus, and byte access to an odd address is performed by using the third-byte data bus.

Access Size	Access Address	Access Count	Bus Cycle	Data Size	Data Bus D15 D8 D7 D0
Byte	Even (2n)	1	1st	Byte	7 0
	Odd (2n + 1)	1	1st	Byte	7 0
Word	Even (2n)	1	1st	Word	15 8 7 0
	Odd (2n + 1)	2	1st	Byte	15 8
			2nd	Byte	7 0
Longword	Even (2n)	2	1st	Word	31 24 23 16
			2nd	Word	15 8 7 0
	Odd (2n + 1)	3	1st	Byte	31 24
			2nd	Word	23 16 15 8
			3rd	Byte	7 0

Figure 5 Access Sizes and Data Alignment Control for 16-Bit Access Space (Big Endian)

Access Size	Access Address	Access Count	Bus Cycle	Data Size	Data Bus (D15 D8 D7 D0)
Byte	Even (2n)	1	1st	Byte	7 0
	Odd (2n + 1)	1	1st	Byte	7 0
Word	Even (2n)	1	1st	Word	15 8 / 7 0
	Odd (2n + 1)	2	1st	Byte	7 0
			2nd	Byte	15 8
Longword	Even (2n)	2	1st	Word	15 8 / 7 0
			2nd	Word	31 24 / 23 16
	Odd (2n + 1)	3	1st	Byte	7 0
			2nd	Word	23 16 / 15 8
			3rd	Byte	31 24

Figure 6 Access Sizes and Data Alignment Control for 16-Bit Access Space (Little Endian)

4.2 Operation Example of Byte Access to 16-Bit Access Space

In this sample task, a 16-bit access space specified for little endian is accessed in bytes and little–big endian conversion is performed. Figure 7 shows an example of little–big endian conversion. The endian can be selected separately for each area by setting the ENDIANCR register of the bus controller.

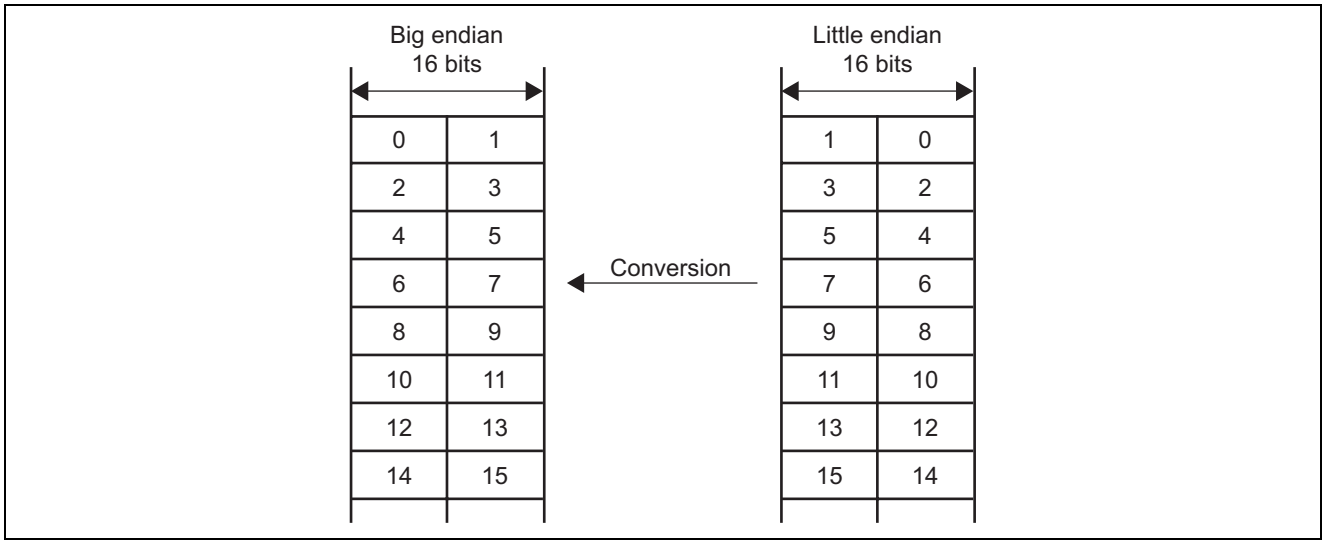


Figure 7 Example of Little–Big Endian Conversion

5. Description of Software

5.1 List of Functions

Table 3 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and clocks, cancels module stop mode, and calls the main function.
main	Main routine Calls the BscInit function, specifies the data format of area 3 as little endian, and transfers data in area 3 to on-chip RAM.
BscInit	Bus setting Connects area 3 to SRAM.

5.2 Vector Table

Table 4 Interrupt Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main

5.3 RAM Usage

Table 5 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	buf[16]	Area in on-chip RAM to which16 bytes of data from little endian area are stored in big endian format.	main
unsigned char	cs3area[16]	Little endian area (area 3)	main

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are shown below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	1	R/W	supplied to the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

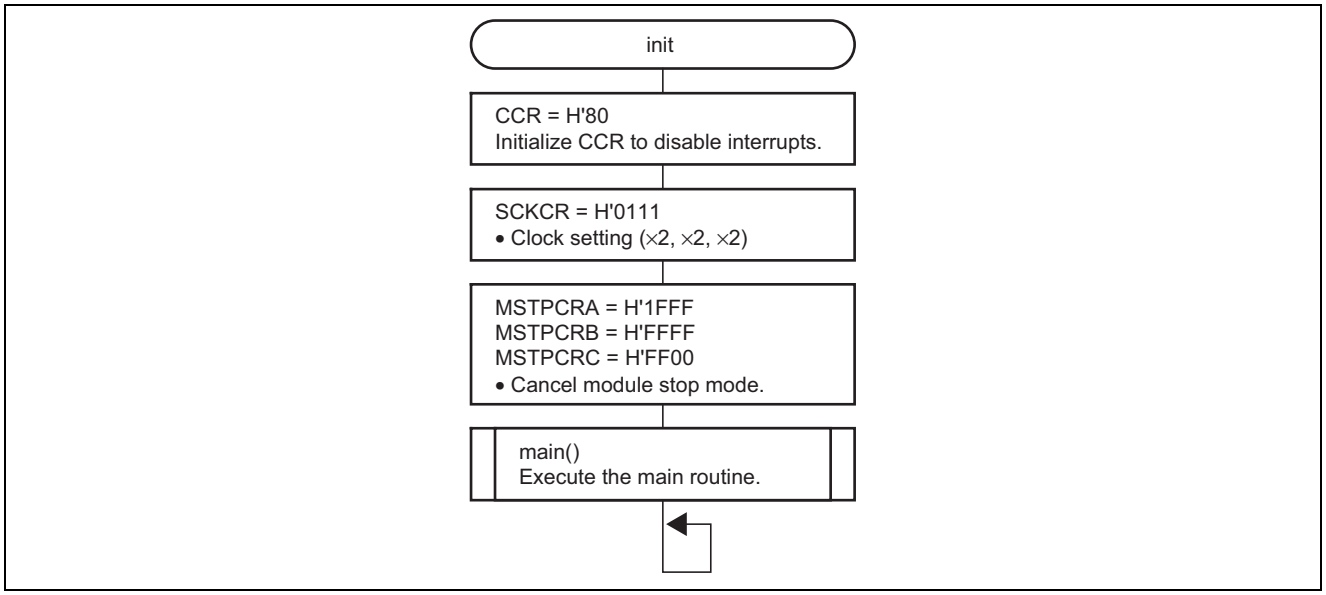
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6 and TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	CRC calculation unit
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart



5.4.2 main Function

(1) Overview of functions

Calls the BscInit function, specifies the data format of area 3 as little endian, and transfers data in area 3 to on-chip RAM.

(2) Argument

None

(3) Return value

None

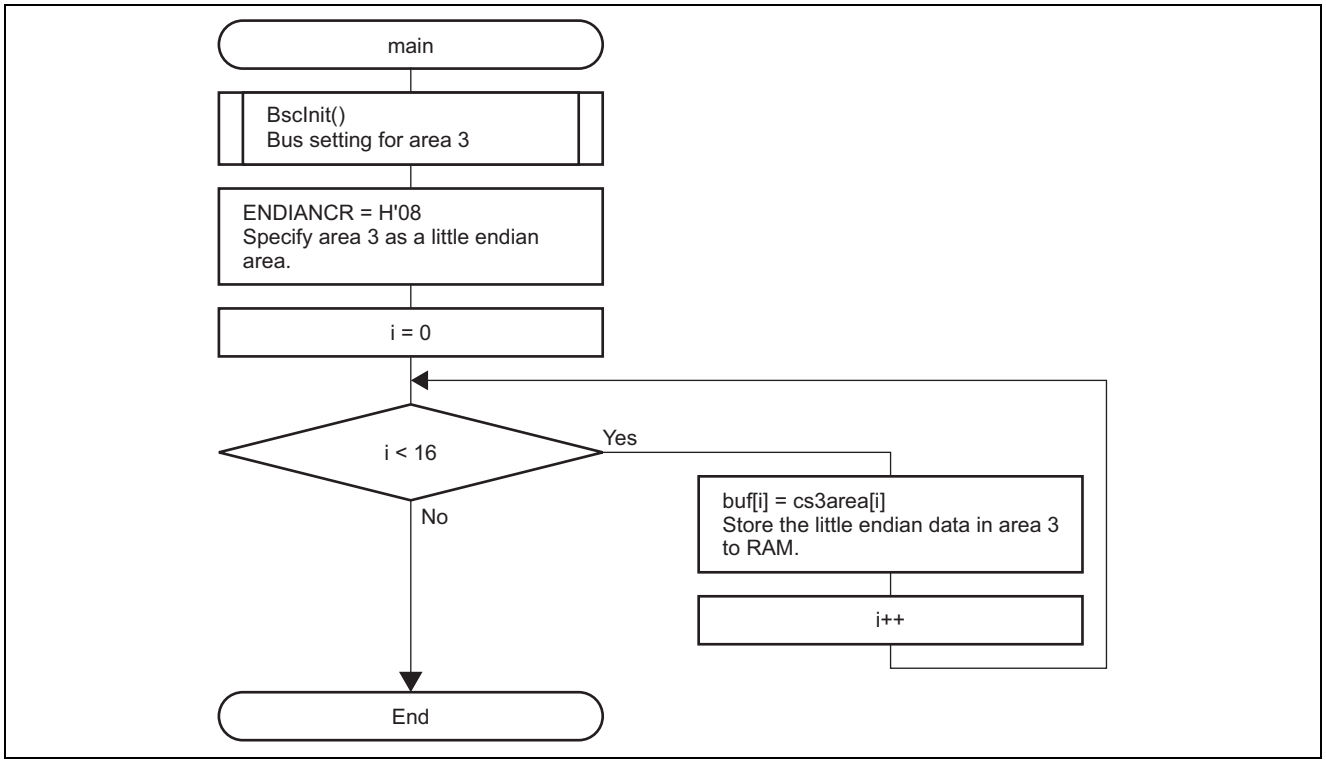
(4) Description of internal register

The internal register used in this sample task is shown below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Endian control register (ENDIANCR) Address: H'FFFD95

Bit	Bit Name	Setting	Function
7	LE7	0/0	Little Endian Select
6	LE6	0/0	LEn = 0: Data format of area n is specified as big endian
5	LE5	0/0	LEn = 1: Data format of area n is specified as little endian
4	LE4	0/0	
3	LE3	1/0	
2	LE2	0/0	

(5) Flowchart



5.4.3 BscInit Function

(1) Functional overview

Makes bus-related settings for area 3.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are shown below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port D data direction register (PDDDR) Address: H'FFFB8C
  Function: Sets the PD7 to PD0 pins to function as address output pins.
  Setting: H'FF

- Port E data direction register (PEDDR) Address: H'FFFB8D
  Function: Sets the PE7 to PE0 pins to function as address output pins.
  Setting: H'FF

- Bus width control register (ABWCR) Address: H'FFFD84
  Function: Specifies areas 7 to 0 as 16-bit access spaces.
  Setting: H'00FF

- Access state control register (ASTCR) Address: H'FFFD86
  Function: Specifies areas 7 to 0 as 3-state access spaces.
  Setting: H'FF00

- Wait control register B (WTCRB) Address: H'FFFD8A
  Function: Sets the number of program wait cycles. 7 program wait cycles are inserted for area 3.
  Setting: H'7000

- Read strobe timing control register (RDNCR) Address: H'FFFD8C
  Function: Sets the $\overline{RD}$ signal to be negated at the end of the read cycle in a read access to areas 7 to 0.
  Setting: H'0000

- Port function control register 0 (PFCR0) Address: H'FFFBC0

Bit	Bit Name	Setting	Function
7	CS7E	0	CS7 to CS0 Enable
6	CS6E	0	These bits enable/disable the corresponding $\overline{CSn}$ output.
5	CS5E	0	0: Pin functions as I/O port
4	CS4E	0	1: Pin functions as $\overline{CSn}$ output pin
3	CS3E	1	(n = 7 to 0)
2	CS2E	0	
1	CS1E	0	
0	CS0E	0	

- Port function control register 2 (PFCR2) Address: H'FFFBC2

Bit	Bit Name	Setting	Function
2	RDWRE	1	RD/$\overline{WR}$ Output Enable 0: Disables the RD/$\overline{WR}$ output 1: Enables the RD/$\overline{WR}$ output

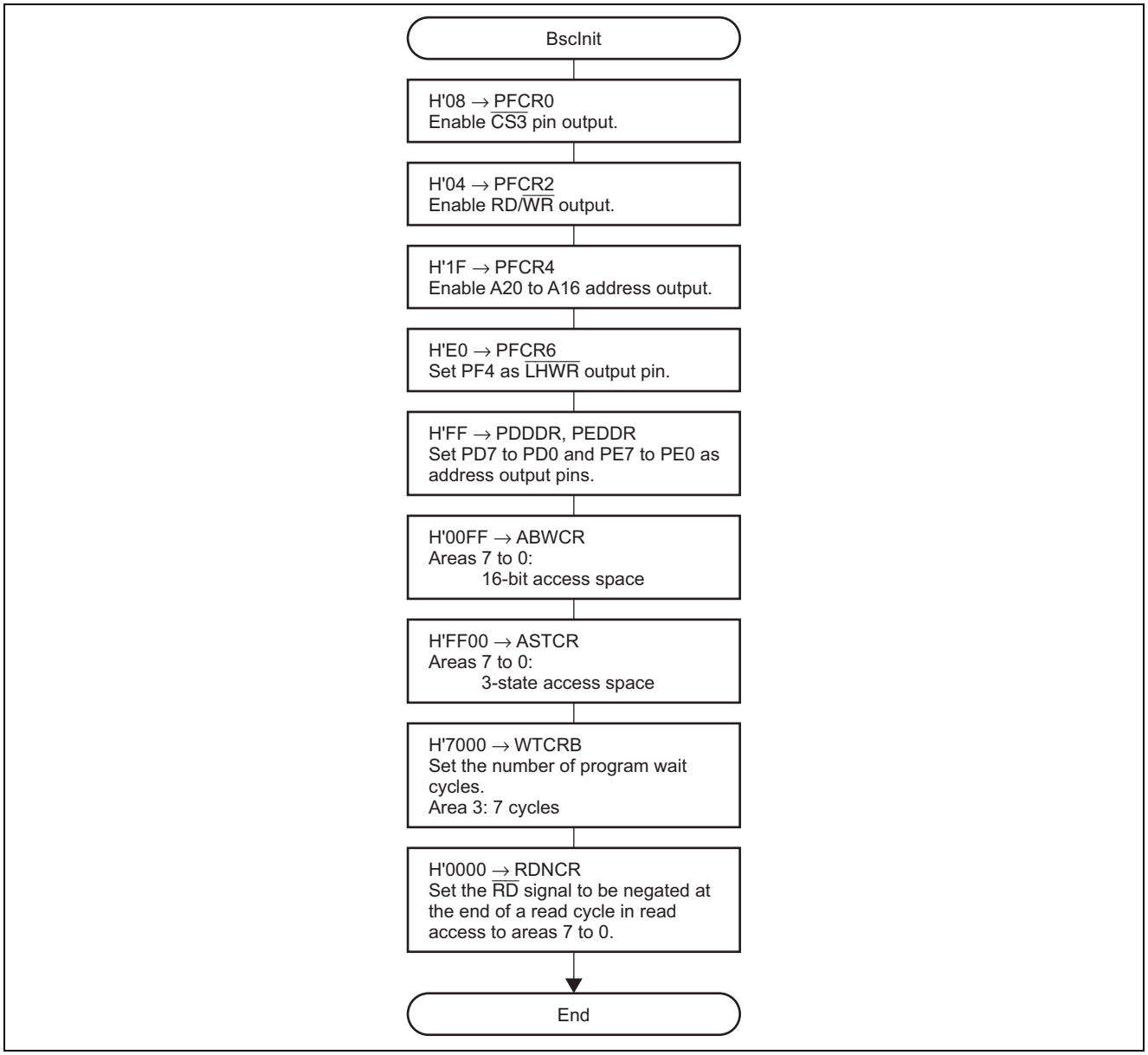
- Port function control register 4 (PFCR4) Address: H'FFFBC4

Bit	Bit Name	Setting	Function
4	A20E	1	Address A20 Enable 0: Disables the A20 address output 1: Enables the A20 address output
3	A19E	1	Address A19 Enable 0: Disables the A19 address output 1: Enables the A19 address output
2	A18E	1	Address A18 Enable 0: Disables the A18 address output 1: Enables the A18 address output
1	A17E	1	Address A17 Enable 0: Disables the A17 address output 1: Enables the A17 address output
0	A16E	1	Address A16 Enable 0: Disables the A16 address output 1: Enables the A16 address output

- Port function control register 6 (PFCR6) Address: H'FFFBC6

Bit	Bit Name	Setting	Function
6	LHWROE	1	$\overline{LHWR}$ Output Enable 0: Specifies pin PA4 as I/O port 1: Specifies pin PA4 as $\overline{LHWR}$ output pin

(5) Flowchart


BscInit
H'08 → PFCR0
Enable CS3 pin output.
H'04 → PFCR2
Enable RD/WR output.
H'1F → PFCR4
Enable A20 to A16 address output.
H'E0 → PFCR6
Set PF4 as LHWR output pin.
H'FF → PDDDR, PEDDR
Set PD7 to PD0 and PE7 to PE0 as address output pins.
H'00FF → ABWCR
Areas 7 to 0:
16-bit access space
H'FF00 → ASTCR
Areas 7 to 0:
3-state access space
H'7000 → WTCRB
Set the number of program wait cycles.
Area 3: 7 cycles
H'0000 → RDNCR
Set the RD signal to be negated at the end of a read cycle in read access to areas 7 to 0.
End

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1.00	Sep.11.06	—	First edition issued

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