Layout Recommendations for Optimal Thermal Dissipation in ProXO II

This application note describes the layout recommendations and correct operating environment for safe thermal operating conditions and thermal dissipation in ProXO II devices.

Contents

1. **Overview** 1
2. **XK Device Profile** 2
3. **Thermal Mitigation Techniques** 2
   - 3.1 Thermal Vias 2
   - 3.2 Placement 3
   - 3.3 Solder and Traces 3
   - 3.4 PCB 3
   - 3.5 Clamshell-type Test Sockets 3
4. **Power Supply** 3
   - 4.1 Lead Length 3
   - 4.2 Placement 3
5. **Reference Layout** 4
6. **Revision History** 5

1. Overview

The XK device belongs to Renesas' high performance ProXO II family. The devices are quartz-based PLL oscillators that offer ultra-low phase jitter while supporting a wide range of frequencies and output interface types. If the device is not operated in the correct environment, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management are critical elements in the successful application of the XK device. The XK device is specified to operate within the industrial temperature range of -40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature is not exceeded. At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device. A maximum junction temperature is listed in the XK datasheet with the ambient operating range. The ambient range and maximum junction temperature specifications ensure the performance of the device, as guaranteed in the Specifications section of the datasheet. Many variables contribute to the operating junction temperature within the device, including:

- Supply voltage
- Component size
- Ambient temperature

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The combination of these variables determines the junction temperature within the XK device for a given set of operating conditions. The XK is specified for an ambient temperature (T_A) range. Values of Theta JA are provided for package comparison and PCB design considerations. Theta J_A can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\text{Theta } J_A \times P_D)$$

where:

T_A is the ambient temperature (°C).

T_J is the junction temperature (°C).

Theta J_A is the junction to ambient thermal resistance found in the datasheet.

P_D is the power dissipation in W.

Values of theta J_A and theta J_B are provided in the datasheet for package comparison and PCB design considerations.

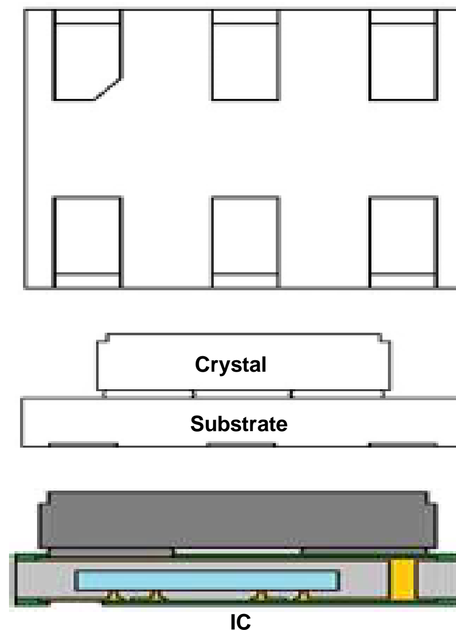
Example

For T_A = 70°C, Theta J_A = 96.7°C/W and P_D = 0.33W

$$T_J = 70 + (96.7 \times 0.33) = 101.9°C$$

2. XK Device Profile

The following image shows the XK device profile in relation to the temperature sensitive quartz element.



3. Thermal Mitigation Techniques

3.1 Thermal Vias

Use thermal vias attached to ground and power planes. This allows heat to flow from the device to the copper area away from the device.

3.2 Placement

Place the device away from the edge of the PCB and away from other high-power components. Devices placed near the edge of the PCB do not dissipate heat as well as those placed more centrally.

3.3 Solder and Traces

Consider using wider as well as thicker traces. Larger component pads can also be beneficial. Take care to ensure there is no voiding in the solder below the device.

3.4 PCB

Thicker PCBs can also improve thermal dissipation. This increases the thermal conductivity of the board and spreads the generated heat.

3.5 Clamshell-type Test Sockets

Frequency control devices are commonly tested in a clamshell-type socket with pogo pins as shown below.

Exercise great care when applying power to a device when using these sockets. The pogo pins do not provide the required thermal dissipation necessary to ensure the device does not exceed maximum junction temperature. Extended periods of applied power while in the socket will result in damage to the device and the socket.

4. Power Supply

Power the device with a quiet and well-regulated power supply. We recommend the use of 0.1μF bypass capacitors between V_{DD} and GND. Place the bypass capacitor as close as possible to the device.

4.1 Lead Length

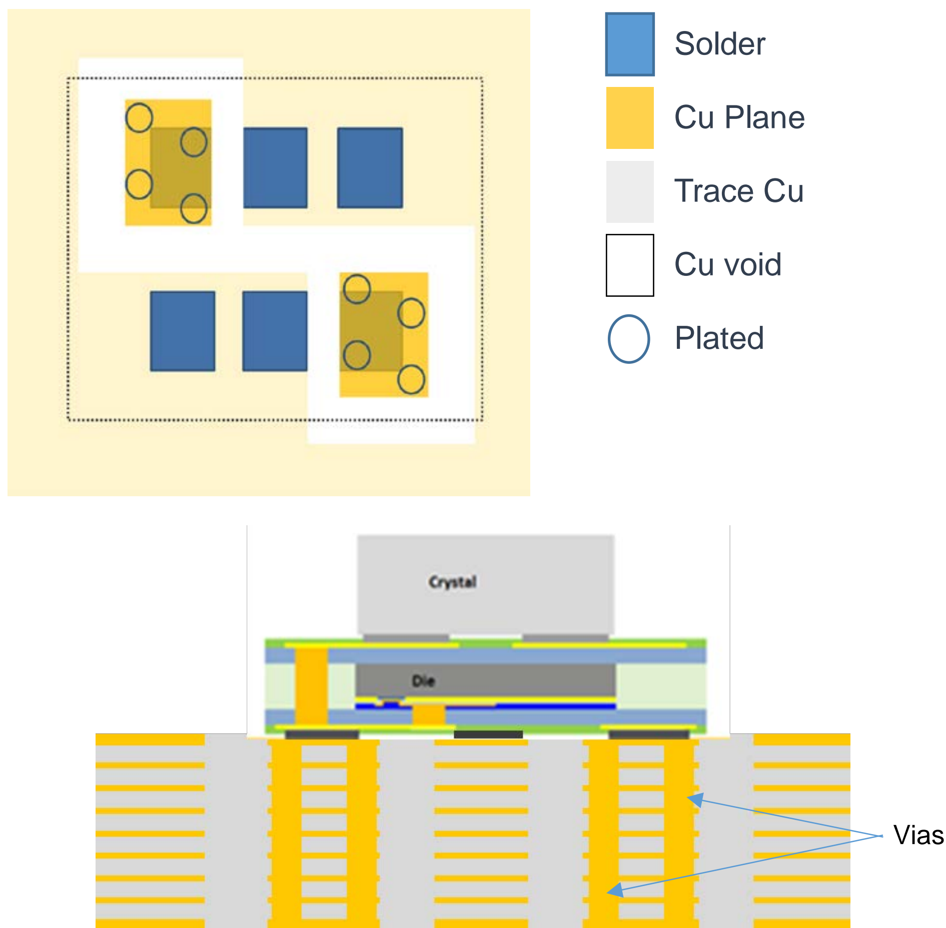
Keep the lead length between the device and clock receiver as short as possible.

4.2 Placement

Do not place the device near switching power supplies or other high frequency components.

5. Reference Layout

The following reference layout is based on devices programmed to HCSL outputs operating at 1.25GHz as a worst-case example. The reference board is 10-layer, 2oz copper on the top and bottom with the remaining layers 1oz copper. There is a Cu plane with 4 × 0.2mm vias for the GND plane and 4 × 0.2mm vias for V_{DD} plane.



The table below shows V_{DD}/GND plate area by package size and maximum dissipated power at 85°C for the reference layout.

Package Size	Max Power (at T_A 85°C)	Theta JA(˚C/W)	T_J(˚C)	V_{DD} Plane Area	GND Plane Area
1.8 × 1.4 mm	0.39 W	101.5	124.6	0.375 mm^2	0.375 mm^2
2.0 × 1.6 mm	0.37 W	106.4	124.4	0.375 mm^2	0.375 mm^2
2.5 × 2.0 mm	0.41 W	96.7	124.6	0.630 mm^2	0.630 mm^2
3.5 × 2.5 mm	0.47 W	85	125.0	1.01 mm^2	1.01 mm^2

6. Revision History

Revision	Date	Description
1.00	Jul 28, 2023	Initial release.

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