Layout Recommendations for FemtoClock 3W Devices

This document provides layout guidelines for a board that uses a FemtoClock3W (FC3W) device (e.g., RC38312, RC38108, RC38208, or RC38308).

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1. Introduction

To obtain the best performance from a FemtoClock3 Wireless device, the board layout must follow certain guidelines as described in this application note.

2. Power

Renesas recommends a dedicated power plane or power distribution network. Each FC3W device should have a dedicated LDO near the device on the same layer. Having dedicated power helps minimize voltage fluctuations and noise caused by other components sharing the same power supply network, and keeps noise from switching power supplies from causing spurs on the outputs of the FC3W. A short LDO output trace from a dedicated LDO will ensure a low IR drop between the LDO and the FC3W device because the trace has a lower inductance and a higher current carrying ability. In addition, the FC3W device should be kept away from noisy components such as switching regulators and high-current traces.

Please follow these general recommendations:

- Do not overlay power trace/plane from the two power layers.
- Do not run power lines parallel/adjacent for long stretches, even if they are of different layers.
- Cross power trace from different layers at 90 degrees – if the crossing is necessary.
- Keep power trace as thick as possible (while keeping a generous spacing to adjacent power lines) for lower resistance and lower inductance.

Of the power pins on the device, VDD_VCO is most sensitive to external noise while VDD_DIG is the noisiest. These two pins should be separated by a power supply pi-decoupling filter similar to the design in Figure 1.

In the power supply-decoupling filter, place 0.1uF bypass capacitors as close as possible to the power supply pins of the FC3W device (see C49 in Figure 1). A second 10uF capacitor near the device is also recommended if there is room. These capacitors help filter out high-frequency noise and provide a stable power supply. For additional filtering, we recommend a 4.7uF or 10uF capacitor with a larger package before the ferrite bead (see

C46 and C47 in Figure 1). If possible, avoid using vias and place the capacitors on the same layer as the device. For this case, the via cannot be avoided but it can eliminate the trace.

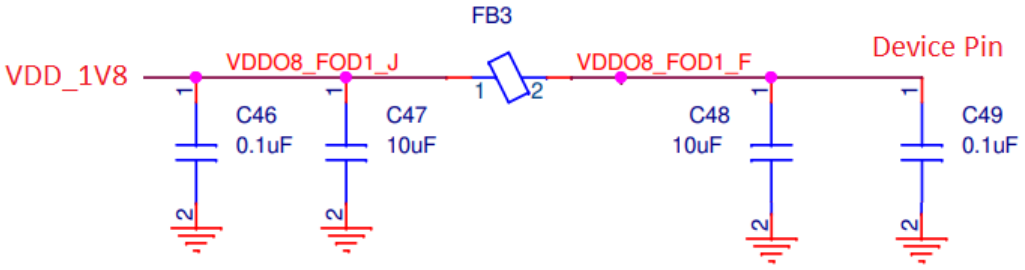


Figure 1. Example Decoupling Schematic Structure

Figure 2 shows that the bypass capacitors for the outer power pins can be placed at the same layout without via.

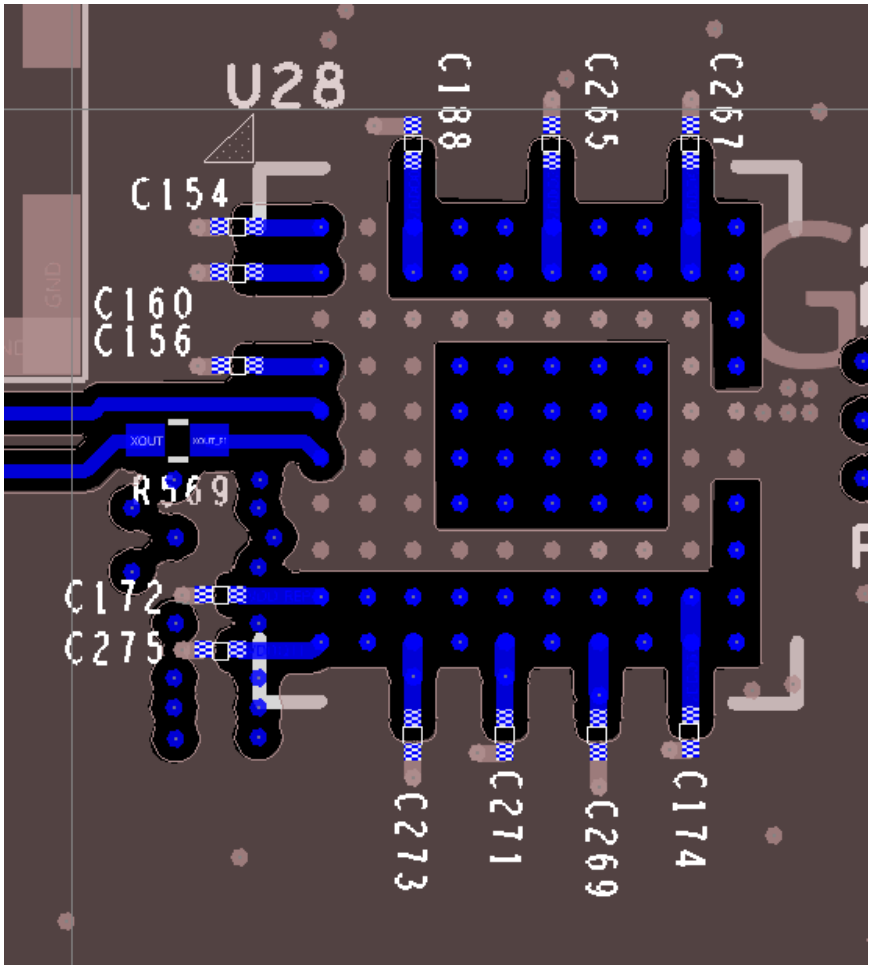


Figure 2. Decoupling Capacitors Placed at the Same Layout as FC3W

For the inner power pins, to minimize the power trace length, the bypass capacitors can be placed on the bottom layer and be located near the pins between power and ground as shown in Figure 3.

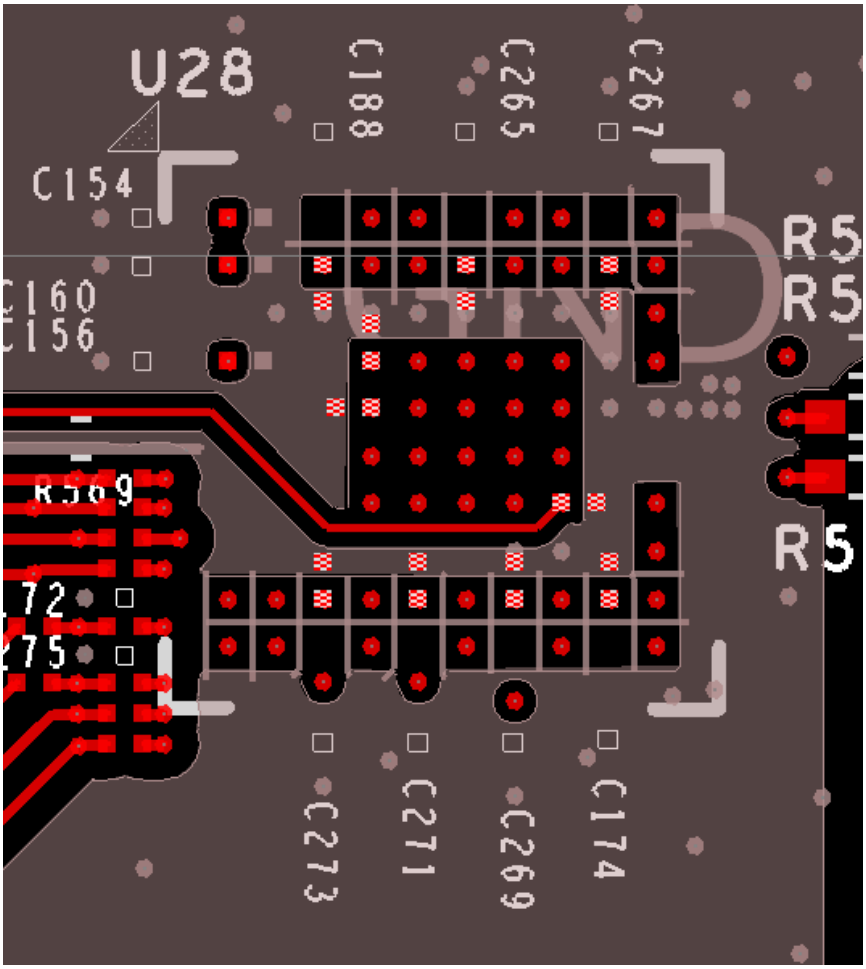


Figure 3. Inner Power Pins Bypass Cap Placed at the Opposite Layer to Avoid the Trace

The ground plane in the design should be a solid and low-impedance ground plane dedicated for clock devices. The ground pins of FC3W should be connected directly to this ground plane, minimizing ground loops and reducing ground noise.

We recommend that the design avoid unnecessary power planes below the FC3W device, so that supply noise and other currents do not couple into the sensitive clock circuitry.

3. Thermal Considerations

We recommend the maximize use of ground pins to provide sufficient heat transfer from the FC3W device to the substrate, and to provide a good ground for the device. Figure 4 shows the ground layer under the device to maximize the heat dissipation paths. The heat will couple from the top layer to the ground layer using the ground pins.

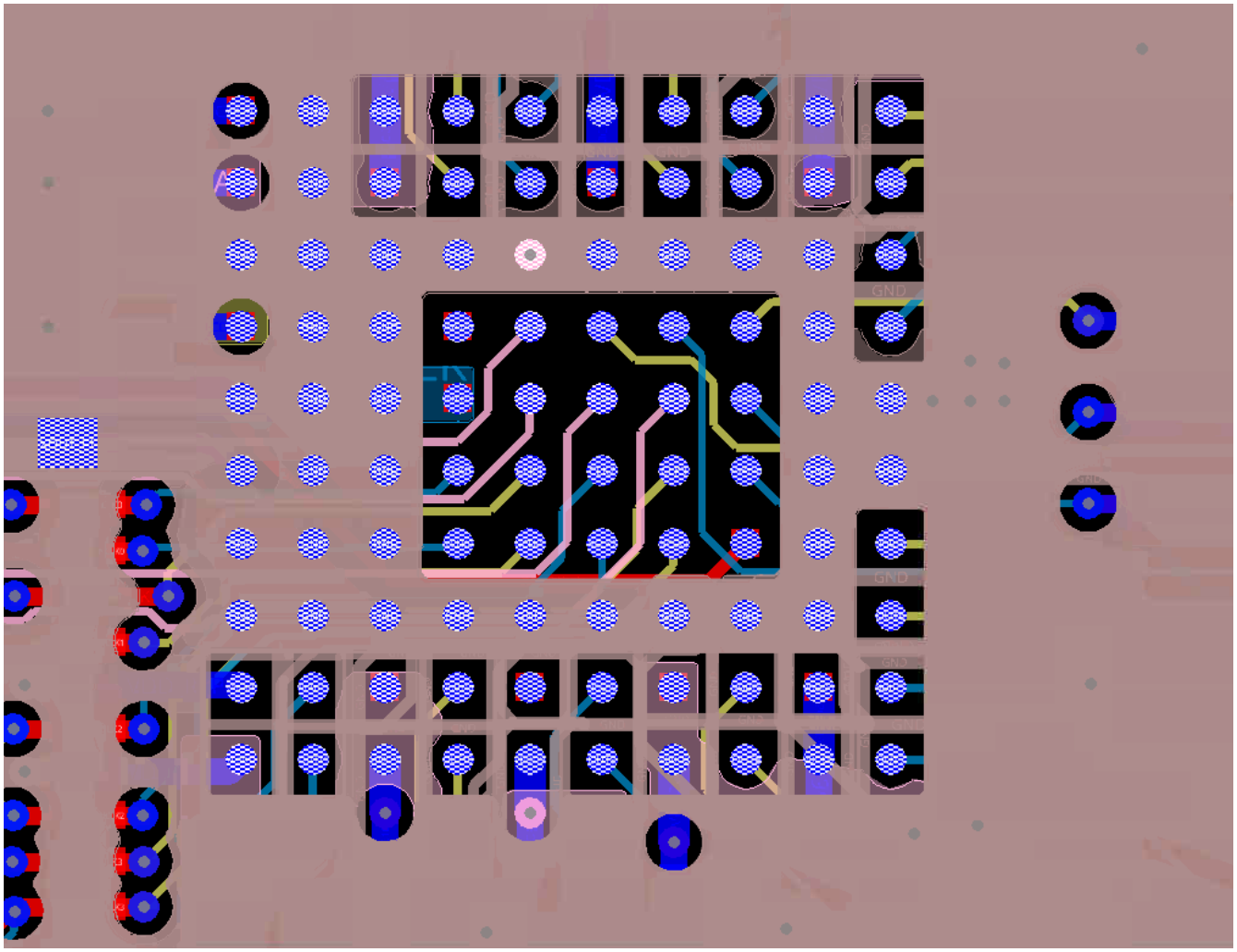


Figure 4. Layout Example for GND

4. Crystal

As with all Timing devices, careful attention is needed on the crystal circuit to ensure best device performance.

For the traces connecting the crystal to the device, the XOUT is low-impedance and XIN is high-impedance. To minimize noise coupling, XIN and XOUT should be as short as possible.

We recommend a GND plane channel (~3mil) around the crystal to isolate it from noise on the plane. The design must ensure that the load capacitors have a common ground plane.

Other signals should not cross the crystal keep-out area to minimize noise from coupling into the crystal traces or grounds. An example crystal layout is shown in the following figure.

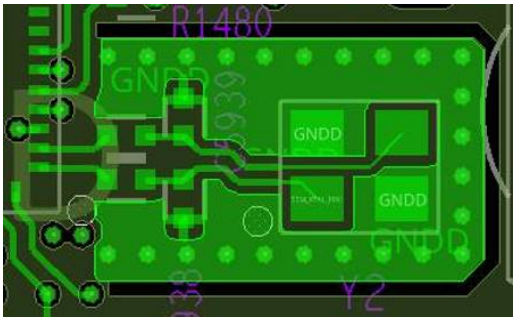


Figure 5. Crystal Layout Example

5. Clock Input and Output Routing

Clock signals must be routed carefully due to their sensitivity to noise and reflections.

The differential clock traces should be routed as 100Ohm signal pairs with impedance control per the PCB fabricator. The layout should minimize the use of vias. The signal should only switch layers at the driver and at the termination since the stubs from the vias will add reflections.

If required due to space, clocks from the same domain (frequency and phase) can run parallel. Clocks from different domains should not run parallel, though an exception can be made if they are on different signal layers, separated by multiple ground layers.

If space is available around the output clocks, then ground stitching can be added around the differential pair to prevent board noise from coupling to the signal.

For inputs, the termination should be placed near the receiver to minimize reflections. The reference ground via should be placed as close as possible to the source or receiver of the differential clock pair and ensure that the reference ground via connects to a continuous ground plane.

6. Layer Stack-Up

A PCB consists of multiple layers of copper (foil) and isolation materials laminated together. A PCB layer stack-up design refers to the layer arrangement of copper and dielectric material layers, with the total number of layers and the thickness of each layer taken into consideration.

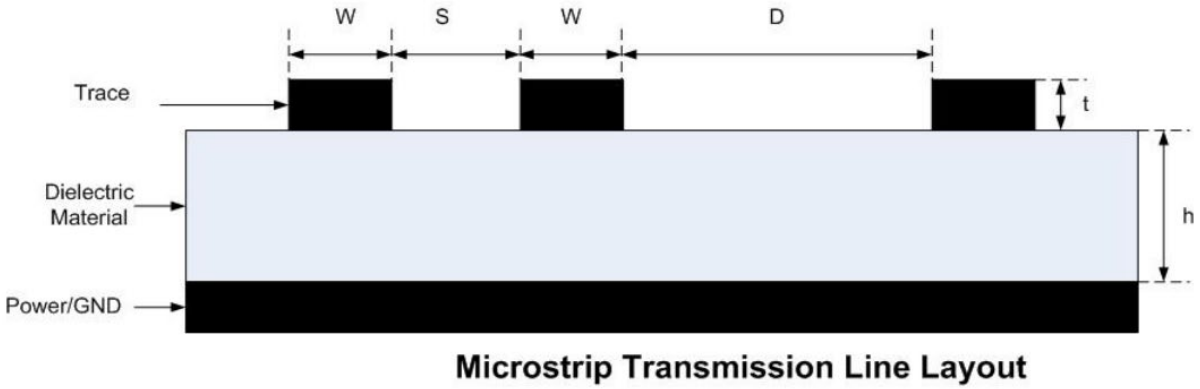
Planning optimal multilayer stack-up is one of the most critical factors in determining electromagnetic compatibility performance of a PCB. A well-designed layer stack-up can both minimize the radiation and stay robust from external noise sources.

The following two diagrams illustrate the significance and relationships of signal impedance and EMC control with the PCB layer stack-up.

A signal trace that is suspended over a ground plane with a dielectric layer between them is call a microstrip. The impedance of the microstrip trace is determined by a number of factors in the PCB and its stack-up arrangement:

- Signal trace width
- Thickness of the trace (thickness of copper layer)
- Distance between the two traces if it is a differential pair
- Thickness of the dielectric layer between a microstrip and the ground plane under the dielectric layer
- Dielectric constant Er

The microstrip structure is displayed in Figure 6 and the impedance is shown in Figure 7 (for more information, see ANSI IPC-D-317A).



Microstrip Transmission Line Layout

W = Width of trace
t = Thickness of trace
h = Height between trace and reference plane
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

Figure 6. Microstrip Signal Example

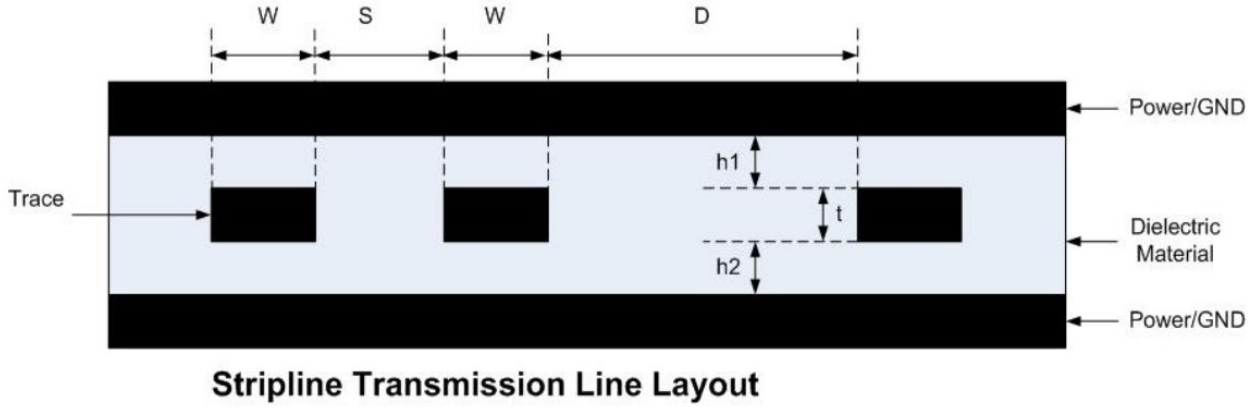
$$Z_o = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w+t)}\right] ohms$$

$$Z_{diff} \cong 2Z_o\left(1 - 0.48e^{-0.96\frac{s}{h}}\right) ohms$$

Figure 7. Microstrip Signal Impedance

When a signal trace changes layers, the above factors affecting trace impedance change as well. Caution must be exercised in order to keep the signal impedance continuous to avoid signal integrity impairments.

Another signal type is called a stripline signal, which is one sandwiched between two dielectric material layers. The stripline structure is displayed in Figure 8 and the impedance is shown in Figure 9.



Stripline Transmission Line Layout

W = Width of trace
t = Thickness of trace
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

Figure 8. Stripline Signal Example

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9(2(h1+h2)+t)}{0.67\,\pi(0.8w+t)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\ e^{-2.9\left[\frac{s}{h1+h2}\right]}\right)$$

Figure 9. Stripline Signal Impedance

For a design with FC3W, we recommend that the clock signals be protected from ambient noise by using the stripline internal trace structure (i.e., sandwiching them between two ground planes).

The FC3W Rev C evaluation board stack-up is displayed in Figure 10.

- The evaluation board uses an 8-layer board.
- There are five copper planes for power and ground – three layers are ground and one layer is dedicated to power. The SIG_3 layer is between ground layers GND2 and GND4, and the SIG_7 layer is between ground layers GND6 and BOTTOM. This generous number of ground and power planes will help the board's EMC performance. (Depending on signal density, not every PCB board can dedicate such an abundant number of copper planes.)
- The evaluation board uses Nanya NPLD-II material due to its low losses at the frequency supported by this device. Other Renesas boards that support similar maximum clock frequencies use other FR4 materials for similar performance.

STACKUP TABLE				
Unit = Mils				
#	NAME	TYPE	MATERIAL	THICKNESS
		SURFACE	AIR	0
	SOLDERMASK_TOP	MASK	NANYA NPLD-II	1
1	TOP	CONDUCTOR	1OZ_COPPER	1.4
		DIELECTRIC	NANYA NPLD-II	4.6
2	GND2	PLANE	1OZ COPPER	1.4
		DIELECTRIC	NANYA NPLD-II	10
3	SIG_3	CONDUCTOR	1OZ_COPPER	1.4
		DIELECTRIC	NANYA NPLD-II	4.6
4	GND4	PLANE	1OZ_COPPER	1.4
		DIELECTRIC	NANYA NPLD-II	10
5	PWR5	PLANE	1OZ COPPER	1.4
		DIELECTRIC	NANYA NPLD-II	4.6
6	GND6	PLANE	1OZ COPPER	1 4
		DIELECTRIC	NANYA NPLD-II	10
7	SIG_7	CONDUCTOR	1OZ_COPPER	1.4
		DIELECTRIC	NANYA NPLD-II	4.6
8	BOTTOM	CONDUCTOR	1OZ_COPPER	1.4
	SOLDERMASK BOTTOM	MASK	NANYA NPLD-II	1
		SURFACE	AIR	0
			TOTAL THICKNESS	61.6

Figure 10. Example Stack-up for FC3W

7. Revision History

Revision	Date	Description
1.00	Oct 4, 2023	Initial release.

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