JEDEC Hardware Reset in Renesas NOR Flash

JEDEC hardware reset is a standard signaling protocol which allows a host to reset a serial Flash device. The standard was developed by JEDEC Solid State Technology association, a consortium of the semiconductor industry. It is published as JEDEC JESD252 standard.

Due to pin count constraints, many Flash products do not provide a hardware reset pin. Others provide a non-dedicated reset pin: the pin can be used as a reset signal or as another type of signal such as an I/O signal, depending on the setting of the status/configuration registers. This means that hardware reset is not available at all times, or some action is required before the reset pin can be used for hardware reset.

The JEDEC hardware reset standard allows the host to reset a serial Flash device without a dedicated reset pin. The protocol uses the same pins which are used for SPI communication with the Flash. Sometimes this is called SPI protocol reset or in-band reset. This hardware reset functionality is available in any configuration.

Many Renesas NOR Flash products support the JEDEC hardware reset standard. Please check the Features section of the specific product's datasheet to see if it supports this feature.

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1. Reset Signaling Procedure

The JEDEC hardware reset signaling procedure involves two active SPI signals which are driven by the host:

- $\overline{CS}$
- SI / IO_0

In addition, the SCK signal is required to stay in a constant state, either high or low. This is done so that no command bits will be accidentally clocked out and transferred to the Flash.

The procedure consists of 4 phases. In each phase $\overline{CS}$ is asserted (driven low) and de-asserted (driven high). After $\overline{CS}$ is asserted, SI is driven low or high, alternating its state on each phase. In other words:

- With the first $\overline{CS}$ assertion SI is driven low.
- With the second $\overline{CS}$ assertion SI is driven high.
- With the third $\overline{CS}$ assertion SI is driven low.
- With the fourth $\overline{CS}$ assertion SI is driven high.

Note: The Flash captures the state of SI on the rising edge of $\overline{CS}$.

With the $\overline{CS}$ de-assertion in the fourth phase the reset signaling procedure is complete. The Flash device goes through a hardware reset which is completed within a period of t_{RST}, as specified in the datasheet.

One way to look at this sequence is to think of $\overline{CS}$ as a clock signal and SI as data signal sampled on the rising edge of that clock. If after four clock cycles the sampled binary data is equal to 0101b then hardware reset takes effect.

The signaling procedure is illustrated in Figure 1:

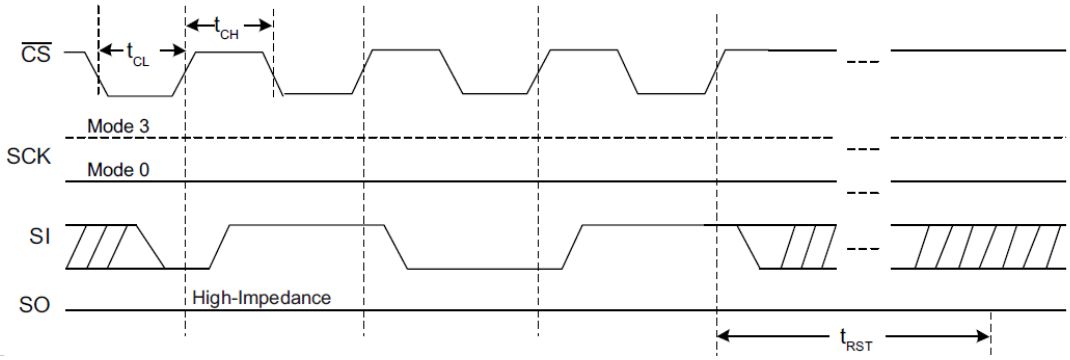

Figure 1. Signaling Procedure

Note: the t_{CL} and t_{CH} periods are required to be at least 500 ns long.

2. Code Implementation

This section includes a simple C code example which implements the JEDEC hardware reset procedure on a typical MCU. The 3 SPI pins involved in the procedure ($\overline{CS}$, SCK, SI) are used as General Purpose I/O (GPIO) signals (see note below). The API has a simple function call for driving the GPIO signals high (1) or low (0).

Notes:

- The pins were configured as GPIO signals prior to the reset procedure. In most MCUs pins have alternate functions which can be configured by the user. The 3 pins involved in the reset procedure are mostly used for SPI communication in which case they are controlled by the MCU's Flash SPI controller and are named $\overline{CS}$, SCK and SI (or similar names). They can also be used as GPIO signals in which case they are controlled by the MCU's GPIO controller and are referred to with GPIO pin numbers (typically a combination of GPIO port number and a pin number within the GPIO port). For implementing the JEDEC hardware reset signaling procedure we use these pins as GPIO signals since the Flash SPI controller cannot generate that signaling sequence. After the code example shown here is complete the pins should be reconfigured as SPI signals.
- In this example port GPIO3 pin 6 is the same pin used as $\overline{CS}$ for SPI communication.
- In this example port GPIO3 pin 7 is the same pin used as SCK for SPI communication.
- In this example port GPIO3 pin 8 is the same pin used as SI for SPI communication.
- The GPIO_WritePinOutput() function is a basic GPIO function which simply drives a specified GPIO signal low or high. Its first 2 arguments specify the GPIO port and pin number. The last argument specifies low output (0) or high output (1).

```
// SCK is driven low or high and must stay in one state
   GPIO_WritePinOutput(GPIO3, 7, 0); // set SCK low
   for(i = 0; i < 4; i++)
   {
      // drive CS low
      GPIO_WritePinOutput(GPIO3, 6, 0);
      // drive SI low or high: alternate its state every iteration
      GPIO_WritePinOutput(GPIO3, 8, (i&1));
      // drive CS high; SI state will be captured on the CS rising edge
      GPIO_WritePinOutput(GPIO3, 6, 1);
   }
```

As seen above, the JEDEC hardware reset signaling is implemented in the code with a loop of four iterations, matching the four phases of the procedure. In each iteration $\overline{CS}$ is driven low and later high. After $\overline{CS}$ is driven low SI is driven low or high, alternating its state on each iteration. The value for driving SI low (0) or high (1) is simply based on the least significant bit of the loop counter.

3. Applications and Advantages

3.1 General

In general, JEDEC hardware reset can be used to reset the Flash device any time. As mentioned earlier, this is done without a dedicated reset pin. It's worth mentioning that JEDEC hardware reset can be applied regardless of the mode the Flash device is in. This makes it a more robust reset solution compared to software reset. Software reset requires sending two commands to the Flash. However, the Flash device could be in a mode where it doesn't accept all commands. For example, when the Flash is in continuous read mode (command format 0-4-4) it accepts read commands only. In that scenario sending a software reset requires the Flash to exit that mode first. In contrast JEDEC hardware reset can be applied while the Flash device is in continuous read mode. In other words, JEDEC hardware reset can be applied instantly at any time.

3.2 Recovering from an Incomplete POR

JEDEC hardware reset has been found useful in cases where the power-on reset (POR) is incomplete.

In cases where the system design doesn't follow the power-on requirements, power-on-reset (POR) may not complete successfully. When this happens the flash chip is not initialized correctly. This may lead to failure sooner or later.

However, if POR is not successfully completed a JEDEC hardware reset can re-initialize the Flash correctly. This essentially fixes the POR failure in such a case and avoids any potential failure later on. This has been clearly proved in testing. Some customers who had marginal power-up sequences (in terms of compliance with datasheet requirements) and initially observed some failures because of that, reported that applying JEDEC hardware reset right after power-up diminished the failure rate or made failures disappear altogether.

3.3 Extending V_{CC} Ramp-Up Time

As an example of the capability to recover from an Incomplete POR, JEDEC hardware reset has the following application: In certain NOR Flash products there is relatively low tolerance for slow V_{CC} ramp rate during power-up. However, if JEDEC hardware reset is applied at the end of the power-up, the Flash memory can tolerate much slower V_{CC} ramp rates. This is because the reset cures any potential initialization problems which could arise due to the slow V_{CC} ramp rate.

3.4 Applying JEDEC hardware reset after power-up

To apply JEDEC hardware reset after power-up, wait t_{VSL} time after Vcc reaches the minimal operating value for the flash chip. At this point, the host can initiate the JEDEC hardware reset signaling procedure.

Note: t_{VSL} is the same parameter used in the datasheet to specify when the flash chip is fully operational after reaching minimum Vcc during power-up.

4. Revision History

Revision	Date	Description
A0	7 / 2025	Initial release.
A1	8 / 2025	Updated document title and introduction. Updated Section 3.3 ‘Extending V_{CC} Ramp-Up Time.’

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