iW1602 and iW1702 Design Guidelines

Introduction

This application note provides a design approach for creating power supplies based on the iW1602 and iW1702 AC/DC Controllers.

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1. Overview

The iW1602 and iW1702 are AC/DC controllers that use a proprietary digital algorithm enabling tight regulation of output voltage and current without direct feedback from the secondary side. The controllers operate in discontinuous mode (DCM) using quasi-resonant, peak current mode control. This is achieved using the Renesas **PrimAccurate**™ digital control technology, which enables a true primary-side regulation technique that eliminates the need for an optocoupler for voltage and current feedback. For additional details and description on the two devices, refer to the corresponding datasheets.

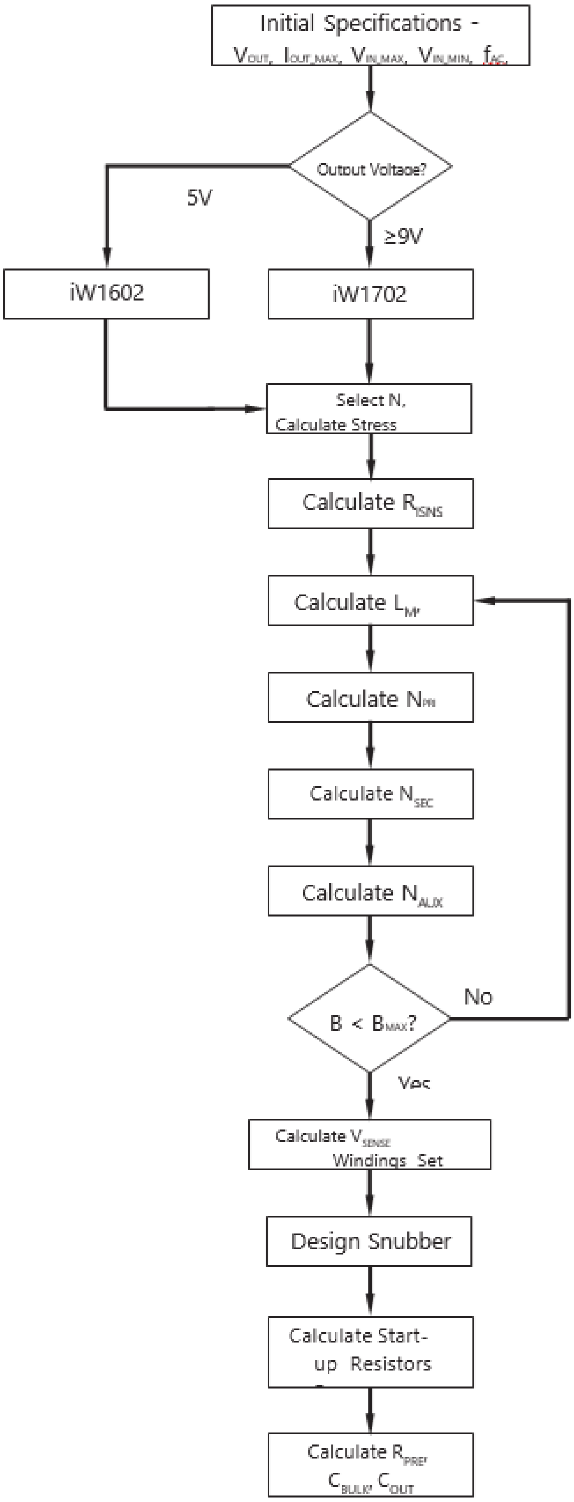


Figure 1. Design Flowchart

2. Terms and Definitions

Term	Definition
$V_{IN\_AC\_MIN}$	The minimum AC input voltage.
$V_{IN\_AC\_MAX}$	The maximum AC input voltage.
$V_{IN\_DC\_MIN}$	The minimum DC voltage seen at the bulk input capacitor.
$V_{IN\_DC\_MAX}$	The peak DC voltage of the rectified AC input voltage.
V_{SEC}	The output voltage directly at the secondary of the transformer.
N:	Turns ratio, Primary-to-Secondary.
N_{PRI}	Number of turns on the primary.
N_{SEC}	Number of turns on the secondary.
N_{AUX}	Number of turns for the auxiliary winding.
V_{FD}	Forward voltage drop of secondary-side rectifier.

3. Initial Criteria – Design Parameters and Assumptions

Digital AC/DC controllers from Renesas use discontinuous conduction mode (DCM) control. This is distinguished from continuous conduction mode (CCM) in that on each cycle, all of the energy stored in the core of the transformer is transferred fully to the secondary during the off-time. In CCM mode, the energy in the transformer never goes to zero, and therefore the primary and secondary currents never reach zero. There are inherent advantages to both topologies, but DCM control enables the quasi-resonant control used by Renesas to improve efficiency, reduce EMI and maintain a small overall circuit size.

The initial design parameters are fundamental and need to be clearly defined prior to starting any design. Once the application design criteria are confirmed, the main controller can be selected. The iW1602 and iW1702 devices share the same core control technology, where the iW1602 is optimized for 5V applications with a maximum power rating up to approximately 30W and the iW1702 is optimized for higher output voltages (≥ 9V) with a power rating up to 45W and output drive capability for load capacitances up to 6,000µF.

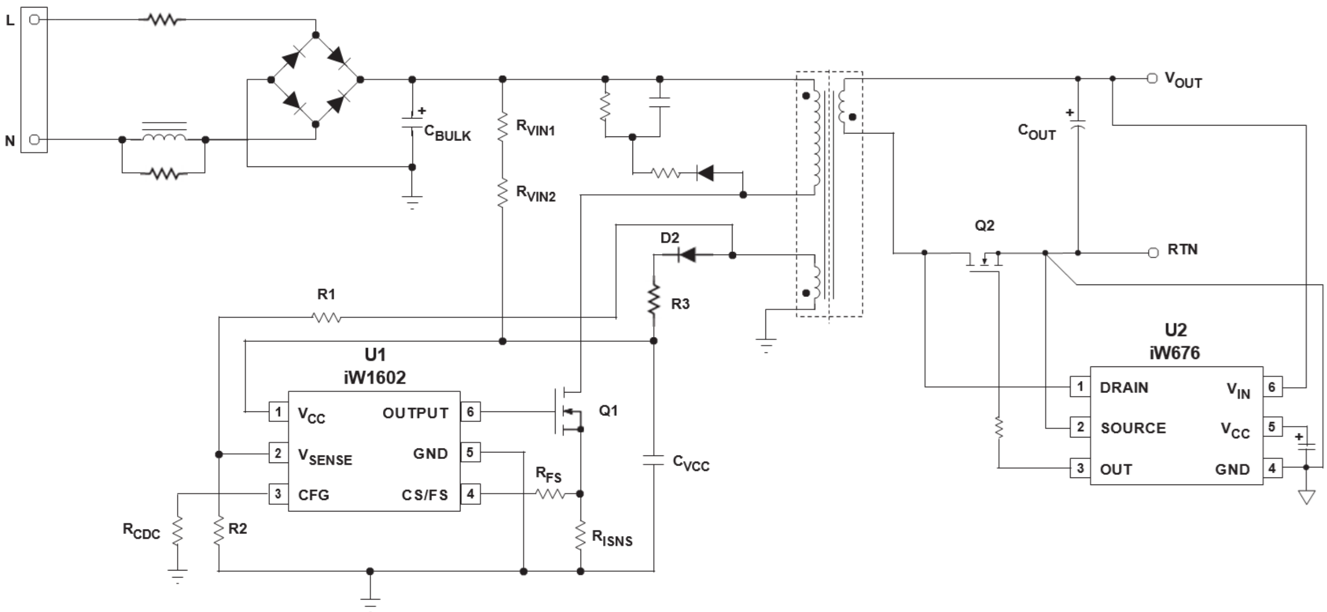


Figure 2. iW1602 Typical Applications Circuit

In this document, the iW1602 is used as the design example, however, where there are differences between using the iW1602 or iW1702, explanations are given to account for the differences between the two devices. Tables 1–3 shows the design example conditions, the constraints/constants for each device and some design assumptions made to start the design process.

Table 1. Design Example Conditions

Name	Conditions	Unit
V_{IN}	90-264	VAC
f_{AC}	47-63	Hz
V_{OUT}	5	V
I_{OUT} (continuous)	2	A
No-load power consumption (max)	75	mW
Cable Length	1	m
MOSFET V_{DS} Derating Factor	10 [1]	%
Rectifier V_{RRM} Derating Factor	10 [1]	%

1. These specifications are application dependent, see section 5 for more details.

Table 2. Design Constraints and Constants

Name	iW1602	iW1702	Unit
k_{CC}	0.422	0.422	-
t_{RST_MIN}	1.2	1.2	µs
f_{SW_MAX}	89	79	kHz
V_{CC_ST} (Start-Up Threshold)	12.7	12.0	V
I_{CC_ST} (Start-Up Current)	10	10	µA
V_{UVLO}	5.5	6.4	V
V_{IPK_HI}	1.0	1.0	V
V_{IPK_FL}	[1]	[1]	V
V_{IPK_LO}	[2]	[2]	V

1. This value is selectable by design and depends upon the end application. See sections 6, 7, and 8 for more details.
2. This value depends upon the LOM mode of operation selected for the design. See section 7 for more details.

Table 3. Design Example Assumptions

Name	Symbol	Value
Transformer Efficiency	17TX	95%
Power Supply Efficiency	17	90%

4. Cable Drop Compensation

The iW1602 and iW1702 digital AC/DC controllers contain an internal voltage compensation circuit for voltage drop across any cable, wire or PCB trace between the output of the power supply and the load. This is common in charger and adapter applications but can be found in any application where the power supply is located far from the load. The discrete voltage levels for cable drop compensation are internally set and selectable via an external resistor to ground.

The actual voltage drop needs to be estimated.

$$V_{CABLE} = R_{CABLE} \times I_{OUT}$$ **Eq. 1**

The resistance of the cable can either be a real cable or a PCB length. For a cable, Table 4 shows the resistance per meter for different wire gauges. Both the power lead and ground lead of the cable/PCB trace must be taken into consideration when calculating the voltage drop. Since the ground conductor length and power conductor length of the cable are approximately the same, simply multiplying the length of cable by two compensates for this double lead length. Equation 2 shows how to calculate the cable resistance.

$$R_{CABLE} = \rho_{CABLE} \times 2L$$ **Eq. 2**

Table 4. Wire Gauge Resistivity

Wire Gauge	π_{CABLE}	Unit
20AWG	33.3	mν/m
22AWG	53.1	mν/m
24AWG	84.2	mν/m
26AWG	134.5	mν/m
28AWG	212.9	mν/m

Using the example conditions and specifications from Table 1 showing a 1m length of cable, an approximate cable drop compensation value can be calculated by following a few simple steps. First, calculate the approximate iW1602 and iW1702 resistance of the cable using Equation 2. The cable, in this example, is a 24AWG gauge cable.

$$R_{CABLE} = 84.2\text{m}\Omega/\text{m} \times 2 \times 1 = 0.168\Omega$$ **Eq. 3**

And the voltage drop is:

$$V_{CABLE} = 0.168\Omega \times 1\text{A} = 0.168\text{mV}$$ **Eq. 4**

The iW1602 IC uses an algorithm that calculates the cable drop compensation level for a 5V output. The iW1702 is optimized for higher output voltages such as 12V, and the cable drop compensation level adjusts to the output voltage level. To calculate the adjusted value, use Equation 5.

$$V_{CDC} = \frac{V_{OUT}}{5} \times V_{CDC\_5V}$$ **Eq. 5**

where V_{CDC} is the actual cable drop compensation required for the output voltage of the application, V_{OUT} is the output voltage of the application and V_{CDC_5V} is the actual CDC voltage that the controller would normally provide at 5V output.

Select the closest value to the calculated CDC value and the programming resistor from the CFG pin to ground to set the CDC level. Table 5 shows the cable drop compensations voltages for both 5V and 12V outputs. For other output voltages, use Equation 5. For the design example, the closest pre-set CDC value to the calculated required voltage level is 150mV.

Table 5. Cable Drop Compensation Resistor Values

R_{CDC} Range	1.5–2.2kv	2.37–3.21kv	3.40–4.64kv	4.87–6.65kv	6.98–10kv
CDC – 5V Output	0mV	75mV	150mV	300mV	450mV
CDC –- 12V Output	0mV	180mV	360mV	720mV	1080mV

The correct resistor value for the design example is the 3.40–4.64kv range. It is recommended to select the standard 1% resistor value closest to the center of the range. For the design example, that resistor value is 4.02kv.

The cable drop compensation function is intelligently controlled and changes with the load such that at no load, the cable drop compensation voltage is 0V. This way, the voltage at the load stays within the required range.

Note that the CFG pin can also be used for optional output OVP or input OVP protection using a simple resistor divider network from the aux winding to the CFG pin and then to ground. For more details, refer to the datasheet.

5. Turns Ratio, Voltage Stress (V_{DS} and V_{RRM}), Power MOSFET and Secondary-Side Rectifier

The next step is to determine the necessary turns ratio for the design. The turns ratio (N) is the ratio of primary-side turns to secondary-side turns (N_{PRI}/N_{SEC}). The iW1602, which is optimized for 5V output voltages works with a turns ratio of approximately 15. The iW1702, which is optimized for ≥ 9V output voltages, works with a lower turns ratio (~6 for $12V_{OUT}$; ~8 for $9V_{OUT}$). Later in the design, the precise value will be determined. For the design example, 15 is used for now.

The maximum voltage seen across the Drain-Source of the primary-side FET is determined by three main factors: the maximum input voltage, the reflected output voltage and a spike of voltage determined by the leakage inductance on the primary side. The input voltage and reflected output voltage are clearly determined, but the parasitic element cannot be easily determined, so a worst-case estimate for that value can be used for the purpose of calculating the maximum voltage. Typically transformer leakage inductance is specified to be < 5% of L_M when the secondary and auxiliary windings are shorted and measured at 10kHz. Equation 6 shows the calculation for max V_{DS}.

$$V_{DS\_MAX} = V_{IN\_DC\_MAX} + (1.5 \times N \times V_{OUT\_PCB}) \qquad \textbf{Eq. 6}$$

The $N^*V_{OUT\_PCB}$ term is the reflected output voltage and the 1.5x factor accounts for the spike voltage caused by leakage inductance, estimated to be 1.5x the reflected output voltage. V_{OUT_PCB} is the value at the PCB including the cable drop compensation component, in the design example, 150mV for a V_{OUT_PCB} value of 5.15V.

The voltage stress across components vs turns ratio can be graphed over a range of turns ratios in order to assist in the best selection of N. The lower the turns ratio, the lower the voltage on the primary-side FET. But the turns ratio has the opposite effect on the secondary-side rectifier, as shown by Equation 7.

$$V_{RRM} = \left(\frac{V_{IN\_DC\_MAX}}{N} + V_{OUT\_PCB} \right) \times K_{DIO} \qquad \textbf{Eq. 7}$$

The K_{DIO} value is a derating factor to account for ringing on the secondary-side rectifier. This factor is 1.2 to give 20% margin for voltage ringing. This derating factor depends upon the end user's requirements and can vary whether using a Schottky diode rectifier or SR MOSFET. For the design example, a 20% derating factor is used.

Graphing these two equations (see Figure 3) for the design example using a turns ratio between 14.5 and 16 will give an indication of where to set the definitive turns ratio based on the optimization of voltage ratings on the main switch and the secondary-side rectifier. Understanding this relationship will help select the voltage ratings for the primary and secondary-side components. The maximum voltage expected on the primary side and the maximum voltage rating selected for the MOSFET also determine the clamping voltage level need for the snubber design discussed in section 11. For the design example, the range between 14.8 and 15.4 is ideal for the main switch. As mentioned earlier, the iW1602 is optimized for use with a turns ratio of approximately 15 and based on the V_{DS} curve and the V_{RRM} curve, that value is a good starting point for voltage stress as well.

The turns ratio selected determines the voltage rating on both devices. The primary-side MOSFET needs to hold off the voltage shown in Figure 3 with sufficient margin for safety. It is recommended to derate the MOSFET V_{DS_MAX} voltage by at least 10% when selecting an external MOSFET, although that derating factor will vary depending upon the designer's own criteria for quality and reliability. If a minimum derating factor of 10% is assumed, the maximum V_{DS} should range between 540V to 560V. As a general rule, 600–650V MOSFETs are recommended for the primary-side power device in 10W applications for cost purposes. For the design example, a 650V MOSFET is chosen.

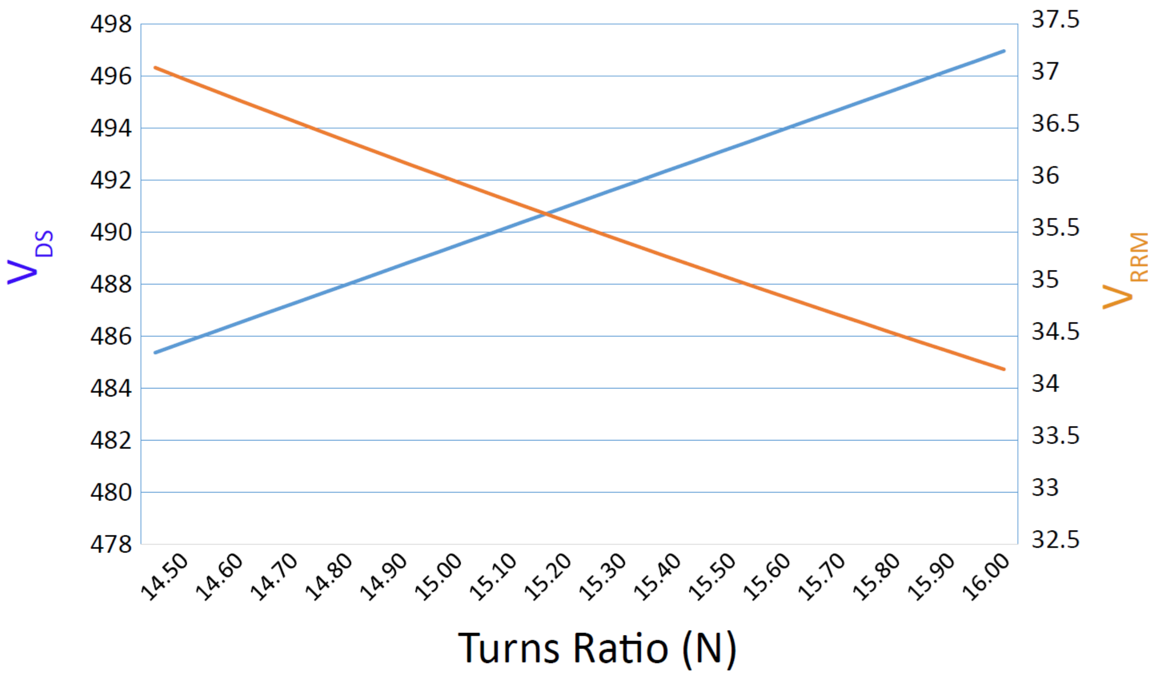


Figure 3. Stress Voltages Across Components vs Turns Ratio

The secondary-side rectifier voltage also needs to be derated similar to the voltage on the primary-side MOSFET.

The derating factor recommended is 10% minimum and similar to the MOSFET selection process, this derating factor may vary from design to design. According to Figure 3, the voltage rating for the secondary-side rectifier needs to be between 40V and 45V for safest operation. Whether the secondary-side rectifier is a Schottky diode or a synchronous rectifier, the voltage rating needs to be the same minimum value. For the design example, a 40V MOSFET is selected.

This same exercise can be done for each output voltage when using the iW1702 for higher output voltages.

MOSFET selection for the primary-side drive needs careful consideration. The minimum voltage rating is already set at 650V. The rest of the key specifications, aside from cost, are $R_{DS(ON)}$, threshold voltage and parasitic capacitances. First, the threshold voltage of the MOSFET should be less than the UVLO threshold shown in Table 2. This ensures proper turn-on of the MOSFET during operation. The peak current is less than 1A for typical low voltage applications, so the key is balancing the resistive losses with the switching losses. This is particularly important for low power mode. A recommended range for $R_{DS(ON)}$ is between 0.6ν and 1.0ν. There are multiple MOSFET manufacturers for these types of devices. For the design example, a device from the IPD65R650 series of FETs from Infineon, or equivalent device, is selected.

For the secondary-side rectifier, the deciding factor between a Schottky diode rectifier and a synchronous MOSFET is cost vs. efficiency. As a general rule, above 2A of output current, the SR controller and FET tend to be used to reduce I^2R losses (or V_{FD} *I loss in the Schottky diode). For the 10W design example, a > 45V rated MOSFET with sub-20mν on-resistance is recommended for optimal trade-off between cost/performance.

The MOSFET selected for the secondary-side rectifier to be used with the iW673 or iW676 controller is generally chosen based on the voltage rated calculated above and the $R_{DS(ON)}$ needed for efficiency. The lower the RDS(ON), the higher the cost, so the choice of SR FET can be determined based on the key design parameters, cost or performance. As a general rule, for sub-3A applications, it is recommended to stay below 20mν and 3A or higher should stay below 15mν, but again this is highly subjective and depends upon the application needs vs cost.

Renesas offers two SR controllers that are functional equivalents but have slightly different feature sets that make them both compatible with the iW1602/iW1702 but are used in different situations. The iW676 has a higher voltage rating which makes it better suited for higher output voltages and it also offers options with active voltage positioning, making it ideal for when the iW1602/1702 are used in LOM2 for lowest no-load power consumption. The iW673 is ideal for lower output voltage applications where the iW1602/iW1702 is used in LOM1/3/4 mode. For more details, refer to the iW673, iW676 datasheets. For the design example, the iW673 is selected.

6. Sense Resistor (R_{ISNS})

The sense resistor value is calculated using Equation 8.

$$R_{ISNS} = \frac{k_{CC} \times N \times \eta_{TX}}{2 \times I_{OUT}} \qquad \textbf{Eq. 8}$$

By initially calculating the sense resistor value, we can begin selecting the rest of the components. The turns ratio selected above is 15 for the design example. The iW1602/iW1702 uses a constant-current mode of current limiting to facilitate the design of power adapters for charging applications. Since the R_{ISNS} value determines the knee point for the constant-current mode, it is recommended to add between 10–20% margin to ensure that the adapter can provide the maximum nominal current required under worst case conditions without entering current limit. For the purpose of the design example, a 20% adder to the nominal 2A design example current is set. Calculating for R_{ISNS} using Equation 9 gives the following.

$$R_{ISNS} = \frac{0.422 \times 15 \times 0.95}{2 \times 2.4\text{A}} = 1.253\Omega \qquad \textbf{Eq. 9}$$

The nearest 1% value is 1.260ν, so this is used for the design example. The sense resistor handles high peak currents and it is important to size this resistor properly to handle the necessary power dissipation. The primary-side peak current is defined in Equation 10.

$$I_{PRI(PK)} = \frac{V_{IPK}}{R_{ISNS}} \qquad \textbf{Eq. 10}$$

V_{IPK} is the I_{PEAK} comparator threshold voltage used for peak current mode control, which is dynamically adjusted by the internal digital controller to maintain the desired regulation. Its upper control limit is 1V (VIPK_HI) and lower limit is variable (V_{IPK_LO}). The lower limit depends upon the LOM mode of operation. If the LOM2 mode is selected for lowest no-load power, then 0.28V is used for the V_{IPK_LO} value. Otherwise, the V_{IPK_LO} value used for design is 0.125V. The real V_{IPK_LO} value will be slightly different from the design target due to the turn-on and turn-off MOSFET delay times. These variables depend highly on the parasitic characteristics of the MOSFET and will also impact EMI, therefore it is recommended to measure the reset time and no-load power and adjust the V_{IPK_LO} value and re-calculate the rest of the magnetics characteristics to optimize the design.

For the design example, 75mW max no-load power consumption is desired, so LOM1 is selected (2kHz min DDPWM frequency). For more details on LOM operation, refer to the datasheet.

The V_{IPK_HI} value of 1V is the design limit, but it is recommended to use a lower value. This allows for transient response peak currents, tolerances in the manufactured inductance, and improved efficiency by reducing peak primary currents. The recommended design value (V_{IPK_FL}) at maximum L_M and at full load is between 0.5V–0.9V. The recommend starting point is between 0.7V–0.8V, with 0.75V used for the design example. A small compensation value is added and used in this equation, 20mV. The V_{IPK} value of 0.75V may need to be adjusted based on the L_M calculations in the next section.

$$I_{PRI(PK)} = \frac{0.7\text{V} + 0.02\text{V}}{1.260\Omega} = 0.571\text{A}$$ **Eq. 11**

The peak current on the primary is important in calculating the magnetizing inductance, as shown in section 9. The RMS current is necessary to calculate the power dissipation in the sense resistor and is calculated by Equation 12.

$$I_{PRI(RMS)} = \frac{2 \times P_{IN\_MAX}}{V_{IN\_DC\_MIN} \times \sqrt{3} \times \sqrt{D_{ON\_MAX}}}$$ **Eq. 12**

The P_{IN_MAX} term is defined as the output voltage (including the CDC voltage) and I_{OUT_CC} divided by the target efficiency of 90%. There is a term in this equation, D_{ON_MAX}, which defines the maximum on-time of the main switch relative to the total switching period. This number can be approximated to 0.4 for this DCM flyback converter as the actual value will not vary much from this number and doesn't make a significant impact to the power dissipation calculation.

$$I_{PRI(RMS)} = \frac{2 \times 13.73\text{W}}{127.3\text{V} \times \sqrt{3} \times \sqrt{0.40}} = 0.197\text{A}$$ **Eq. 13**

The power dissipation in the sense resistor is calculated very simply using Equation 14.

$$P_{RISNS} = R_{ISNS} \times I_{RMS}^2$$ **Eq. 14**

$$P_{RISNS} = 1.260\Omega \times 0.197\text{A}^2 = 0.049\text{W}$$ **Eq. 15**

The power dissipation required by the sense resistor needs to be considered at maximum ambient temperature to properly select the size and number of resistors needed for the application. Resistor manufacturers recommend derating the power dissipation capability of surface mount resistors above 70ºC ambient temperature. The application requires 50mW of power dissipation, so the first step is to review the derated power dissipation capability of surface mount resistors to properly select the resistor size for the application. Most derating curves are similar but check with the manufacturer to confirm the derating curve for the chosen resistor supplier. For the design example, 0805 resistors can dissipate 0.25W max at room temperature. With derating, at 85ºC, this same resistor can dissipate 0.182W of power, enough to satisfy the application requirements.

Once the turns ratio has been chosen and the sense resistor calculated, the rest of the magnetics characteristics need to be determined. We'll start by calculating some of the fundamental voltages and currents and then design the transformer windings based on these calculations.

7. Magnetizing Inductance (L_M)

With the sense resistor calculated, the turns ratio tentatively set and the primary-side peak current also established, the next step is to estimate the required magnetizing inductance for the primary side of the transformer.

The magnetizing inductance needs to be within a set range to maintain DCM operation and once set, the number of windings can be selected using the maximum allowed flux density (see section 8). Calculations for the minimum and maximum potential magnetizing inductances need to be made and then an operating range for the magnetizing inductance selected. Based on the tolerance of that range of inductance, it may be necessary to go back and modify the selected V_{IPK_FL} value as mentioned in section 6. One additional value needs to be calculated and that is the maximum transformer power (P_{XFMR_MAX}). This is the output power at max output current (I_{CC_OUT}) divided by the transformer efficiency (95% per Table 3).

$$L_{M\_MIN0} = \frac{N \times (V_{OUT} + V_{FD}) \times T_{RST\_MIN} \times R_{ISNS}}{V_{IPK\_LO}} \qquad \textbf{Eq. 16}$$

$$L_{M\_MIN1} = \frac{2 \times P_{XFMR\_MAX}}{f_{SW\_MIN} \times 0.95 \times \left(\frac{V_{IPK\_HI}}{R_{ISNS}}\right)^2} \qquad \textbf{Eq. 17}$$

Equation 16 shows the calculation for minimum required magnetizing inductance during the minimum reset time and Equation 17 shows the minimum required value during normal operation. Of these two values, the highest is selected as the minimum desired inductance value. As explained in section 6, the V_{IPK_LO} value is either 0.28 (LOM2) or 0.125 (LOM1/2/4). Since LOM1 is selected for the design to fulfill the 75mW no-load power consumption requirement, the V_{IPK_LO} value is set to 0.125V and the min magnetizing inductance values can be calculated.

The next step is to calculate the maximum magnetizing inductance.

$$L_{M\_MAX0} = \frac{2 \times P_{XFMR\_MAX}}{f_{SW\_MAX} \times \left(\frac{V_{IPK\_FL} + 20\text{mV}}{R_{ISNS}}\right)^2} \qquad \textbf{Eq. 18}$$

$$L_{M\_MAX1} = \frac{(0.9 \times \sqrt{2} \times V_{IN\_AC\_MIN} - 2) \times 1.8\text{x}10^{-6}}{(0.18/R_{ISNS}) \times 1000} \qquad \textbf{Eq. 19}$$

For the range of inductances, we select the lowest of the maximum inductances and the highest of the minimum inductances. For the design example, these calculate to a range of 0.793mH to 0.902mH for the design. The tolerance for this is about 6%, which is tight, but within a manufacturable range for a transformer. If the tolerance is tighter than a manufacturable range, typically 5%, then the V_{IPK_FL} value needs to be increased (50mV increments) and the values re-calculated. The LM value for the design example is set at 0.85mH, the center of the calculated range of inductances.

8. Primary and Secondary Turns (NPRI and NSEC)

The equation for setting the minimum number of primary-side turns for the transformer is shown in Equation 20. Several variables in Equation 20 have been set in sections 5, 6, and 7, but a magnetic core still needs to be set. The magnetic core center-leg cross-sectional area A_e determines the energy storage and is inversely proportional to the required number of turns. Equation 20 shows the relationship between the number of turns and the area. In order to set the minimum number of primary turns, a core size has to be selected for the transformer. For the design example, it is best to start with a more conservative approach and adjust later if desired. Table 6 shows a small selection of cores and their corresponding A_e. For the design example, the EE20/10/6 core with an A_e of 32mm^2 is selected.

Table 6. Magnetic Core Material Characteristics (TDK)

Core	A_e(mm^2)		Core	A_e(mm^2)
PC40/44 - B_{SAT} = 0.39T at 100ºC				
EE10/11	12		RM4	14
EE13	16		RM5	23.7
EE16	19.2		RM6	36.6
EE20/10/6 (EF20)	32		RM8	64

Maximum flux density should always be determined at the highest desired temperature (maximum ambient temperature plus maximum temperature rise due to power dissipation). This will be the worst case scenario for potential saturation and that is the condition to which the transformer must be designed.

The desired maximum operating flux density for the transformer design is highly subjective. Some applications where cost drives the design objectives can choose to set a maximum flux density near the saturation level with the understanding that this will be less efficient (higher copper and core losses) while providing a smaller, lower cost transformer design. Setting a lower allowable B_{MAX} value gives better efficiency and safety at the expense of a slightly higher cost transformer. The difference in cost comes from either using a larger bobbin to get a larger cross-sectional area and subsequently a high saturation rating or by using more turns on the primary.

For high reliability applications, it is recommended to use a conservative B_{MAX} value that is 15%–25% below the saturation value. The flux density value is considered at maximum transformer temperature, as discussed previously, due to the negative temperature coefficient of flux density in ferrite cores.

Max flux density needs to be calculated under the worst case condition for current through the primary since the B_{MAX} level is achieved at peak primary current. The maximum voltage sense value (V_{IPK_HI}) is the level at which current through the primary side of the transformer will reach its peak and that value is what should be used at B_{MAX} in order to calculate the maximum number of turns. The V_{IPK_HI} level for these products is 1V.

The B_{SAT} value for the core selected is 0.390T at 100ºC, and to be conservative, we will use 85% of that value in order to ensure that the transformer never enters saturation. That gives a B_{MAX} value of 0.332T, which can be rounded to 0.33T for the design example.

Using the cross-sectional area from Table 6 for the EE20/10/6 core, we can calculate the minimum number of turns required on the primary. The equations used are as follows.

$$N_{PRI} > \frac{L_M}{R_{ISNS}} \times \frac{V_{IPK\_HI}}{A_e \times B_{MAX}} \quad \textbf{Eq. 20}$$

$$N_{PRI} > \frac{0.850\text{mH}}{1.260\Omega} \times \frac{1\text{V}}{32\text{mm}^2 \times 0.33\text{T}} > 63.8 \quad \textbf{Eq. 21}$$

The number of windings on the primary side needs to exceed 63.8 turns to ensure proper operation. The nearest integer value is 64 turns and is set as the number of primary-side turns.

The previously chosen turns ratio of 15 is used to calculate the minimum number of secondary-side windings.

$$N_{SEC} = \frac{N_{PRI}}{N} \quad \textbf{Eq. 22}$$

For the design example with 64 primary-side turns, the number of required secondary-side turns is 4.3 and the nearest integer value is 5. The new turns ratio for the design example is 12.8. It is good practice to check Figure 2 to make sure that with the new, higher turns ratio, the voltages are still within the desired range. The primary-side FET voltage will go down with this new turns ratio, but the secondary-side rectifier will go up quite a bit. Since Equations 20 and 21 give the minimum required turns, the number of primary turns can be increased to bring down the secondary-side voltage. For the design example, 72 primary-side turns and 5 secondary turns for a turns ratio of 14.4 are chosen.

While the selection criteria for the core size/shape and bobbin type are beyond the scope of this document, one fundamental check needs to be done at this point. Based on the winding area available for the core/bobbin selected, and the gauge of wire required for the primary-side currents, it is important to determine if the primary-side turns will fit in the area available. Also, a quick copper/core loss calculation can be made to determine if the proper core size has been selected.

9. Auxiliary Sense Winding (NAUX)

The primary-side controller obtains information about the secondary from the auxiliary winding of the transformer and care needs to be taken in determining the correct number of auxiliary windings. The controller needs a V_{CC} operating voltage in the range of 6.5V and 20V for proper operation. Best design practice is to set the number of auxiliary windings to keep the V_{CC} voltage out of UVLO. Equation 23 shows the basic calculation for determining the required number of turns for the auxiliary winding.

$$N_{AUX} = \frac{N_{SEC} \times V_{AUX}}{V_{SEC}} \quad \textbf{Eq. 23}$$

N_{AUX} is the number of auxiliary windings, V_{AUX} is the voltage at the auxiliary winding and the V_{SEC} voltage is the output of the secondary, before the rectifying diode. The worst case scenario for the minimum V_{CC} voltage is at no-load, and the V_{AUX} voltage is the V_{CC} voltage plus the V_{AUX} diode and series resistor voltage drop (1–2V). The CDC voltage is 0V at no-load.

$$V_{SEC} = V_{OUT} + V_{FD} + V_{CDC} \quad \textbf{Eq. 24}$$

$$V_{SEC} = 5\text{V} + 0.5\text{V} + 0.15\text{V} = 5.65\text{V} \quad \textbf{Eq. 25}$$

For the design example, V_{AUX} is 8.5V (6.5V + 2V) and the V_{SEC} is simply the output voltage because the forward voltage drop across the synchronous rectifier is zero volts and the CDC voltage at no-load is also zero. Therefore, the number of turns in the auxiliary winding is determined as follows.

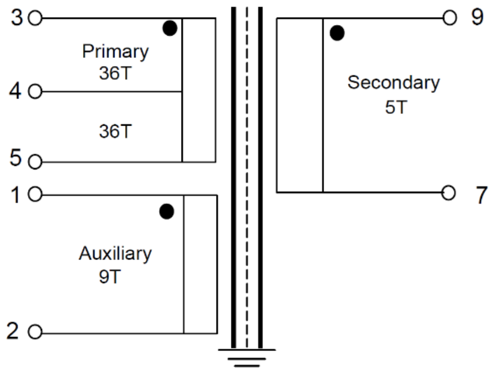
$$N_{AUX} = \frac{5 \times 8.5\text{V}}{5\text{V}} = 8.5 \quad \textbf{Eq. 26}$$

Rounding to the nearest integer value, 9 turns are selected for the auxiliary winding. It is good practice to keep the number of auxiliary winding turns to a minimum due to imperfect coupling between windings on the transformer could cause higher than expected voltage at max output load.

10. Final Magnetics Specification

Now that all the key characteristics of the magnetics have been determined, the final specification can be shown. Aspects of the magnets design, such as shielding for EMI purposes, are beyond the scope of this document.

Table 7. Transformer Design Specifications

Transformer Specifications	
Schematic	
	
Electrical Specifications	
1.	Primary inductance (L_M) = 0.85mH at 10KHz
2.	Electrical strength = 3kV, 50/60Hz, 1 Min.
Materials	
1.	Core: EE20/10/6 (EF20) (Ferrite material TDK PC40 or equivalent)
2.	Bobbin: EF20/10/6 horizontal
3.	Magnet wires (pri): type 2-UEW
4.	Magnet wire (sec): triple insulated wires
5.	Layer insulation tape: 3M1298 or equivalent

11. Snubber Design

When the primary-side FET is turned off, the voltage on the DRAIN of the FET will quickly rise up beyond the input voltage and will ring due to the parasitic elements of the transformer. The primary-side winding needs a circuit to clamp the excess flyback voltage in order to protect the main MOSFET. A snubber circuit is used to absorb the excess energy of the leakage inductance after the main switch is closed. This leakage inductance is the main contributor to the peak voltage and needs to be known to design a proper snubber circuit. A simple RCD type snubber circuit as shown in Figure 2 is usually sufficient for most flyback converter designs, although the topic of snubber circuit topologies and design is quite broad and is beyond the scope of this design document. There are many design resources available in the industry that can be consulted for snubber design. See the References section for a recommended snubber paper that discusses the basic principles to take into consideration.

12. V_{SENSE} Voltage Feedback Resistors

The V_{SENSE} pin monitors the same auxiliary winding that powers the IC via the V_{CC} pin and uses that information for the main feedback control signal. The feedback signal, V_{SENSE}, is sensed at the end of the T_{RST} time when the current in the rectifying diode is near zero. The design output voltage is set by the following equation.

$$V_{OUT} = \frac{N_{SEC}}{N_{AUX}} \times \left[\left(1 + \frac{R_1}{R_2}\right) \times V_{SENSE}\right] - V_{FD} \qquad \textbf{Eq. 27}$$

The VSENSE voltage under normal constant voltage feedback is 1.536V. The feedback resistors R1 and R2 are shown with their correct implementation in Figure 2. The forward voltage drop in the output diode (V_{FD}) is the voltage at zero forward current, typically around 0.2V for most Schottky diodes.

Solving for R1/R2 for the design example gives the following ratio:

$$\frac{R_1}{R_2} = \frac{N_{AUX}}{N_{SEC}} \times \frac{V_{OUT} + V_{FD}}{V_{SENSE}} - 1 \qquad \textbf{Eq. 28}$$

$$\frac{R_1}{R_2} = \frac{9}{5} \times \frac{5\text{V} + 0\text{V}}{1.536\text{V}} - 1 = 4.86 \qquad \textbf{Eq. 29}$$

The value of R_1 needs to be a minimum value in order to limit the current into the controller under high input voltage (V_{AC}) conditions. For AC input voltage up to $264V_{AC}$, the ratio of auxiliary-to-primary windings multiplied by 125kν gives the minimum resistor value for R_1 (for input voltages higher than $265V_{AC}$, contact your local Renesas FAE). For the design example, the required size is >15.6kν. Using standard 1% resistors, R_1 is set to 17.8kν and R2 is 3.65kν.

13. Start-Up Resistors

The iW1602/iW1702 has a multi-stage start-up profile as defined in section 9.2 of the datasheets. The start-up resistors needs to be connected directly to the V_{CC} pin to provide the charging current. The start-up resistors are chosen based on desired start-up time (dominated by RC time constant of C_{VCC} and R_{VIN}), input voltage and current drawn by the V_{CC} pin.

$$T_{START} = \frac{C_{VCC} \times V_{CC\_ST}}{\frac{V_{IN\_AC\_MIN} \times \sqrt{2}}{R_{VIN}} - I_{CC\_ST}} \qquad \textbf{Eq. 30}$$

Equation 30 shows a first-order estimate of the start-up time calculation at minimum supply voltage, which is the worst case condition. Due to parasitics and other factors that may affect turn-on time, it is important to verify on the bench for applications with critical turn-on time requirements. For the V_{CC} pin, normally a bulk capacitor is used and most applications use ceramic capacitors for this node. Ceramic capacitors have a voltage bias factor that is important to consider. For example, a 25V, X7R ceramic capacitor can lose 20% of its capacitance at 12V applied voltage. Therefore, the C_{VCC} value used to calculate the start-up time should use a lower value when ceramic capacitors are used, or when any capacitor that has a voltage bias component is used.

For the V_{CC} capacitor, a minimum value of 2.2µF is recommended for most designs. Along with the bulk capacitance, a high frequency 0.1µF capacitor in parallel is recommended to reduce high frequency noise. For this design, a 4.7µF bulk capacitor is used. For a desired start-up time of 3s, the R_{VIN} calculates to 4.256Mν.

For safety in a universal-input design, it is necessary to split the needed start-up resistance into two series values of half the total resistance each. This is because 1206-sized surface mount resistors are only rated for 200V–250V across their package body. The peak input voltage is 375V, so a single resistor can not meet the requirement unless an appropriate conformal coating is applied. For the design example, two 2.128Mν resistors in series are required. Using standard 1% values, two 2.1Mν resistors are selected.

14. Pre-Load Resistor (No Load)

For proper regulation under no-load conditions, the power supply circuit will require a pre-load resistor. This value needs to be small enough to keep the output voltage regulating properly but not too large to impact no-load power consumption. The LOM (light-load operating mode) described in detail in the datasheet offers the ability to select between four different minimum operating frequencies. The higher the minimum operating frequency set by the LOM resistor (R_{FS}), the higher the no-load power consumption value. The pre-load resistor is inversely proportional to this value. If the device is operating at a higher minimum frequency, then the output requires a smaller no-load resistor.

As described in the datasheet, the higher the minimum frequency, the faster the output will respond to sudden load changes. At the lowest setting, LOM2, an active voltage positioning option of the SR controller (iW676-3x) is recommended on the output to improve dynamic load response (DLR) during light load mode.

Equation 31 shows the fundamental relationship between the no-load power consumption and the output pre-load resistor. If the pre-load resistor is too small, the excess energy stored in the transformer will cause the output voltage to increase.

$$R_{PRE} = \frac{V_{OUT}^{2}}{P_{IN\_NL}} \qquad \textbf{Eq. 31}$$

The P_{IN_NL} term needs to be calculated based on the previously selected values for LM, RISNS and some constants specific to the controller selected. Equation 32 shows the input power at no-load for a specific LOM frequency (f_{SW_DDPWM}).

$$P_{IN\_NL} = 0.5 \times L_M \times \left(\frac{V_{IPK\_NL}}{R_{SNS}} \right)^2 \times f_{SW\_DDPWM} \qquad \textbf{Eq. 32}$$

The V_{IPK_NL} term in Equation 32 is set at 0.18V for these controllers.

For the design example, we chose LOM1, which from table 9.1 in the iW1602 datasheet gives a f_{SW_DDPWM} frequency of 2kHz. As a side note, there is no recommended value for f_{SW_DDPWM} for LOM2. In this case, it is recommended to use 200Hz to calculate the minimum pre-load resistor value. Therefore, the P_{IN_NL} value calculates to 19.8mW. Finally, using Equation 31, the resistor value is determined to be 1.26kν. In order to absolutely guarantee that there will be no regulation issues under true no-load conditions, some derating is recommended without the value going below 1kν. For the design example, 1kν is selected as the pre-load value.

15. Input Capacitance

The input capacitor holds up the supply voltage to the converter during the low-voltage portion of the AC-cycle. The appropriate amount of input capacitance must be used to prevent undervoltage conditions on the input. A conservative approach is to use 2–3μF/W of output power for a universal input power supply. A detailed analysis of the voltage at the bulk capacitance can help determine a more precise amount of capacitance required for the application.

Equation 33 shows the relationship between the input capacitor and the minimum DC input voltage. This equation is a fairly accurate first-order estimate that is based upon the amount of energy required to maintain the DC voltage above a minimum value required for the design. Two equations, one that calculates the energy stored in the bulk input capacitance and a second that determines the energy discharged from the bulk capacitance, are defined and equated to solve for the bulk capacitance value. By knowing what minimum input voltage is required by the application, the minimum amount of bulk capacitance can be calculated by Equation 33.

$$C_{BULK} = \frac{2 \times P_{IN} \times \left[0.25 \times \sin^{-1}\left(\frac{V_{IN\_DC\_MIN}}{\sqrt{2} \times V_{IN\_AC\_MIN}} \right) / 2\pi \right]}{\left(\sqrt{2} \times V_{IN\_AC\_MIN}\right)^2 - V_{IN\_DC\_MIN}^{\ 2} \times f_{LINE}} \qquad \textbf{Eq. 33}$$

The bulk capacitor discharges as a function of the current drawn from the capacitor. The assumption of a constant maximum load is made in order to calculate the worst case capacitance required. In this case, the load on the capacitor is actually a constant power load, or a changing current as the voltage decreases, causing the discharge characteristic of the bulk capacitor to be non-linear. Equation 33 takes into account this non-linearity but is an approximation more than an exact calculation. It is recommended to increase the amount of calculated capacitance by 5–10% to allow for the small error in the calculation.

Figure 4 shows a graphical representation of the input voltage for the design example. Each curve represents a different bulk input capacitance value on the resulting minimum DC input voltage (indicated by the dashed line). The minimum input voltage recommended for a home appliance application is 100V and this corresponds to a minimum input capacitance value of approximately 35µF. For travel adapter applications, the minimum voltage can be allowed to drop to a lower level to reduce the BOM cost by using a smaller input capacitor. For a minimum input voltage between 80V and 90V, a 22µF input capacitor can be used. For 100V, a minimum of 33–47µF is recommended.

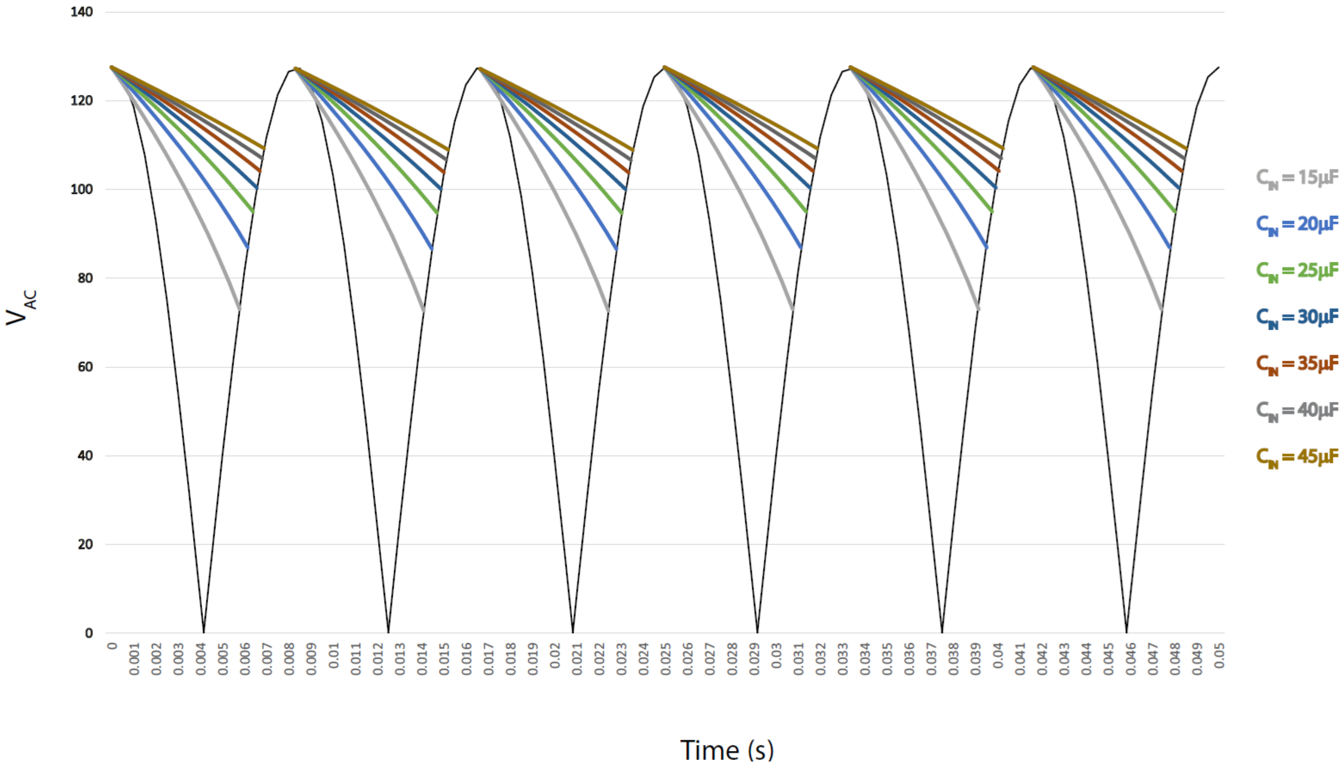


Figure 4. Input Voltage vs Bulk Input Capacitance

The proper selection of the input capacitor needs to consider the ripple current on the capacitor and the ESR of the capacitor to ensure that the capacitor self-heating is minimized. Electrolytic capacitors running at high temperatures for long periods of time show a faster decrease in capacity compared to the same capacitor operating at lower temperatures, so understanding the impact of ESR is important to the expected lifetime of the design.

The ripple current through the input capacitor is calculated using Equation 34. This is an approximation as the ripple current will be lower due to the nature of a charging/discharging capacitor:

$$\Delta I = C_{IN} \times \frac{\Delta V}{\Delta T} \quad \textbf{Eq. 34}$$

The ripple current rating of the capacitor must be able to handle this ripple current to ensure safe operation over the life of the capacitor. Most capacitor manufacturers rate the ripple current at 120Hz and that ripple current rating increases as the ripple frequency increases.

$$P_{DISS} = I_{RIPPLE}^{2} \times Z_{CIN} \quad \textbf{Eq. 35}$$

The power dissipation of the input capacitor depends upon the impedance at the line frequency. This characteristic depends upon the specific capacitor selected for the application. It is important to consider the power dissipation caused by the ripple current due to the fact that the useful life of an electrolytic capacitor reduces by half for every 10°C rise above 25°C. Reduce ripple current by increasing the value of the capacitor or by using high-quality, low-ESR electrolytic capacitors.

16. Output Capacitor

The output capacitor needs to hold up the output and provide energy to the load. The amount of output capacitance is highly subjective and depends upon the type of capacitor used (high ESR vs low ESR, etc.) which will determine how much capacitance is needed. As a rule of thumb, a minimum of 330µF is recommended for 10W applications.

17. PCB Layout

The PCB layout needs to be done with care in order to help maintain good EMI and overall noise performance. As a general rule, all loops and traces should be as short as possible. There are some additional guidelines that should be followed to get the best possible performance out of the power supply design.

1. Keep all power paths as short as possible and avoid sharp corners when routing the power traces. Use thick traces as well to reduce the impedance of the path.
2. All loops should be isolated/separated from each other whenever possible. If it is not possible to completely isolate all loops, the amount of crossover should be minimized. It is important that the power traces do not overlap with signal traces where noise can capacitively couple into the signal paths.
3. The V_{SENSE} and V_{CC} loops should be kept as far from the power paths as possible to ensure the highest signal integrity of the feedback and supply voltage to the controller. Avoid crossover of these signal traces with power traces when ever possible. While complying with this rule, it is still important to keep these loops as short as possible.
4. Use a star-connection for ground to avoid any ground noise or ground bounce caused by stray impedance between the ground traces.
5. Minimize the trace lengths of all current paths that have high *di/dts* or high *dv/dts*. This includes the drain pin of the main power switch and the transformer primary winding. This helps improve EMI performance.

6. All decoupling capacitors should be placed as close to the IC as possible. Of primary concern is the V_{CC} capacitor. The V_{CC} decoupling capacitor needs to be as close to the IC as possible. The auxiliary winding provides the power to V_{CC} and if a bulk hold up capacitor is used, it should be connected first after the winding and the decoupling capacitor second, with the decoupling capacitor being as close to the IC as possible.

Additional areas of concern when designing the layout of a power supply are the current sense and voltage sense lines. It is important to route these lines as cleanly as possible to avoid noise injection on these signals. The R_{ISNS} resistor needs to be as close to the source of the external MOSFET to avoid any stray parasitics from adding noise on that line. The V_{SENSE} line needs to be as close to the transformer as possible to be able to detect the most accurate voltage from the transformer and improve the quality of the sensing signal. The bottom sense resistor, R2, should be as close as possible to the V_{SENSE} pin and GND. This helps reduce noise injection and improve overall noise immunity.

For circuits using a Schottky diode rectifier, keep the power loop between the secondary winding, the rectifier and the output capacitor a small as possible with short, thick copper traces as indicated in points 1–4. With the SR controller and MOSFET, the datasheets have detailed layout recommendations, but it is very important that the source of the synchronous MOSFET is directly connected to the SOURCE pin of the SR controller. The DRAIN pin must be connected as close to the drain of the synchronous MOSFET as possible. The voltage sensing loops must be minimized to reduce the coupling of noise.

Figure 5 shows a graphical representation of the above guidelines using the iW1602. Following the guidelines above, the connection between the primary winding of the transformer and the drain of the MOSFET is a high *dv/dt* path and should have minimum trace lengths and thick trace widths. The connection from the source of the MOSFET to the sense resistor and then the sense resistor to both ground and the I_{SENSE} pin also must be as short as possible. This will improve the accuracy of the current sense circuit and improve the overall performance of the power supply.

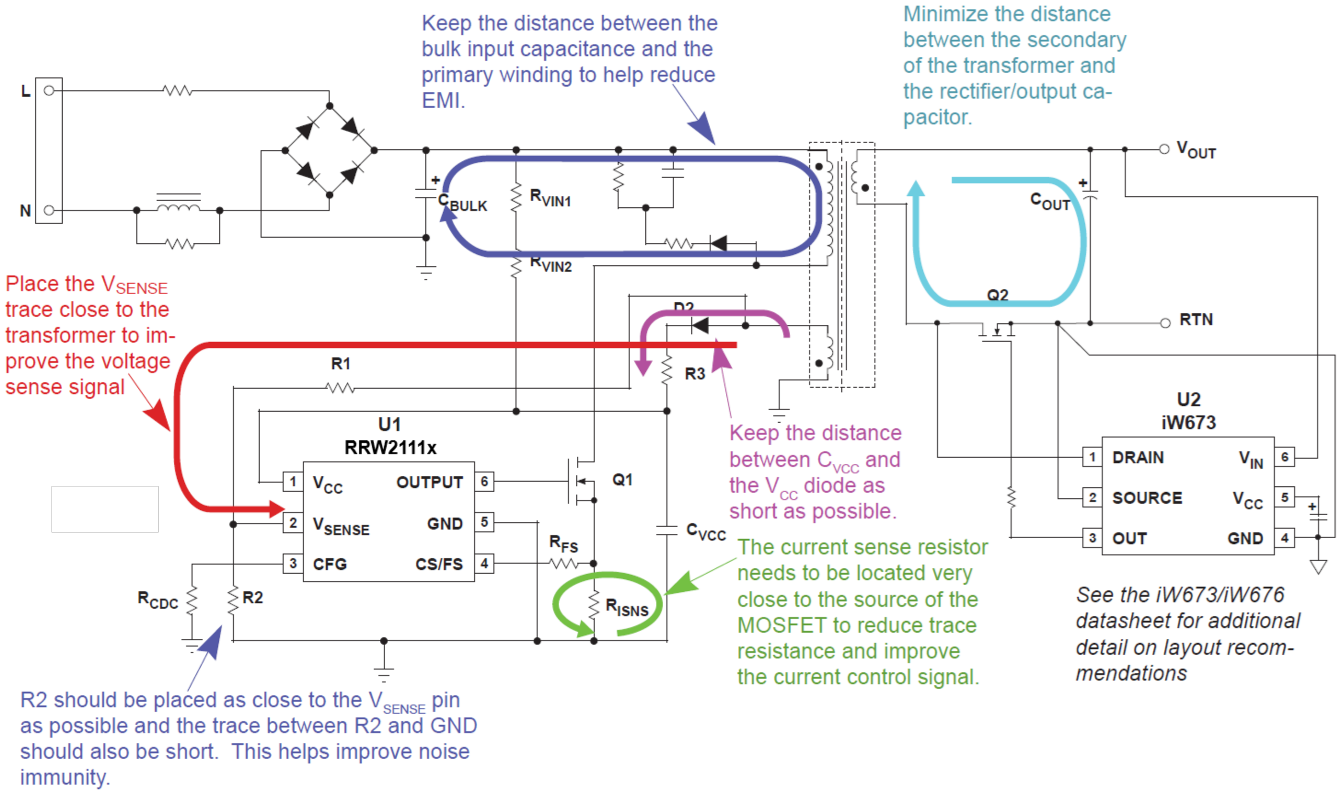


Figure 5. Schematic with Layout Recommendations

18. Design Summary

With the final components selected, the component values are shown in the table below.

Item	Ref	Part Description
1	R_{VIN1}, R_{VIN2}	2.1Mv, 1% – Start-up Resistors
2	R_{CDC}	4.02kv, 1% – Cable Drop Compensation Resistor
3	R1	17.8kv, 1% – Voltage Sense Resistor
4	R2	3.56kv, 1% – Voltage Sense Resistor
5	R_{ISNS}	1.260v, 1% Current Sense Resistor
5	R_{PRE}	1kv, 1% – Pre-load Resistor
6	R_{FS}	499v, 1% – LOM Setting Resistor
7	C_{OUT}	2 x 470μF, 25V e-Cap
8	C_{BULK}	47μF, 400V e-Cap
9	C_{VCC}	4.7μF, 25V 0805 X7R MLCC
10	D1	FR107 diode
11	D2	V10PL45 – Schottky rectifier diode
12	Q1	IPD70R600 – MOSFET: 700V, 0.6v
13	Q2	IRL60HS118 – MOSFET, 55V, 17mv

19. References

[1] iW1602, iW1702 Datasheets

[2] iW673, iW676 Datasheets

[3] Wurth DCM Flyback Transformer Cookbook

[4] Snubber Design Paper, Ridley Engineering

20. Revision History

Revision	Date	Description
1.00	Apr 8, 2026	Initial release.

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