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H8SX Family

IRQ Interrupts

Introduction

This application note describes setting up the $\overline{\text{IRQ}}$ pin functions.

Target Device

H8SX/1653

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1. Specification

Using the IRQ interrupts of the H8SX/1653 microcontroller requires selection of the input pin and edge that is sensed as the interrupt request, setting to enable the interrupt request, and so on.

This application note describes operation of the IRQ0 interrupt in interrupt control mode 0. The specifications are given below.

1. The P50 pin acts as the $\overline{\text{IRQ0}}$-B input pin.
2. IRQ0 interrupt requests are falling edges of the signal on the $\overline{\text{IRQ0}}$-B pin.
3. As is shown in figure 1, pin P20 has an initial value of zero and is toggled by IRQ0 interrupt processing.

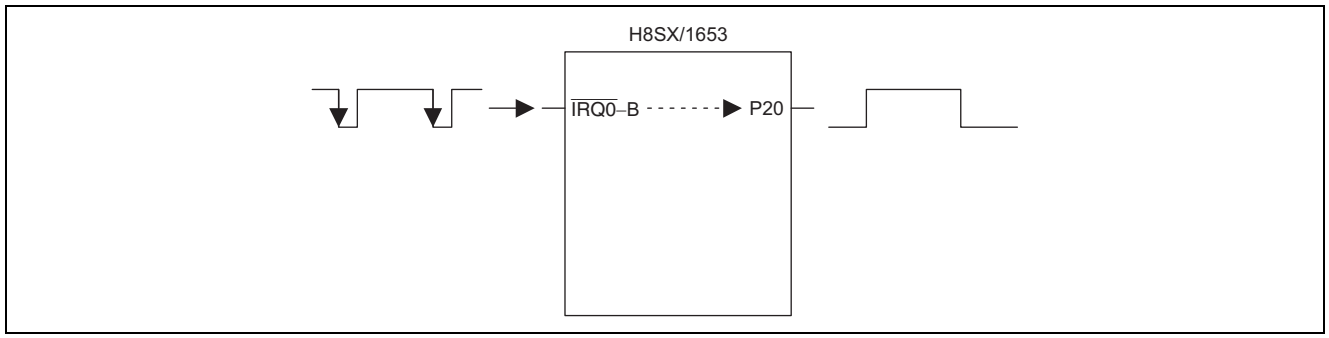


Figure 1 Operation of the Example for IRQ Interrupts

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating frequency	Input clock	: 16 MHz
	System clock (Iϕ)	: 32 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	: 32 MHz (input clock frequency × 2)*
	External bus clock (Bϕ)	: 32 MHz (input clock frequency × 2)
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0)	

Note: * USB module cannot be used with this frequency setting.

3. Description of Modules Used

3.1 IRQ Interrupts

An IRQ interrupt is an interrupt request generated by the signal on the corresponding $\overline{\text{IRQn}}$ (n = 11 to 0) pin. IRQn interrupts have the following features.

- The ISCR can be used to select whether each interrupt is generated by a low level, falling edge, rising edge, or both edges on the corresponding $\overline{\text{IRQn}}$ pin.
- The IER can be used to enable or disable each IRQn interrupt request.
- The IPR can be used to set the order of interrupt priority levels.
- The states of IRQn interrupt requests are indicated in the ISR. The flags in the ISR can be cleared to 0 by software. Use either bit-manipulation or memory-operation instructions to clear the flags.

Detection of IRQn interrupts is enabled through the P1ICR, P2ICR, and P5ICR register settings, and does not change regardless of the output setting. Accordingly, when a pin is in use as an external interrupt input pin, the corresponding DDR bit must not be cleared to 0 so that the pin can be used as an I/O pin for another function.

Figure 2 is a block diagram of the input logic for an IRQn interrupt.

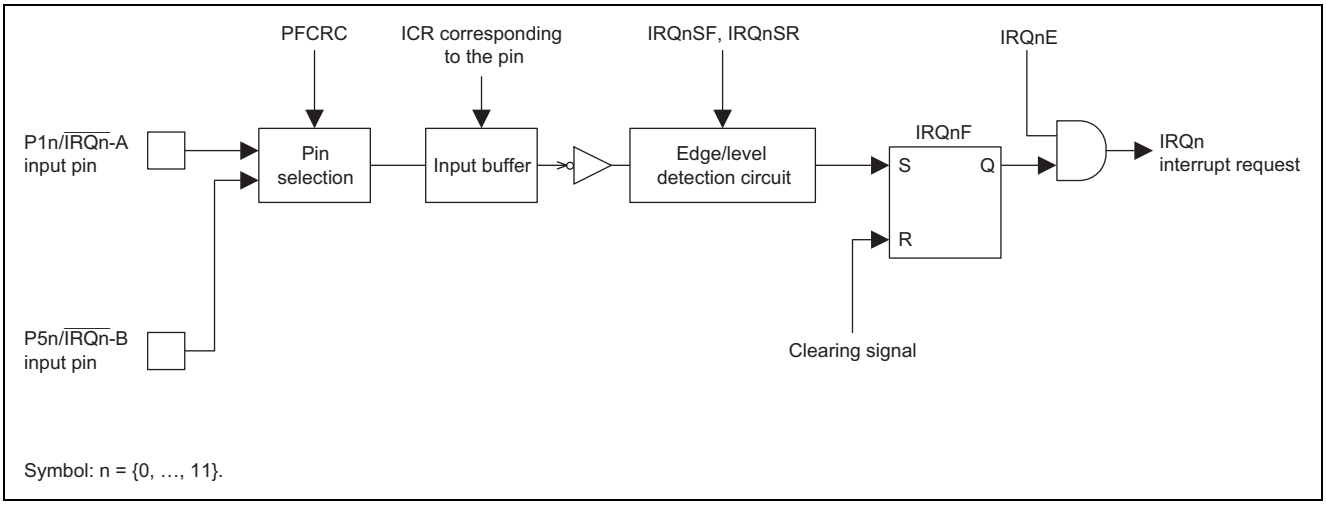


Figure 2 Block Diagram of the Input Logic for an IRQn Interrupt

When the IRQ sensing control in ISCR selects the low level of signal $\overline{\text{IRQn}}$, the level of $\overline{\text{IRQn}}$ should be held low until interrupt handling starts. Then set the corresponding $\overline{\text{IRQn}}$ input signal to high in the interrupt handling routine and clear the IRQnF to 0. The interrupt handler might not be executed if the corresponding $\overline{\text{IRQn}}$ input signal returns to the high level before the interrupt handling begins.

4. Principles of Operation

4.1 Flow in Outline

The operation of this example is summarized in the flowchart below.

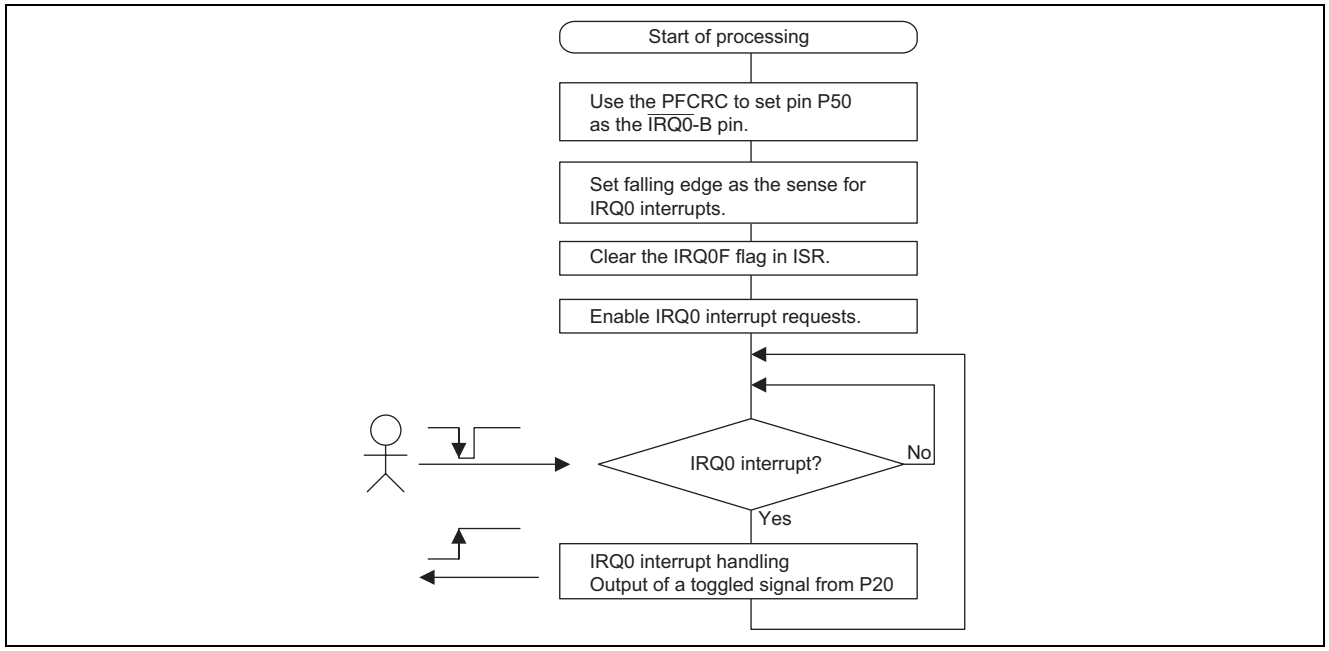


Figure 3 Outline of the Flow

4.2 Timing and Details of Processing

The timing of operations in this example is shown in figure 4. Explanations of software and hardware processing at the numbered points in the figure are given in table 2.

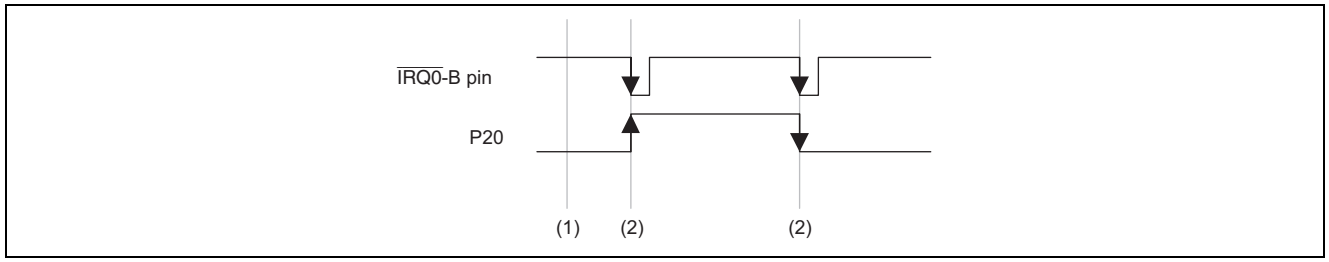


Figure 4 Example of the Timing of Operations in Interrupt Control Mode 2

Table 2 Details of Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial settings*
(2)	Set IRQ0F in ISR to 1.	IRQ0 interrupt handling a. Clear the IRQ0 interrupt flag (IRQ0F in ISR = 0). b. Toggle the output on pin P20.

Notes: * Initial settings
a. Enable the input buffer for pin P50 (the IRQ0-B pin).
b. Set the trigger for IRQ0 interrupts as falling edges on the IRQ0 input.
c. Set pin P50 as the IRQ0-B input pin.
d. Clear the IRQ0 interrupt flag (IRQ0F in ISR = 0).

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler, ver. 6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area

Table 5 Vector Table for Exception Processing

Exception Processing Source	Vector No.	Vector Address	Function to Interrupt Destination
Reset	0	H'000000	init
IRQ0	64	H'000100	irq0_int

5.2 List of Functions

Table 6 Functions in File main.c

Function Name	Function
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from the module stop mode, and calls the main function.
main	Main routine Makes interrupt settings and initializes interrupt IRQ0.
irq0_int	Interrupt handler for IRQ0 Toggles the signal on pin P20.

5.3 Description of Functions

5.3.1 Function init

1. Functional overview
   Initialization routine. (Releases the required modules from module stop mode, configures the clocks, and calls the main function.)
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. The latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by mode pins (MD2 to MD0; see table 7). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latching is released by a reset.
10	MDS2	Undefined*	R	
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD0 to MD3.

Table 7 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is provided to the CPU, DMAC, and DTC.
8	ICK0	1	R/W	001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB and MSTPCRC control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 releases the module from module stop state.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

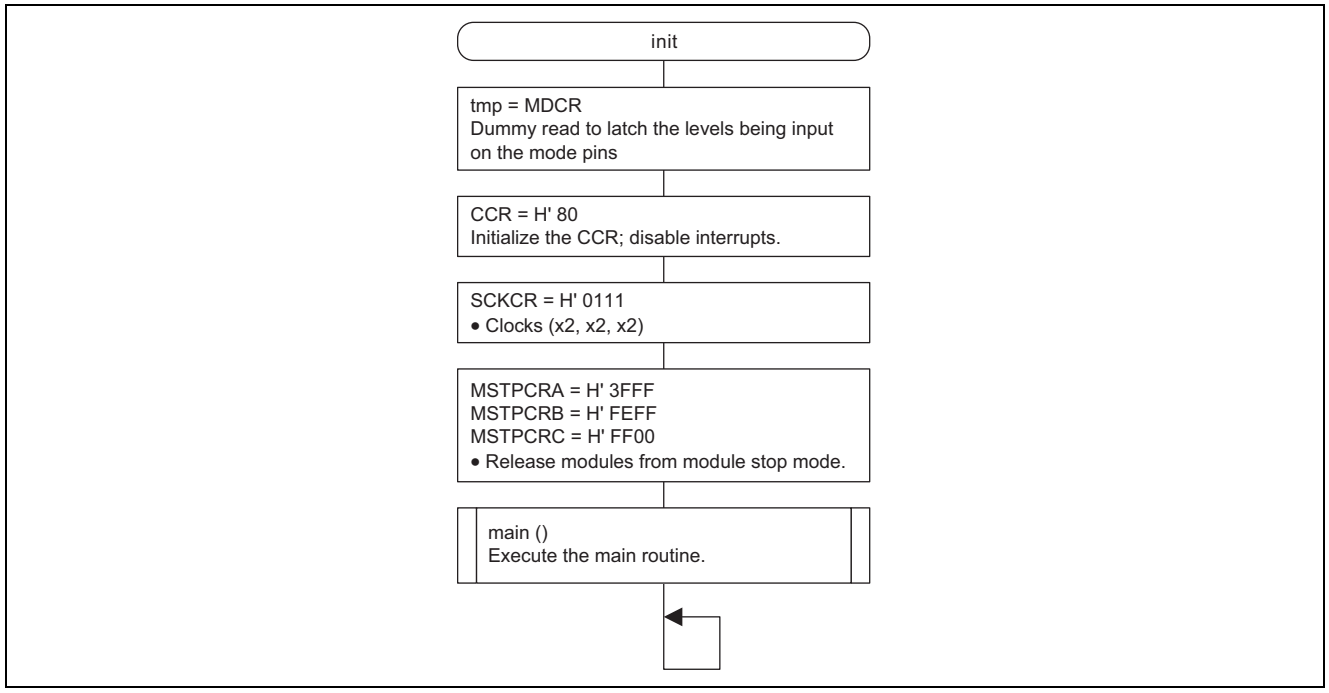
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface 0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.3.2 Function main

1. Functional overview
   Makes interrupt settings and initializes the IRQ0 interrupt.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 2 data direction register (P2DDR) Number of bits: 8 Address: H'FFFB81
  Function: P2DDR sets pin P20 as an output pin.
  Setting: H'01

- Port 5 input buffer control register (P5ICR) Number of bits: 8 Address: H'FFFB94

Bit	Bit Name	Setting	R/W	Description
0	P50ICR	1	R/W	0: Input buffer for pin P50 ($\overline{\text{IRQ0}}$-B) is disabled. 1: Input buffer for pin P50 ($\overline{\text{IRQ0}}$-B) is enabled.

- Port function control register C (PFCRC) Number of bits: 8 Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Description
0	ITS0	1	R/W	0: Selects pin P10 as the $\overline{\text{IRQ0}}$-A input 1: Selects pin P50 as the $\overline{\text{IRQ0}}$-B input

- IRQ sense control register L (ISCRL) Number of bits: 16 Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Description
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1	R/W	IRQ0 Sense Control Fall 01: The interrupt request is generated on falling edges of the IRQ0 input.

- IRQ enable register (IER) Number of bits: 16 Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Description
0	IRQ0E	0	R/W	IRQ0 Enable 0: IRQ0 interrupt requests are disabled. 1: IRQ0 interrupt requests are enabled.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

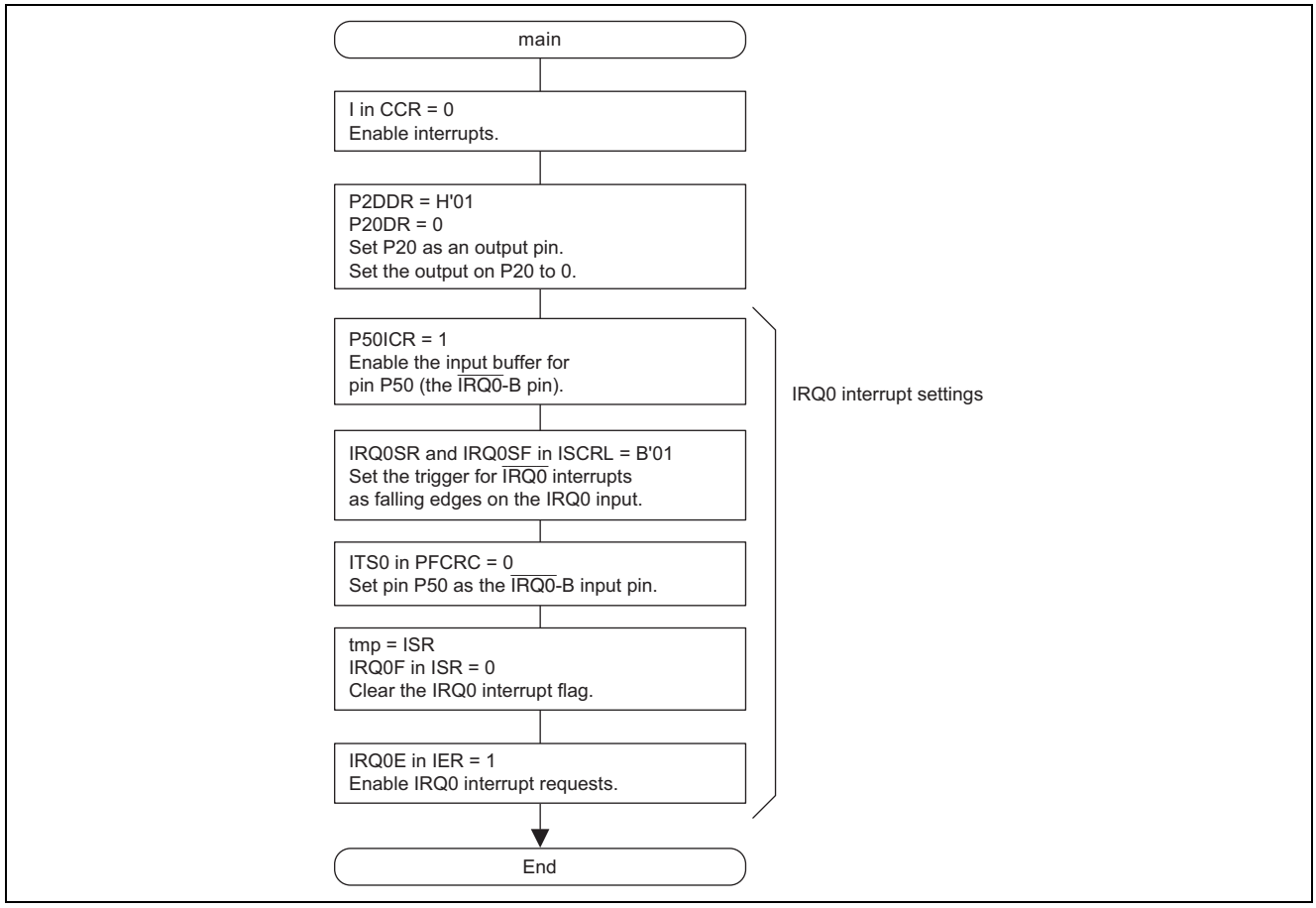
Bit	Bit Name	Setting	R/W	Description
0	IRQ0F	0	R/(W)*	[Setting condition] • Generation of an interrupt source selected in the ISCR [Clearing conditions] • Writing 0 to IRQ0F after having read it as 1 • Execution of interrupt exception handling while low-level sensing is selected and the $\overline{\text{IRQn}}$ input is high (n = 0, …, 11) • Execution of IRQn interrupt exception handling while falling-, rising-, or both-edge sensing is selected • Activation of the DTC by an IRQn interrupt when the DISEL bit in MRB of the DTC is cleared to 0

Note: * Only 0 can be written, to clear the flag.

- Port 2 data register (P2DR) Number of bits: 8 Address: H'FFFF51

Bit	Bit Name	Setting	R/W	Description
0	P20DR	0	R/W	0: Pin P20 is at the low level. 1: Pin P20 is at the high level.

5. Flowchart



5.3.3 Function irq0_int

1. Functional overview
   This is the handler for IRQ0; it produces toggled output on pin P20.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 2 data register (P2DR) Number of bits: 8 Address: H'FFFF51

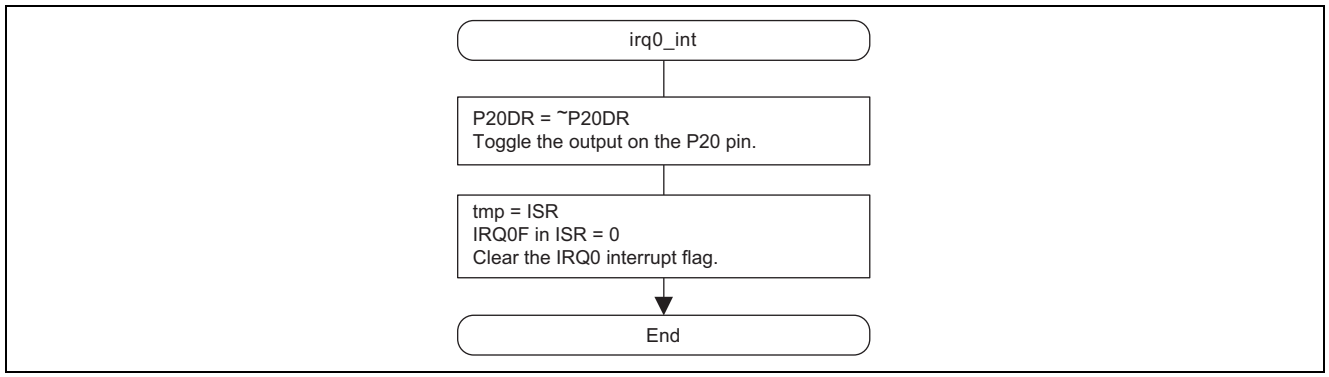
Bit	Bit Name	Setting	R/W	Description
0	P20DR	0/1	R/W	0: Pin P20 is at the low level. 1: Pin P20 is at the high level.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Description
0	IRQ0F	0	R/(W)*	[Setting condition] • Generation of an interrupt source selected in the ISCR. [Clearing conditions] • Writing 0 to IRQ0F after having read it as 1 • Execution of interrupt exception handling while low-level sensing is selected and the $\overline{\text{IRQn}}$ input is high (n = 0, …, 11) • Execution of IRQn interrupt exception handling while falling-, rising-, or both-edge sensing is selected • Activation of the DTC by an IRQn interrupt when the DISEL bit in MRB of the DTC is cleared to 0

Note: * Only 0 can be written, to clear the flag.

5. Flowchart



6. Documents for Reference (Note)

- Hardware Manual
  H8SX/1653 Group Hardware Manual
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1.00	Sep.25.07	—	First edition issued

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