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M32C/85 Groups

Intelligent I/O - Use of 2 Channels for Clock Synchronous Serial Communication and 4 Channels for PWM Output (Fixed PWM Cycle)

1. Abstract

This application note describes a procedure to use 2 channels for clock synchronous serial communication and 4 channels for PWM output (fixed PWM cycle).

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M32C/85 Groups, 144-pin package

(In a 100-pin package, eight intelligent I/O waveform output ports and five out of six intelligent I/O serial communication ports are shared)

System clock: 30MHz

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFRs (Special Function Registers) as the M32C/85 Groups. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

3. Detailed Description

The intelligent I/O includes followings.

- 16-bit base timer register for free-running operation x 1
- 16-bit register for time measurement or waveform generation x 8
- A set of two 8-bit shift registers for communication x 2

The OUTC1j (j = 4 to 7) pin outputs PWM waveform signal with fixed cycle and variable duty ratio.

The transmit data for the clock synchronous serial communication is output from the ISTxDi (i = 0,1) pin and the transfer clock is output from the ISCLKi pin while the received data is input to the ISRxDi pin.

Table 1 lists pin settings for a sample program in this application note.

Figure 1. Pin Settings

Category	Pin No.	Pin Name	Port No.
Serial Communication Channel 1	34	ISTxD1	P73
	33	ISCLK1	P74
	32	ISRxD1	P75
Serial Communication Channel 0	31	ISTxD0	P76
	30	ISCLK0	P77
	29	ISRxD0	P80
Fixed PWM Cycle Output	14	OUTC14	P140
	13	OUTC15	P141
	12	OUTC16	P142
	11	OUTC17	P143

Table 2 to Table 4 list selectable functions. The sample program is for when the checked functions are selected in these tables.

Table 2. PWM Output Channel j (j = 4 to 7) Selectable Functions in Single Waveform Output Mode

Item	Settings	✓
Default Output	"L" output as default	✓
	"H" output as default	
Inverse Output Level	Output level is not inversed	✓
	Output level is inversed	

Table 3. Selectable Functions in Communication 0 Clock Synchronous Serial Interface Mode

Item	Settings	✓
Count Source		Cannot be selected
Divide Ratio of Count Source		Cannot be selected
Transfer Clock	Internal clock	✓
	External clock	
Transfer Clock Setting	f8	
	f2n (n = 15)	✓
	Input from ISCLK0	
Transfer Format	LSB first	✓
	MSB first	
ISRxD, ISTxD Polarity Inverse	No inverse	✓
	Inverse	
Transmit Interrupt Cause	No data in the G0TB register	
	Transmission is completed	✓

Table 4. Selectable Functions in Communication Unit 1 Clock Synchronous Serial I/O Mode

Item	Settings	√
Count Source	Stop clock	
	Apply two-phase pulse	
	f1	√
Divide Ratio of Count Source	Divide-by-2	
	:	
	Divide-by-64	
	No division	√
Transfer Clock	Internal clock	√
	External clock	
Transfer Clock Setting	Generate in channel 3 phase-delayed waveform output mode	√
	f8	
	f2n	
	Input from ISCLK0	
Transfer Format	LSB first	√
	MSB first	
ISRxD, ISTxD Polarity Inverse	No inverse	√
	Inversed	
Transmit Interrupt Cause	No data in the G1TB register	
	Transmission is completed	√

(1) Settings for PWM Cycle by Channel 0 and Transfer Speed of Communication Unit 1

Set the PWM cycle and transfer clock cycle for communication unit 1 by channel 0. (the PWM cycle and the transfer clock cycle are synchronized in the following program)

Set the FSC0 bit in the G1FS register to 0 (selects the waveform generating function).

Set bits MOD 2 to 0 in the G1POCRj (j=0 to 7) to 111b (use communication function output).

Data output for communication unit 1 is automatically selected as to the ISTxD1 pin.

Set the RST1 bit in the G1BCR1 register to 1 (the base timer is reset by matching with the G1PO0 register).

When fBT1 is the count source of base timer and n is a setting value of the G1PO0 register, PWM cycle and transfer speed of communication unit 1 (transfer clock cycle) can be calculated by following equations.

$$\text{PWM cycle: } \frac{n+2}{fBT1}$$

$$\text{Transfer speed: } \frac{fBT1}{2(n+2)}$$

(2) Output Setting for the ISCLK1 Pin

Set the FSC1 bit in the G1FS register to 0 (selects the waveform generating function).

Set bits MOD 2 to 0 in the G1POCRj (j = 0 to 7) register to 111b.

Clock output for communication unit 1 is automatically selected as to the ISCLK1 pin.

(3) Transfer Clock Generation by Channel 3 (Communication Unit 1)

The transfer clock is generated in phase-delayed waveform output mode of the channel 3 waveform generating function. In the sample program, the transfer clock is generated as soon as the base timer starts counting, when the G1PO3 register is set to 0001h.

(4) Low-level ("L") Width Setting of PWM Pulse by Channel j (j = 4 to 7)

Set the "L" width of PWM output waveform in single-phase waveform output mode of channel j waveform generating function.

The "L" width can be calculated from the following equation when m is the setting value of the G1POj register.

$$\text{"L" width: } \frac{m}{f_{BT1}}$$

(5) "L" Width of PWM Pulse

When the G1POj register value is rewritten in the channel 0 waveform generating interrupt mode, the "L" width of PWM waveform is changed.

4. Settings for Sample Program

- Channel j(j=4 to 7)PWM cycle: 100 μ s
- Communication unit 1 bit rate: 5000 bps
- Communication unit 1 bit rate: 1 Mbps

Sample program has the definition values as listed in Table 5. The “H” width ratio of channel j (j = 4 to 7) PWM output is increased in the sample program. When the frequency of duty ratio change reaches the set value (“3” for an example in Table 5), the ratio is back to the default. This routine is repeated.

Table 5. Definition Value of Sample Program

Items	Definition Value	Setting Ranges
PWM cycle based on fBT1 (number of communication unit 1 transfer clock cycle divided by 2)	3000	100 to 65500 (hector-unit)
Initial ratio of “H” width (channel 4 PWM output) (%)	60	0 to 100
Initial ratio of “H” width (channel 5 PWM output) (%)	50	”
Initial ratio of “H” width (channel 6 PWM output) (%)	40	”
Default ratio of “H” width (channel 7 PWM output) (%)	30	”
“H” width increment ratio (%)	10	0 to (no more than the “H” width ratio of 100%)
Frequency of duty ratio change	3	0 to (no more than the “H” width ratio of 100%)

Figure 1 to Figure 3 show timing diagrams of the sample program

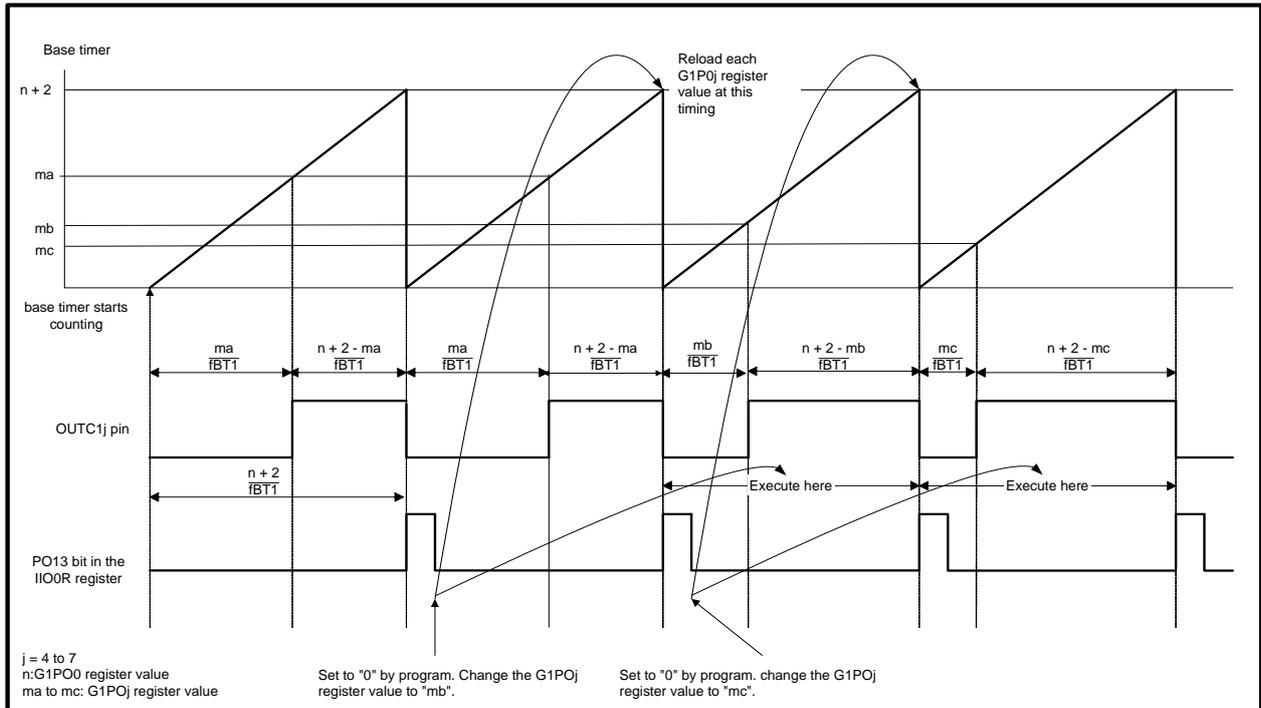


Figure 1. PWM Waveform Timing Diagram

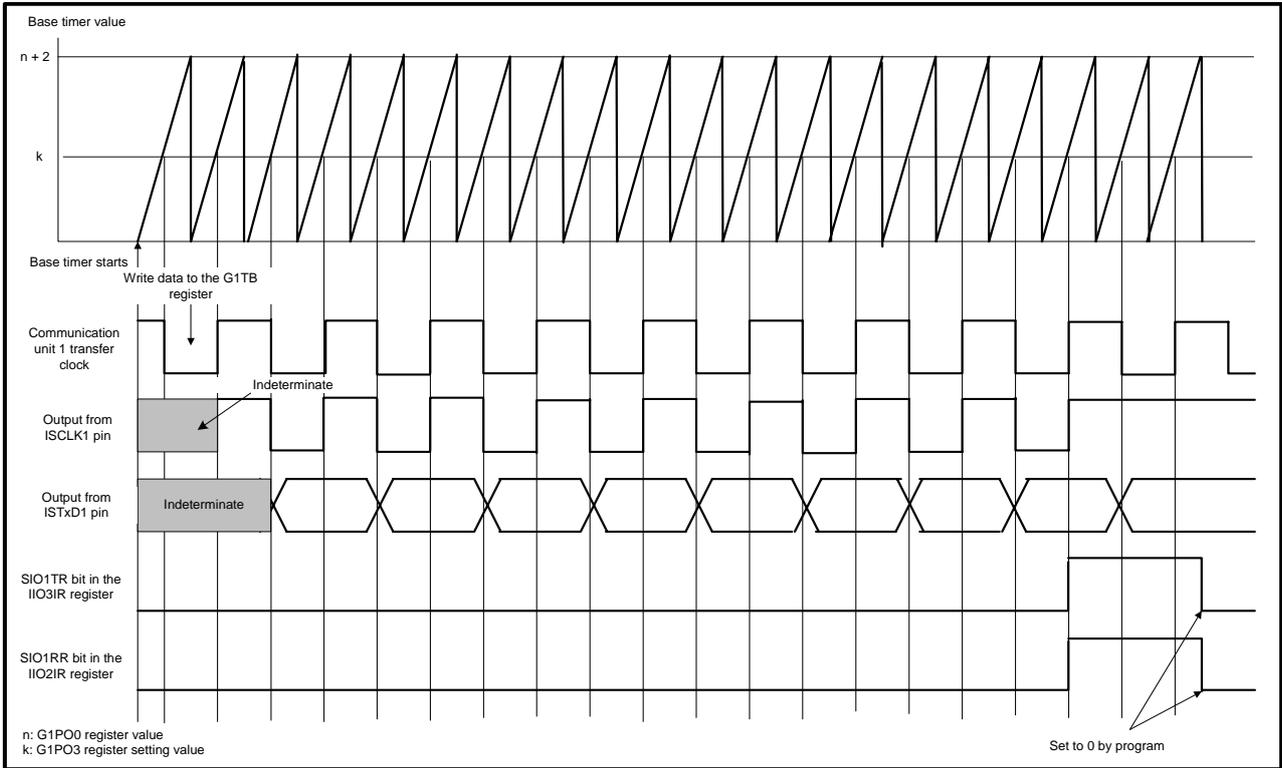


Figure 2. Transfer/Receive Timing Diagram of Communication Unit 1

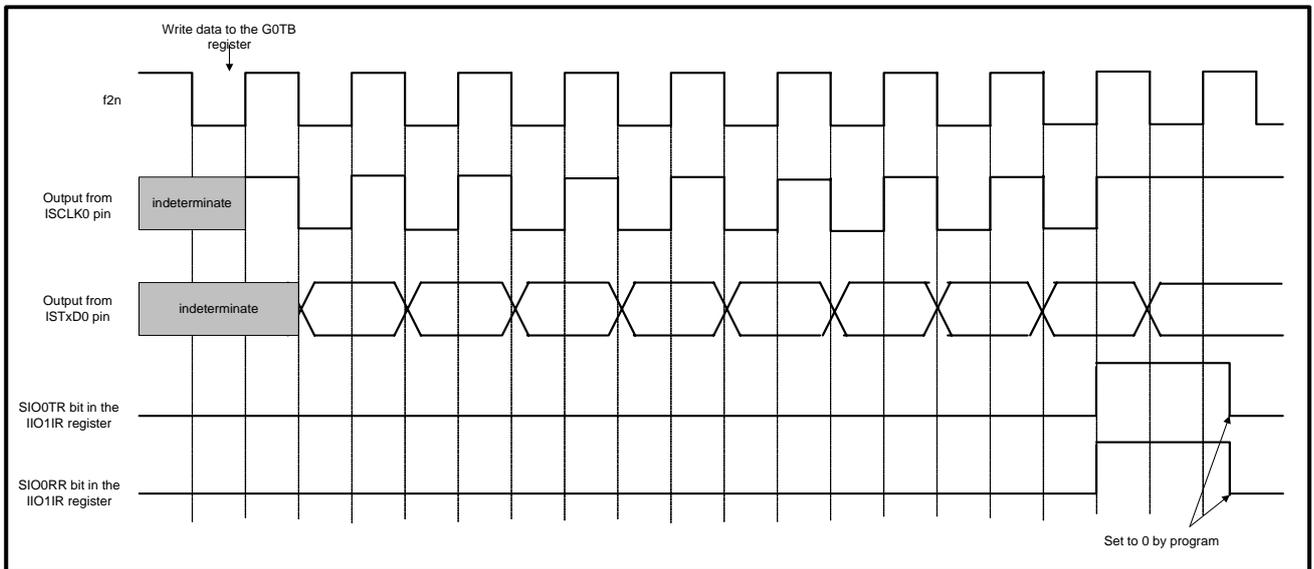


Figure 3. Transfer/Receive Timing Diagram of Communication Unit 0

Figure 4 to Figure 6 show flow charts of register settings.

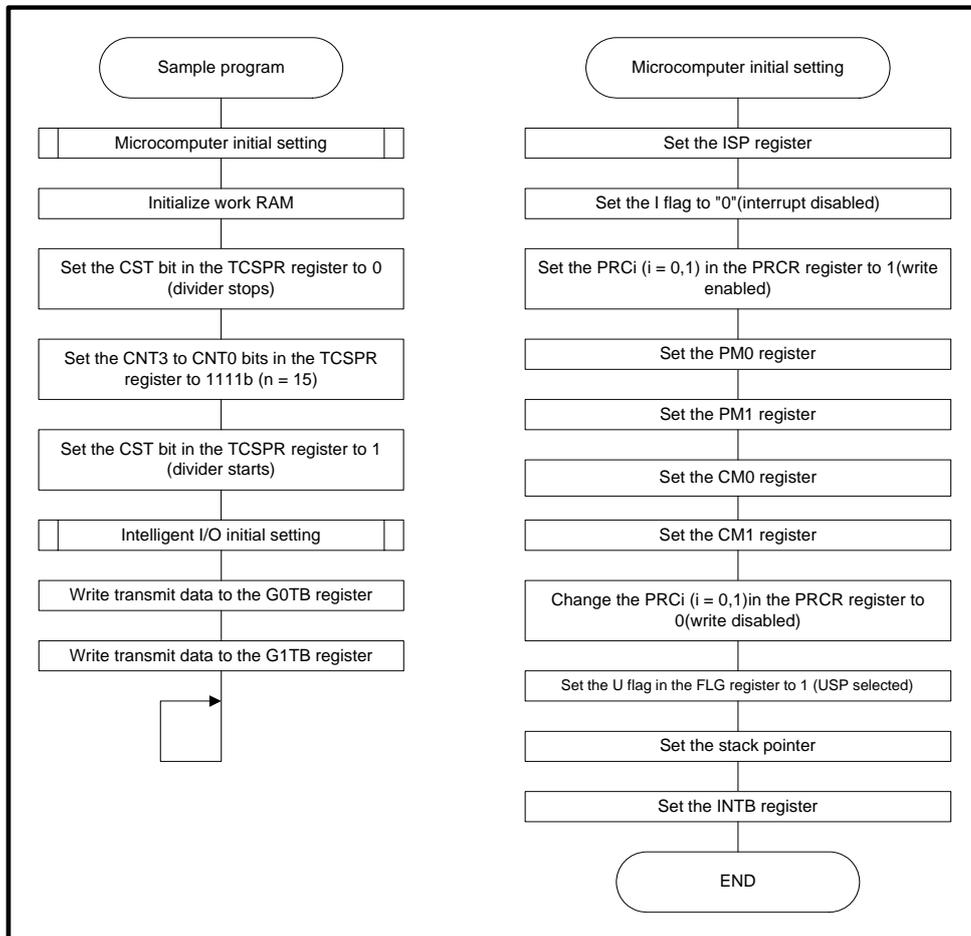


Figure 4. Register Setting (1)

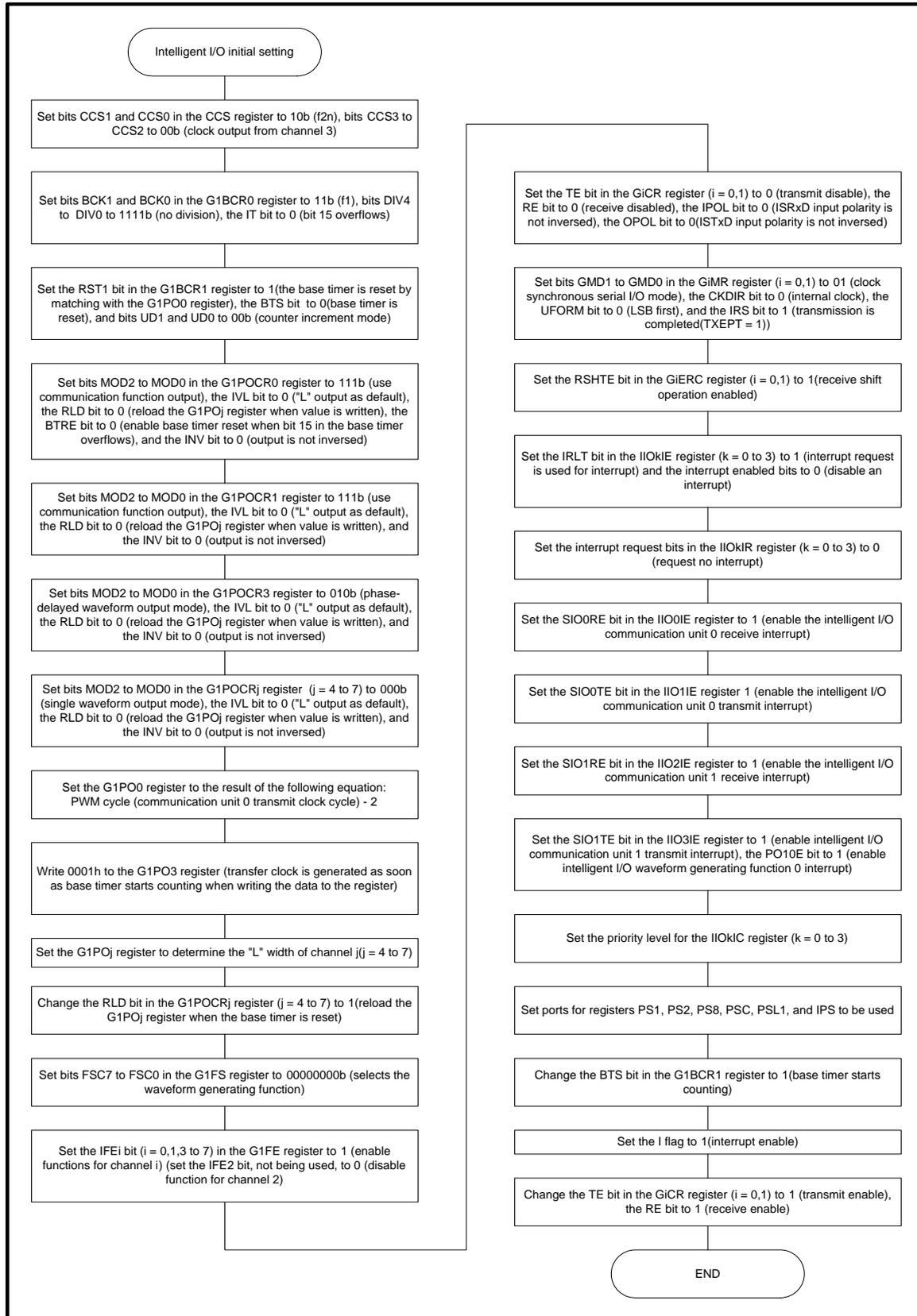


Figure 5. Register Settings (2)

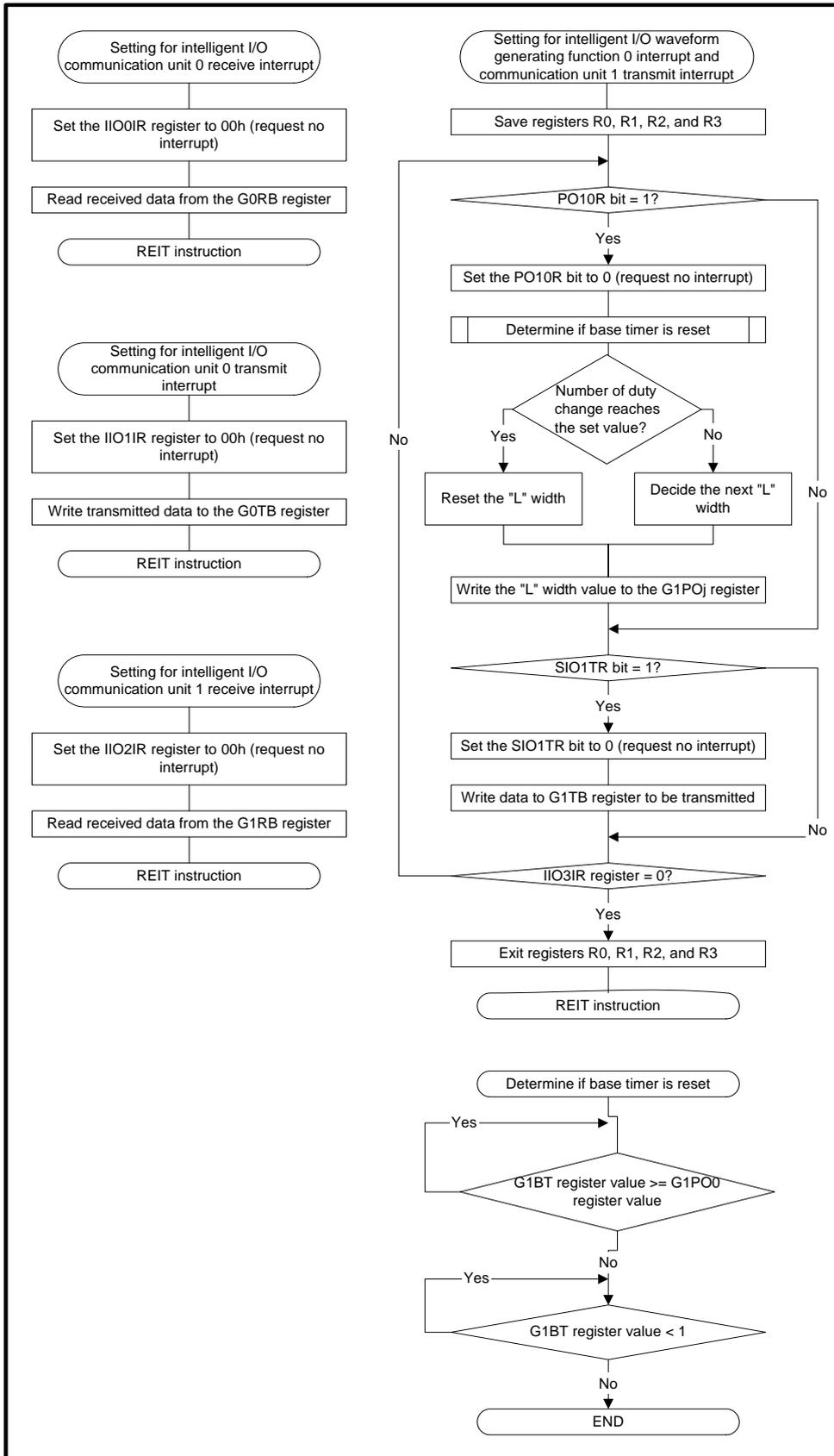


Figure 6. Register Settings (3)

5. Reference Program

Please find the reference program from the Renesas Technology Web site.
Click Application Note in the left menu of the M32C/80 Series top page.

6. Reference Documents

Hardware manual

M32C/85 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update

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