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M32C/80 Series

Intelligent I/O Functions

1. Abstract

This application note describes the intelligent I/O functions of M32C/80 series.

2. Introduction

This application note is applied to the following microcomputers.

MCU : M32C/80 series

3. Introduction of Applied Technology

3.1. Intelligent I/O

Intelligent I/O is a peripheral function of M32C/80 series, composed of time measurement (timer) unit and communication unit.

- Time measurement unit
  Input capture (Note1) (time measurement function)
  Output compare(Note1) (waveform generation function)

- Communication unit
  Various types of serial bus interfaces can be achieved with the combination of the time measurement unit and the communication unit.
  (Applicable interface: Clock Synchronous Serial I/O, UART, HDLC data processing, IEBus(note2) etc.)

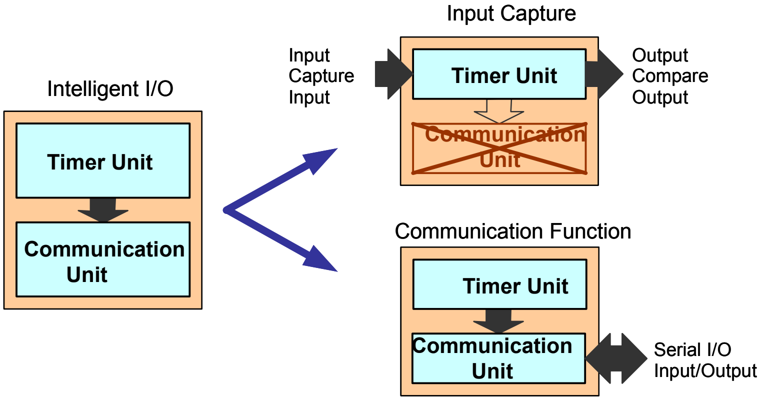


Figure 1 Intelligent I/O Configuration

Figure 1 summarized how to use the intelligent I/O. Please use time measurement unit for time measurement function, and both time measurement unit and communication unit for communication function.

Note1: In hardware manual, “Input Capture” is described as “Time Measurement Function”, while “Output Compare” as “waveform generation Function”. In this application note, the expression of “Input Capture”, “Output Compare” are used.
Note2: IEBus is the trade mark of NEC Electric Corp.

Intelligent I/O consists of 4 groups from group 0 to group 3. Intelligent I/O contains input capture channels up to 12, and output compare channels up to 20 at the maximum.
There are various serial bus interfaces available in the communication unit of every group.

- Group 0, Group 1
  8-bit synchronous/asynchronous communication function, HDLC data processing function
- Group 2
  Variable bit length synchronous communication function, IEBus communication function
- Group 3
  8-bit/16-bit Synchronous communication function.

Table 1 lists existence of intelligent I/O groups for M32C/80 series.

Table 1 Existence of Intelligent I/O group for M32C/80 Series

	M32C/80	M32C/81	M32C/82	M32C/83	M32C/84	M32C/85	M32C/86
Group 0	Communication unit only	O	O	O	-	-	-
Group 1	Communication unit only	O	O	O	O	O	O
Group 2	-	O	O	O	-	-	-
Group 3	-	-	-	O	-	-	-

Table 2 lists functions and channels of intelligent I/O for M32C/80 series.

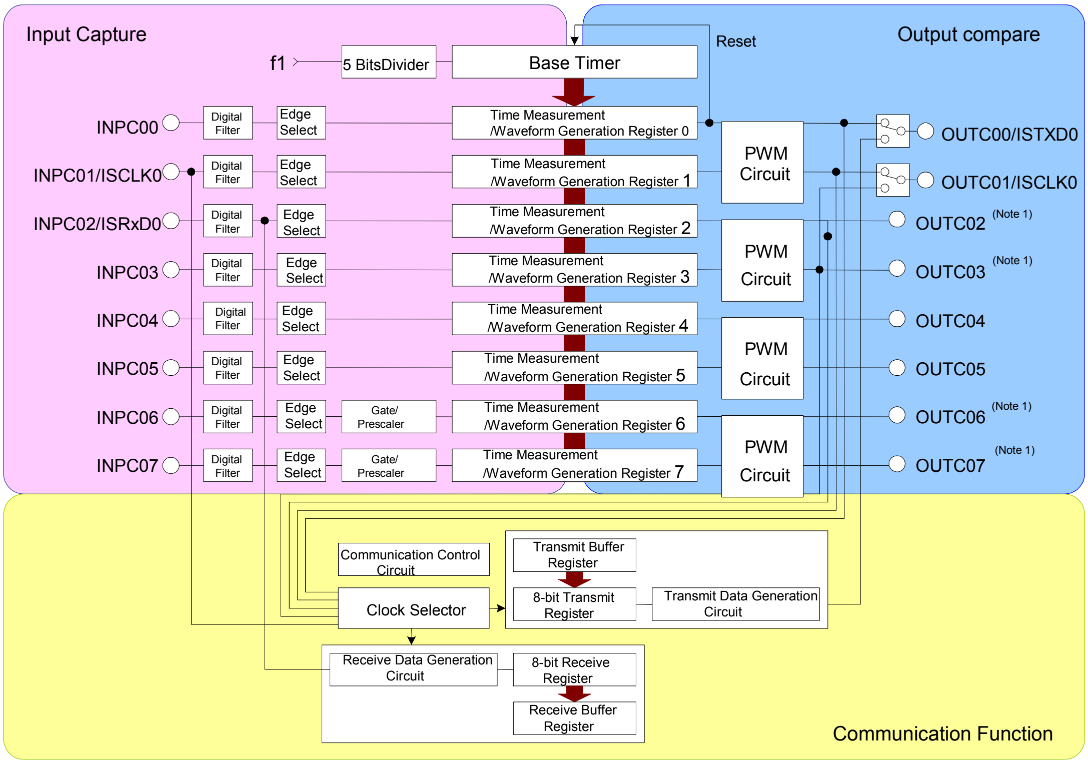
Table 2 M32C/80 Series Intelligent I/O Functions and Channels

Functions	Group 0	Group 1	Group 2	Group 3	Group 0,1 cascaded
Input Cature	O	O	-	-	O
Digital Filter	O	O	-	-	O
Trigger Input Prescaler	O	O	-	-	O
Trigger Input Gate	O	O	-	-	O
Waveform Generation	O	O	O	O	O
Single-phase Waveform Output Mode	O	O	O	O	O
Phase-delayed Waveform Output Mode	O	O	O	O	O
SR Waveform Output	O	O	O	O	O
Bit Modulation PWM Mode	-	-	O	O	-
RTP Mode	-	-	O	O	-
Parallel RTP Mode	-	-	O	O	-
Communication	8 bit fixed		Variable	8 or 16 bit	-
Clock Synchronous Serial I/O Mode	O		O	O	-
UART Mode	O		-	-	-
HDLC Data Processing Mode	O		-	-	-
IE Mode	-		O	-	-

3.2. The consist of Intelligent I/O (Group 0)

Following is an example of group 0 to explain the configuration of Intelligent I/O groups.
Base timer operation is a basic element of input capture function and output capture function of time measurement unit.

Base timer is a 16-bit free-running timer, and peripheral function clock becomes count source of the base timer



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Note 1 M32C/81,82,83are not to connect to pins

Figure 2 Intelligent I/O Block Diagram

- Timer Unit
  Base timer
    5-bit divider
    16-bit base timer
  Input capture
    Time measurement register
    Digital filter function
    Edge select function
    Gate/prescaler function
  Output compare
    Waveform register
    PWM circuit
- Communication Unit
    8-bit receive buffer
    8-bit receive register
    8-bit transmit buffer
    8-bit transmit register
  Transmit and receive data generation circuit
    Start/stop bit generation function
    Bit stuffing (bit insert/delete) functions
    CRC calculation function
    Interrupt generation function matching receive data

3.3. Input Capture Function (Time Measurement Function)

When a trigger input signal is applied, the timer value is stored in the time measurement register, and interrupt request is generated.

At the timing when an external trigger output signal is applied, the base timer value is stored in the time measurement register. A time measurement interrupt request is generated when a trigger input signal is applied.

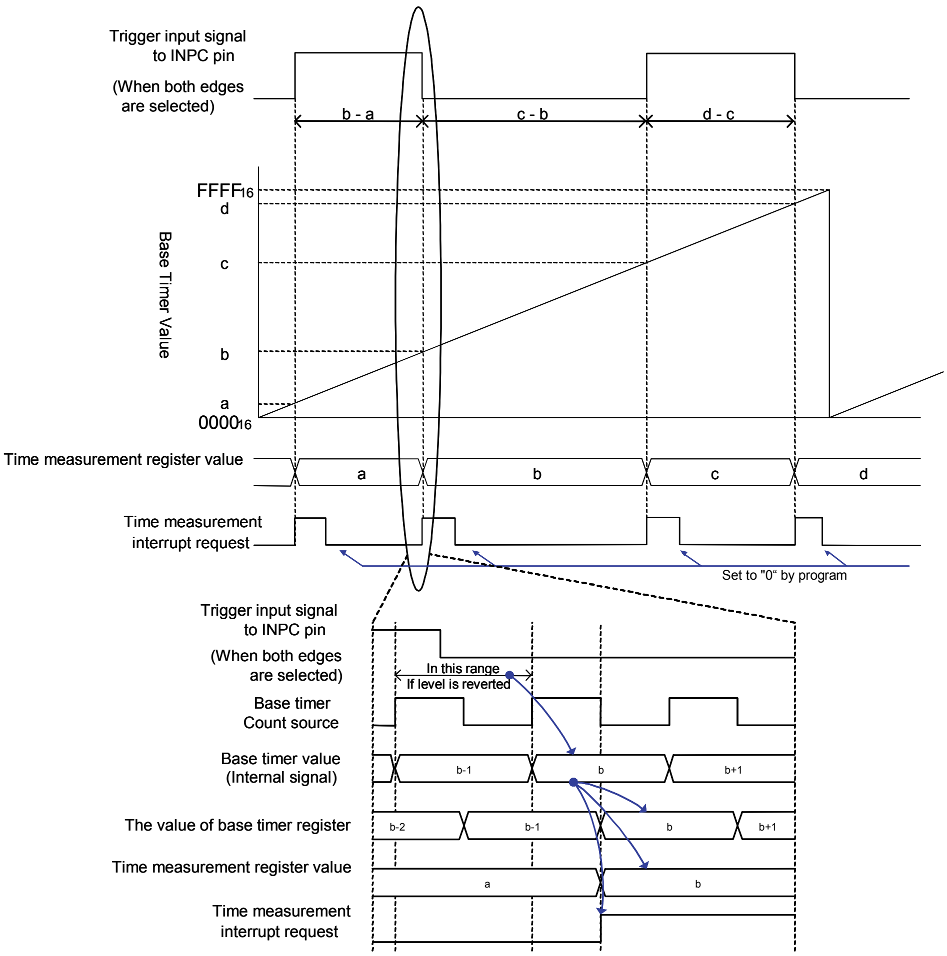

Figure 3 Input Capture Operation Diagram

Input capture function enables to measure signals per following purpose.

- Edge select function
- Digital filter function
- Gate function
- Prescaler function

Following is the explanation for these functions.

3.3.1. Edge Select Function

Edge select function can select trigger input polarity out of rising edge, falling edge and both edges.

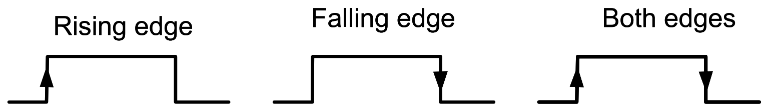

Figure 4 Edge Select Figure

3.3.2. Digital Filter Function

The filter clock samples trigger input signal and signals that match three times are passed. f1 or base timer count source can be selected as filter clock.

The digital filter function samples a trigger input signal level three times. The signal, which level matches three times, can pass digital filter and become the trigger signal. The signal, which doesn't match three times, is stripped off.

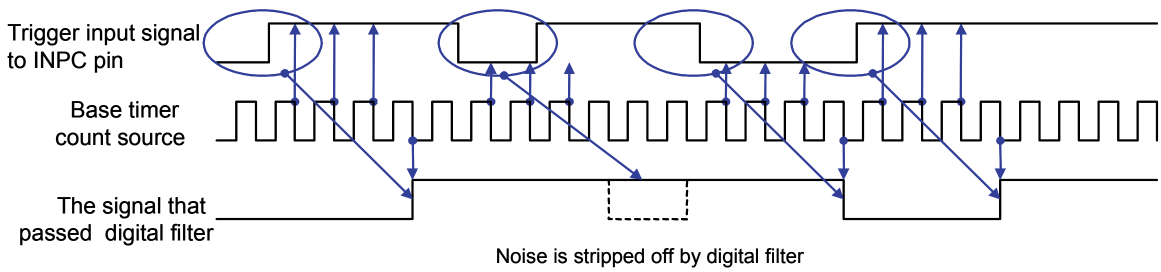

Figure 5 Digital Filter Operation Timing Diagram

In Figure 5, both edges are selected as trigger input polarity, while the count source (fBT) of the base timer is selected as the filter clock.

After the rising edge is applied to INPC pin, level sampling has been carried out three times per every fBT cycle. The signal that matches three times changes after passing the digital filter. Time measurement can be carried out by using the noise-free signal that passed digital filter.

(When using the digital filter function, the trigger signal is delayed due to sampling of the trigger input level. However, as the delay happened in the over all process, time measurement can be carried out correctly.)

3.3.3. Gate Function

Gate function is a function that could disable the trigger input signal receiving at any time after the initial trigger signal is applied.

This receive disable status can be cleared by the program or by matching waveform generation register with the base timer.

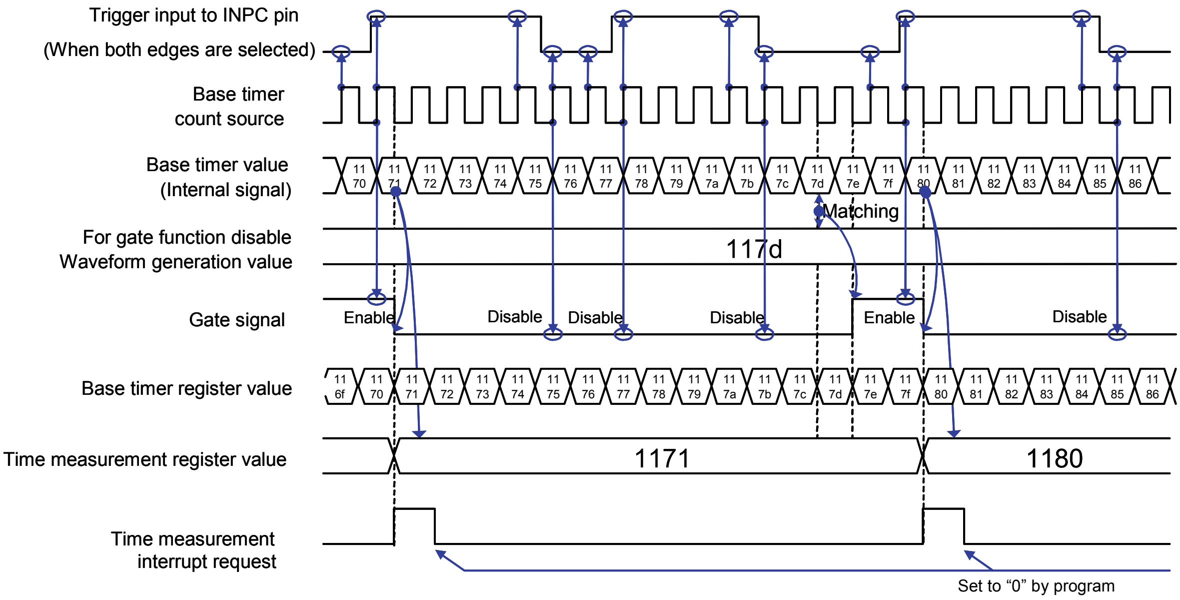

Figure 6 Gate Function Operation Timing Diagram

In Figure 6, when a trigger input signal is applied to INPC pin, the base timer value is stored in the time measurement register, and trigger input receive is disabled. However, trigger input receive disable can be cleared by matching the base timer value with the one written in the waveform generation register ($117d_{16}$). After trigger receive disable is cleared, the base timer value is stored in time measurement register at the timing when the trigger input is applied.

3.3.4. Prescaler Function

By counting trigger input signals, capture is carried out at every designated number of times.

In prescaler function, the base timer value is stored in the time measurement register at every designated number of times of applied trigger input signals. The register that designates the prescaler value consists of 8 bits, and the prescaler value could be set up to 255 times. (the designated number of times stands for the prescaler setting value +1.)

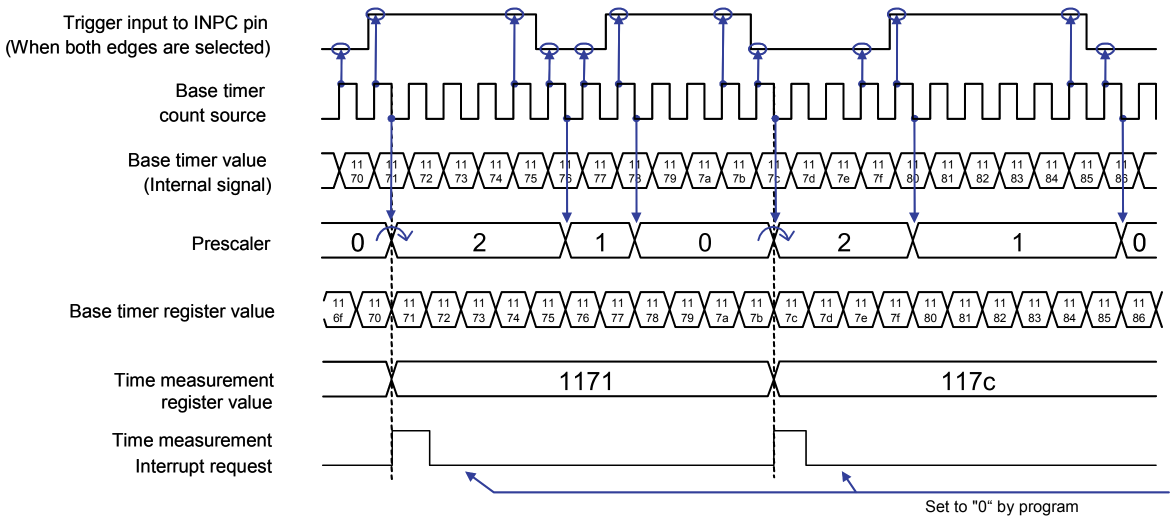

Figure 7 Prescaler Operation Timing Diagram

Figure 7 the prescaler value is set to “2”. When the initial trigger input signal is applied, the base timer value is stored at the time measurement register. Then, by counting the trigger input signal, the base timer value is stored at the third time trigger signal input.

3.4. Output Compare (Waveform Generation Function)

The output compare function can generate matching signal at the timing when the base timer value matches that of the waveform generation register. Interrupt request is generated by this matching signal, and the output signal changes.

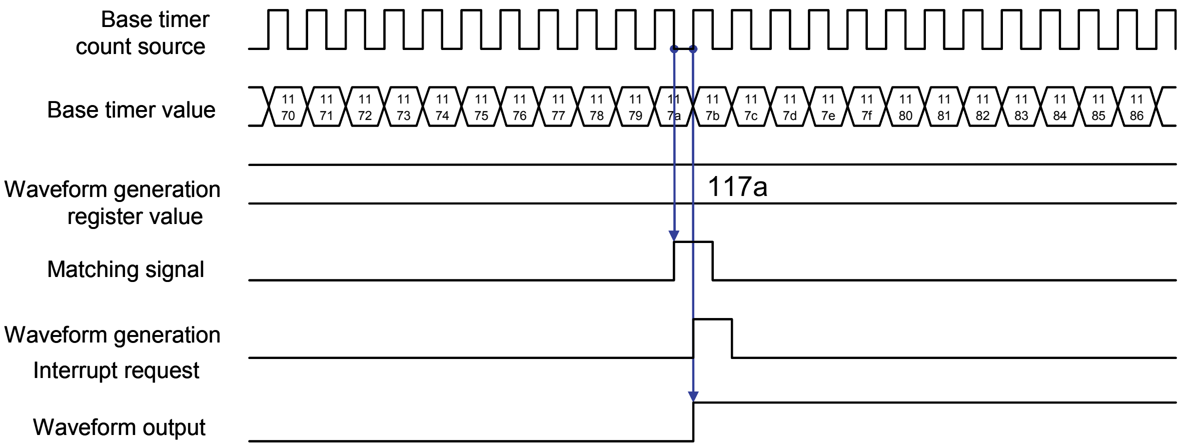

Figure 8 Output Compare (Waveform Generation Output) Operation Timing Diagram

3.4.1. Basic Waveform Output

This is a waveform output mode common to all groups.

(1) Single-phase waveform output
In single-phase waveform output mode, output level of the waveform output pin becomes “H” at the timing when the value of waveform generation register matches that of the base timer. The “H” signal switches to “L” when the value of the base timer value reaches “0000_{16}”.

(2) Phase-delayed waveform output
In phase-delayed waveform output mode, the output signal level from the waveform output pin is inversed at the timing when the value of the waveform generation register matches that of the base timer.

(3) Set-reset (SR) waveform output
In set-reset waveform output mode, the output signal level from the waveform output pin becomes “H” level at the timing when the value of waveform generation register “n (n=0,2,4,6)” matches that of the base timer. The output signal level from the waveform output pin switches to “L” at the timing the value of waveform generation m (m=n+1) matches that of the base timer, or when the value of the base timer reaches “0000_{16}”.

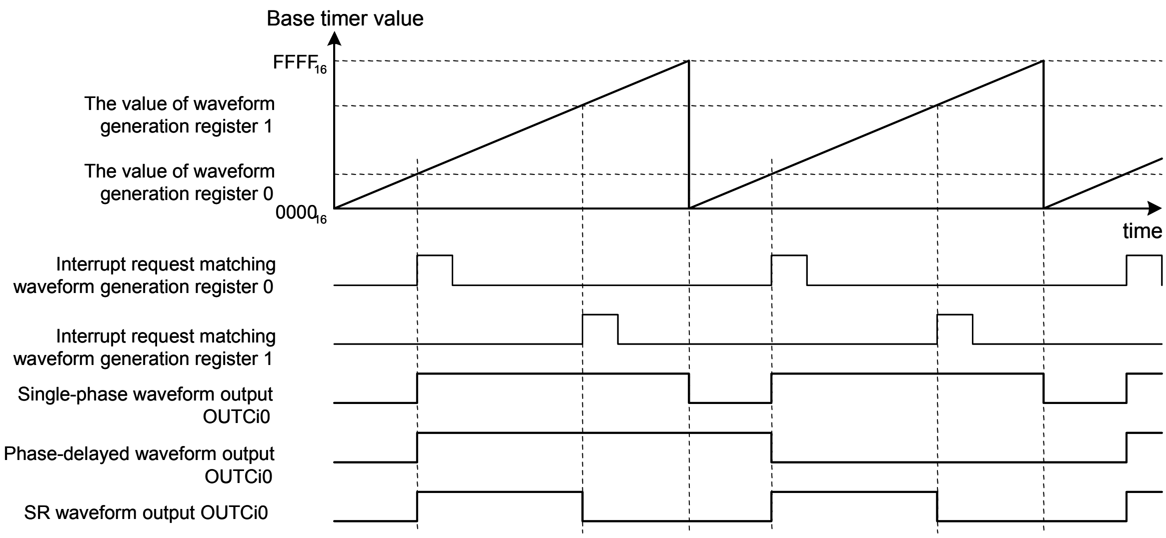

Figure 9 Waveform Generation Output Operation Timing Diagram

Selectable functions in each mode:

• Initial value set function
  Initial output level setting of the output compare pin

• Output inverse function
  The output inversing circuit is the final step of the waveform generation circuit.
  Output polarity can be inversed.

• Base timer reset function by matching waveform generation register 0 with base timer.
  Base timer is reset when the value of the waveform generation register 0 matches that of the base timer.
  The base timer reaches "0000_{16}" two clock cycles after the base timer value matches that of the waveform generation register.

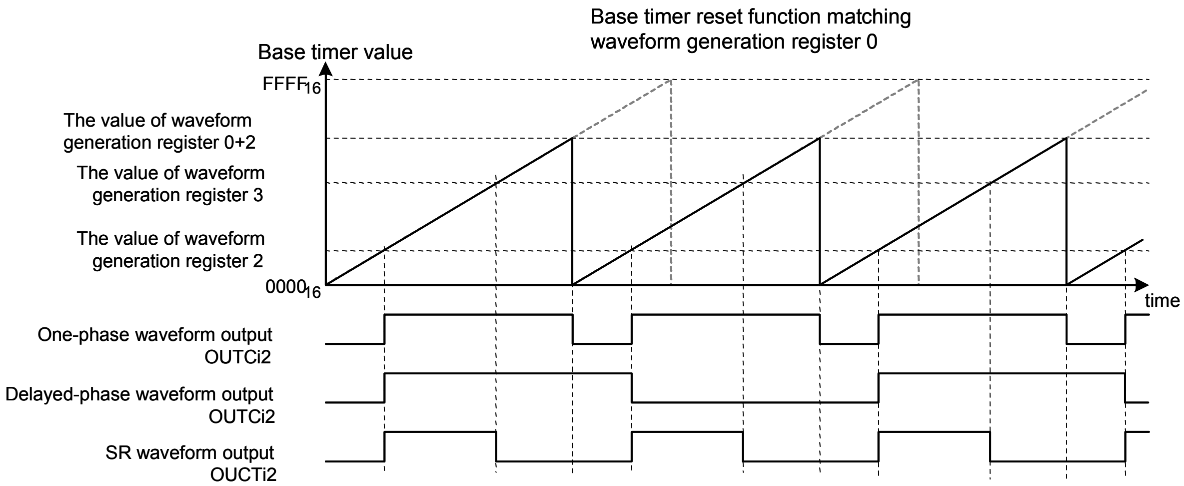

Figure 10 Base Timer Reset Function Operation Diagram

In Figure 10, the base timer reaches "0000_{16}" two clock cycles after the base timer value matches that of the waveform generation register.

3.4.1.1. Application Example: 16-Bit PWM Output

Following is an example of 16-bit PWM output by using output compare function.

PWM frequency is set at waveform generation register 0. Please select “Reset base timer by matching the base timer value with that of the waveform generation 0.

Output compare “L” width is set at waveform generation register 1 to 7.

In conventional M16C series, frequency is fixed when a 16-bit PWM output by timer A is achieved. When using intelligent I/O, a 16-bit PWM output can be achieved with variable frequency.

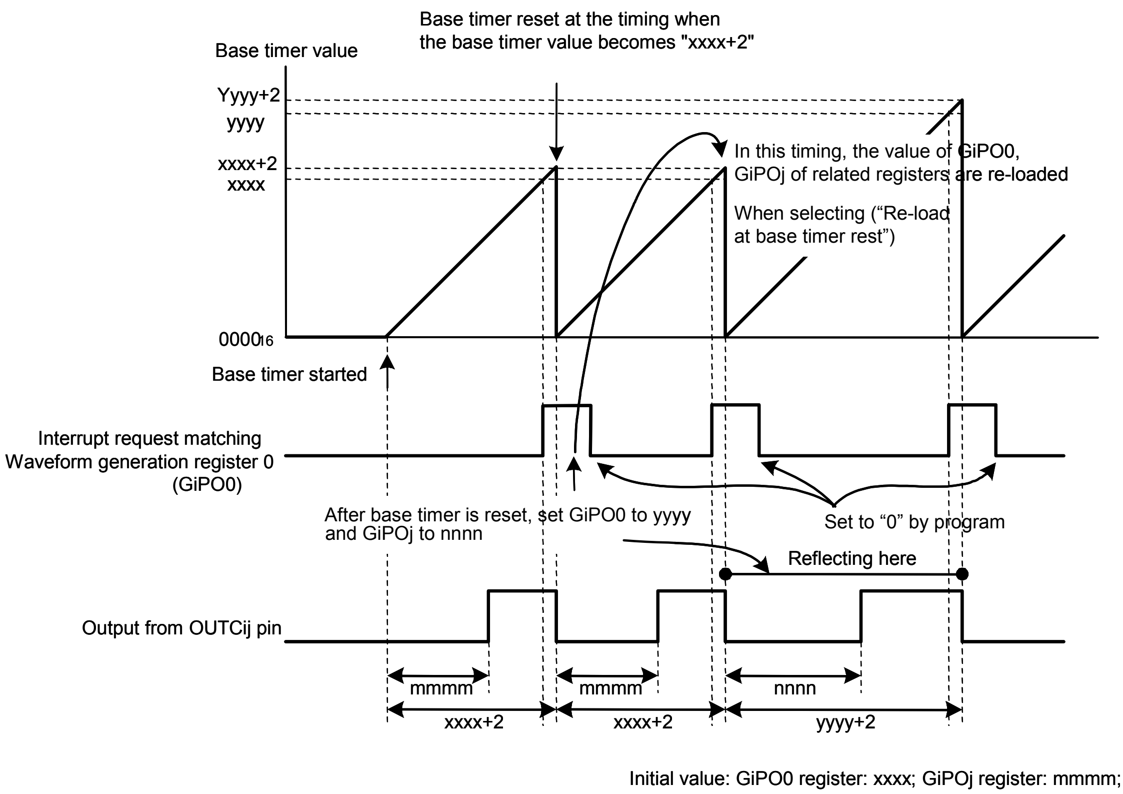

Figure 11 16-bit PWM Output Timing Diagram

In Figure 11, the GiPO0 register is set to xxxx, while the GiPOj register to mmmm to start the base timer. A interrupt request is generated when the base timer value matches that of GiPO0 register, then the output of OUTCij pin becomes “L”, and the value of base timer becomes “0000_{16}” 2 clock cycles later.

3.4.2. Bit Modulation PWM Output

Bit modulation PWM output mode can be used in group 2 and 3.
When using this function, high-frequency output can be achieved while maintaining the accuracy of the 16-bit PWM output.

• Carrier-frequency	6-bit PWM equivalent
• PWM precision (resolution)	16-bit

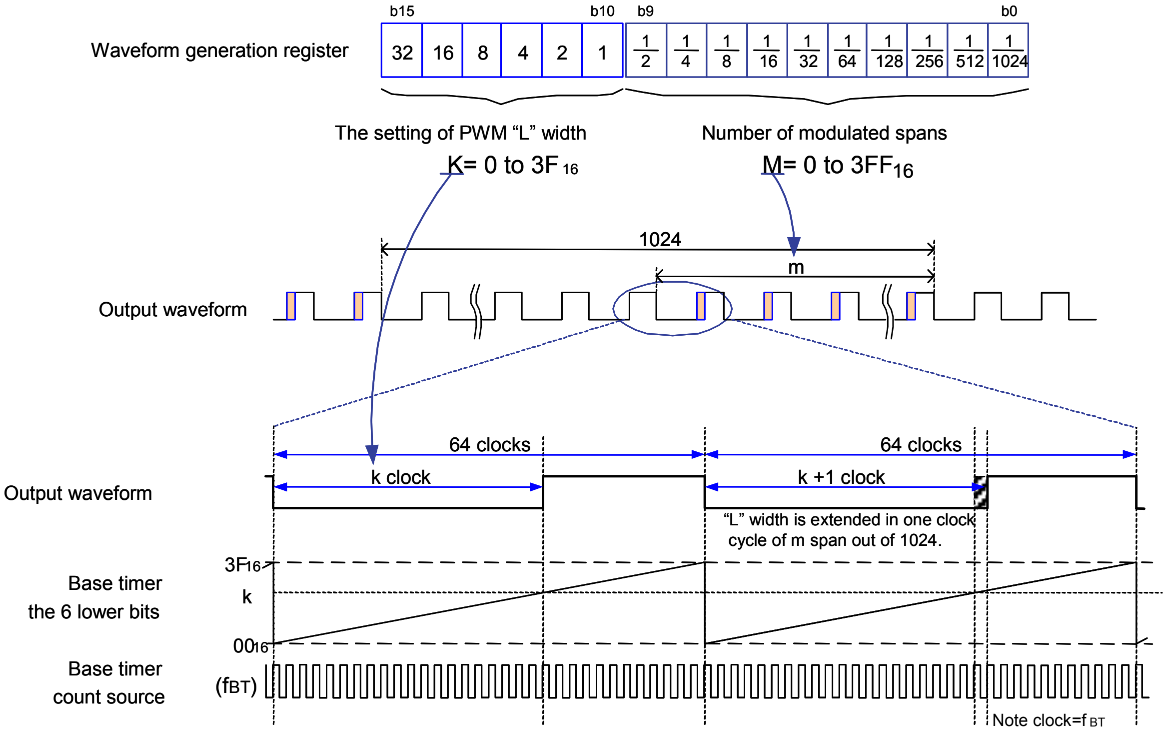

Figure 12 Bit Modulation PWM Output Schematic Drawing

PWM cycle is fixed at 64 clock cycles/fBT. The "L" pulse width of PWM is set in the upper six bits in the 16-bit waveform register, the incremental number of "L" pulse width in one clock cycle is set in the lower 10 bits of the 16-bit waveform register.

When the PWM output pulse width is varied with 16-bit resolution, the $FFFF_{16}$/count source cycle for the PWM output that using the base timer is required. High carrier frequency PWM output can be achieved in the bit modulation PWM output mode.

3.4.3. Real-Time Port (RTP) Output

Following is an explanation for real-time port output mode. This mode can be used in group 2 and 3. When the base timer value matches that of the waveform generation register, the setting value for the RTP output buffer register is output in bit.

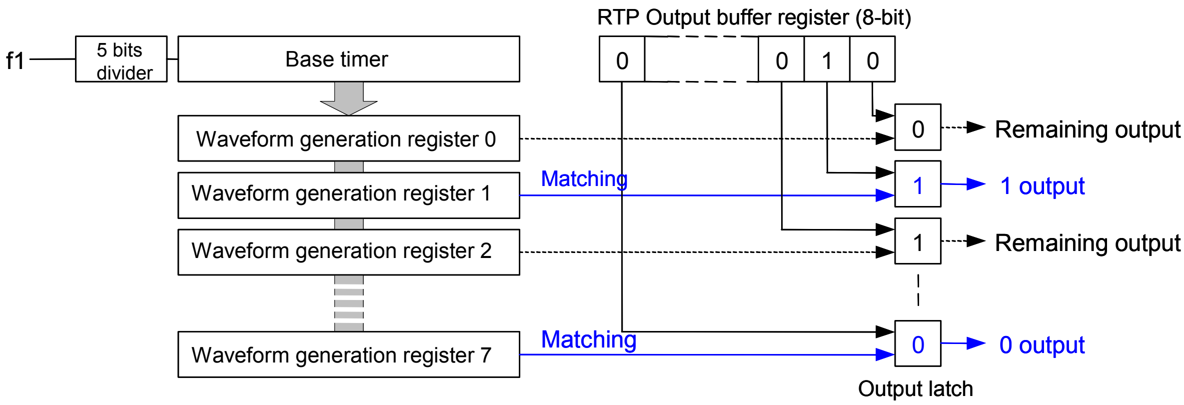

Figure 13 Configuration of Real-Time Port Output

Whenever the base timer value matches that of register i(i=0 to 7), the value of RTP output buffer register bit i is output from designated waveform output pins.

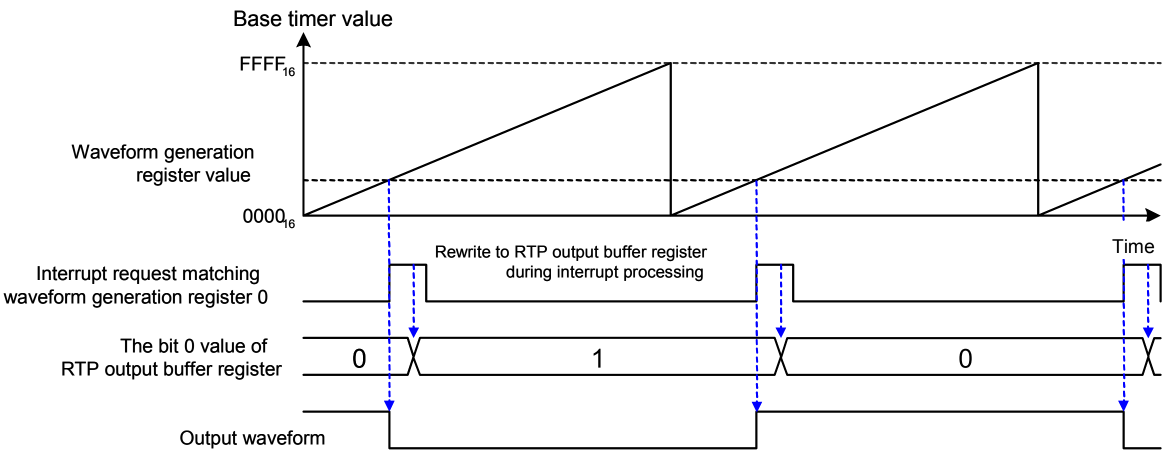

Figure 14 Real-Time Port Output Timing Diagram

3.4.4. Parallel Real-Time Port Output

Following is an explanation for parallel real-time port output mode. This mode can be used in group 2 and 3. When the base time value matches that of the waveform generation register, the value that set for RTP output buffer register is output in bit.

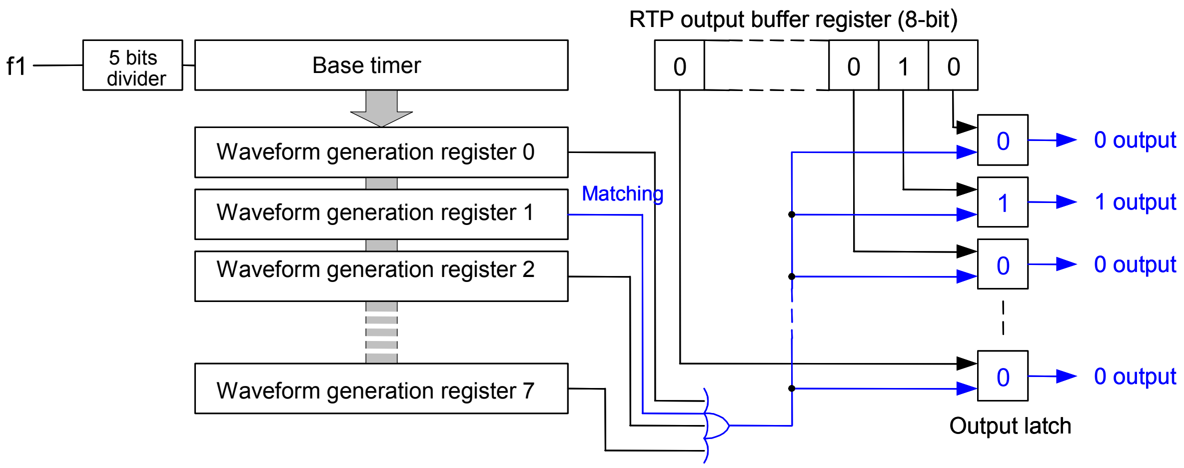

Figure 15 Parallel Real-Time Port Output Schematic Drawing

Whenever the base time value matches that of waveform generation register, the value of RTP output buffer register is output simultaneously from corresponding output pins. The signal level at the pin can be varied in a short interval by this function.

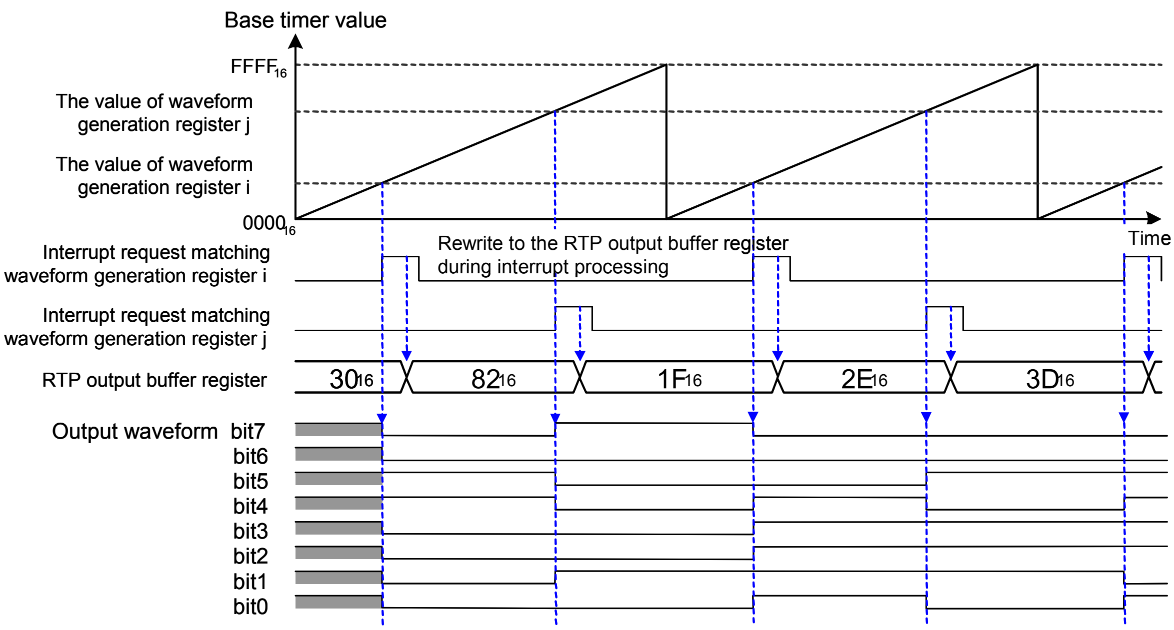

Figure 16 Parallel Real-Time Port Output Operation Timing Diagram

3.5. Communication Function

3.5.1. Clock Synchronous Serial I/O Mode (Group 0 and 1)

Following is an explanation for intelligent I/O communication function.
In the intelligent I/O groups 0 and 1, clock synchronous serial I/O and clock asynchronous serial I/O are available.

In clock synchronous serial I/O mode, transmit clock is generated by channel 3 phase-delayed waveform output mode of output compare function. When the transmit data is written in the transmit buffer register (GiTB register), the transmit data from ISTxD pin is output synchronously with the transfer clock.

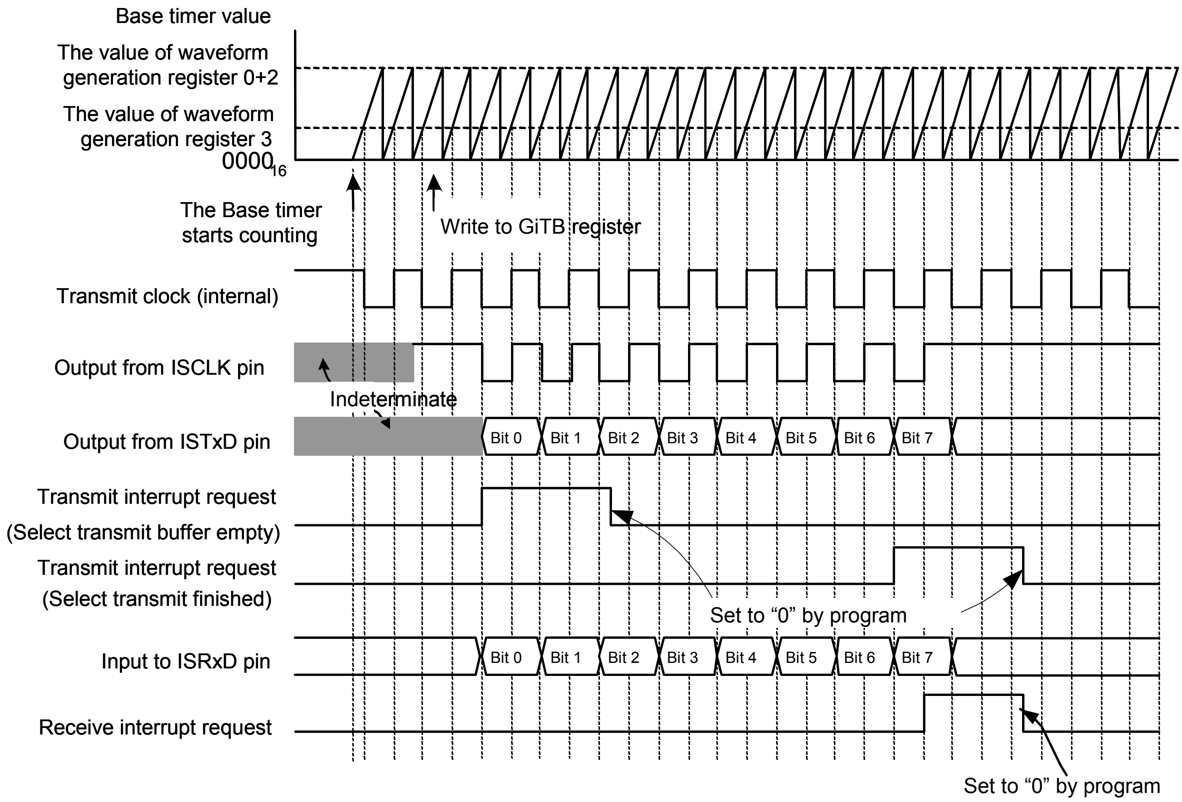

Figure 17 Clock Synchronous Serial I/O Output Timing Diagram

3.5.2. UART (Group 0 and 1)

Following is an explanation for clock asynchronous serial I/O (UART).

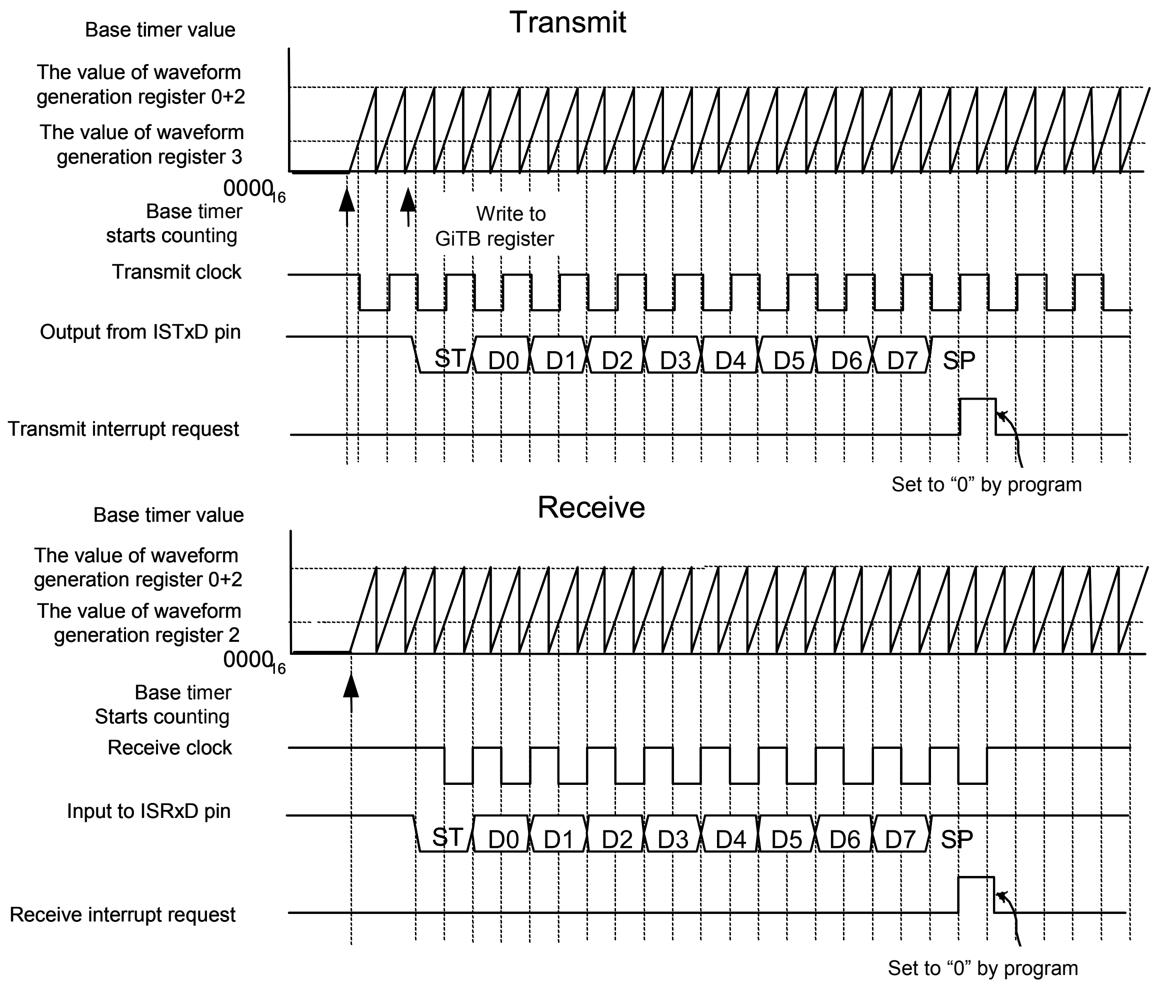

Figure 18 Clock Synchronous Serial I/O (UART) Output Timing Diagram

Similar to clock synchronous serial I/O output mode, a transfer clock is generated by phase-delayed waveform output mode.

In case the data is transmitted by UART, start bit, transmit data bit (8-bit) and stop bit are output from ISTxD pin by writing transmit data in GiTB register. A transmit interrupt request is generated after stop bit transmitting is completed.

In case the data is received by UART, when the input signal level to ISRxD pin varies, input capture function detects this change as a start bit. When start bit is detected, a transfer clock is generated, and when stop bit is detected, interrupt request is generated.

4. Reference

Hardware manual

Please refer to the hardware manual of M32C/80 series.
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5. Website and contact for support

Renesas web-site

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