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SH7262/SH7264 Group

Implementing the USB Enumeration on the USB Function Controller

Summary

This application note describes the configuration to use the SH7262/SH7264 USB 2.0 host/function module as the USB function controller and enumerate with the USB host.

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

Contents

1. Introduction

1.1 Specifications

Specifies the SH7264 MCU as the USB function to enumerate with the USB host.

1.2 Modules Used

- USB 2.0 Host/Function Module (USB module)
- Interrupt controller (INTC)

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.04.01
C Compiler	Renesas Technology SuperH RISC engine Family C/C++ compiler package Ver.9.02 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization

2. Applications

This application uses the USB 2.0 host/function module (USB module) as the USB function to enumerate with the USB host.

2.1 Overview of USB Module

(1) Includes the USB host controller and function controller compliant to USB high-speed
- Includes the USB host controller and function controller
- USB host controller and function controller can be switched by setting registers
- Includes the USB transceiver

(2) Reduced number of external pins and space-saving installation
- Includes the D+ pull-up resistor (When operating as the function)
- Includes the D+ and D− pull-down resistors (When operating as the host)
- Includes the D+ and D− terminator (When operating at high-speed)
- Includes the D+ and D− output resistor (When operating at full-speed)

(3) Supports all types of USB transfer
- Control transfer
- Bulk transfer
- Interrupt transfer (High-bandwidth is not supported)
- Isochronous transfer (High-bandwidth is not supported)

(4) Internal bus interface
- Includes two channels of DMA interface

(5) Pipe configuration
- Includes 8-KB buffer memory for USB communication
- Up to 10 pipes can be specified (including the default control pipe)
- Programmable pipe configuration
- Any endpoint number can be assigned to pipes 1 to 9
- Transfer conditions for pipes are as follows:
  - Pipe 0: Control pipe (Default control pipe: DCP), 64-byte fixed single buffer
  - Pipes 1 and 2: Bulk or isochronous pipe, continuous transfer mode, programmable buffer size (Double buffer can be specified up to 2 KB)
  - Pipes 3 to 5: Bulk pipe, continuous transfer mode, programmable buffer size (Double buffer can be specified up to 2 KB)
  - Pipes 6 to 9: Interrupt pipe, 64-byte fixed single buffer

(6) Features as the host controller
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) supported
- Communicates with multiple peripherals via a hub (tier 1)
- Automatically responds to the reset handshake
- Automatically schedules to transmit SOF, and packets
- Specifies the interval on the isochronous and interrupt transfers

(7) Features as the function controller

- High-speed (480 Mbps), and full-speed (12 Mbps) supported
- Automatically detects the high-speed or full-speed operation by replying to the reset handshake
- Manages stage on the Control transfer
- Manages the device state
- Automatically responds to the SET_ADDRESS request
- NAK response interrupt (NRDY)
- SOF Tracking and Recovery

(8) Other features

- Completes transfer by counting transactions
- Delays the BRDY interrupt event notification timing (BFRE)
- Automatically clears the buffer memory after reading data from the pipe specified by the DnFIFO (n = 0, 1) port (DCLRM)
- Specifies NAK to the response PID by the end of transfer (SHTNAK)

2.2 Enumeration

Enumeration is the activity that the USB host detects a device, assigns an address, collects the descriptor information and configures the detected device. This section describes the configuration required to enumerate with the USB host.

Table 1 lists the configuration required to enumerate with the USB host. Figure 1 shows the enumeration sequence.

Table 1 Configuration to Enumerate with the USB Host

Item	Description
Initialization	Initializes the USB module as a USB function
USB interrupt	Analyzes causes of interrupts occurred in the USB module and handles the interrupts according to the cause
Response to request	Responds to requests required to enumerate with the USB host

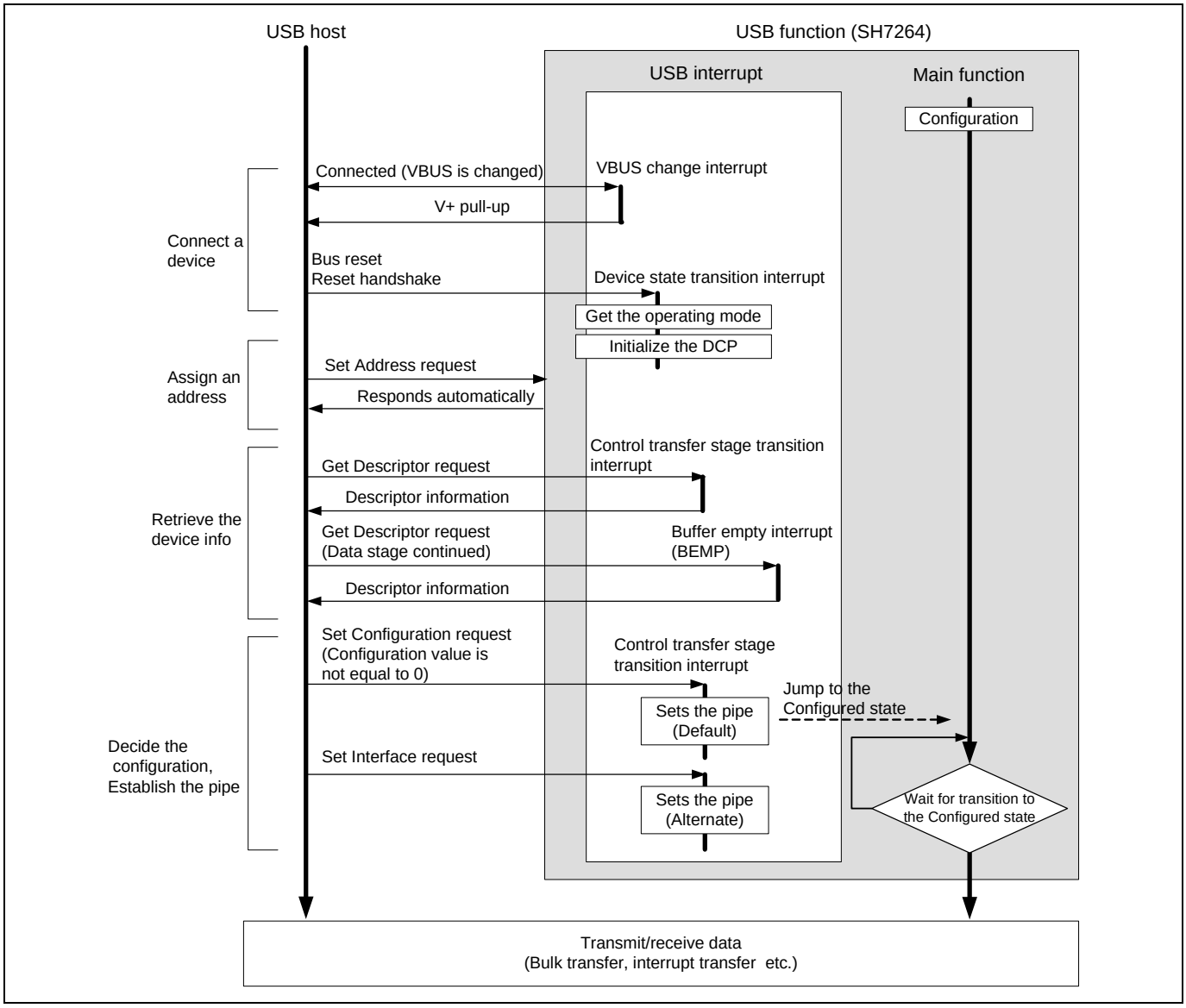


Figure 1 Enumeration Sequence

2.2.1 Configuration

Figure 2 shows the flow chart of configuration to enumerate as the USB function.

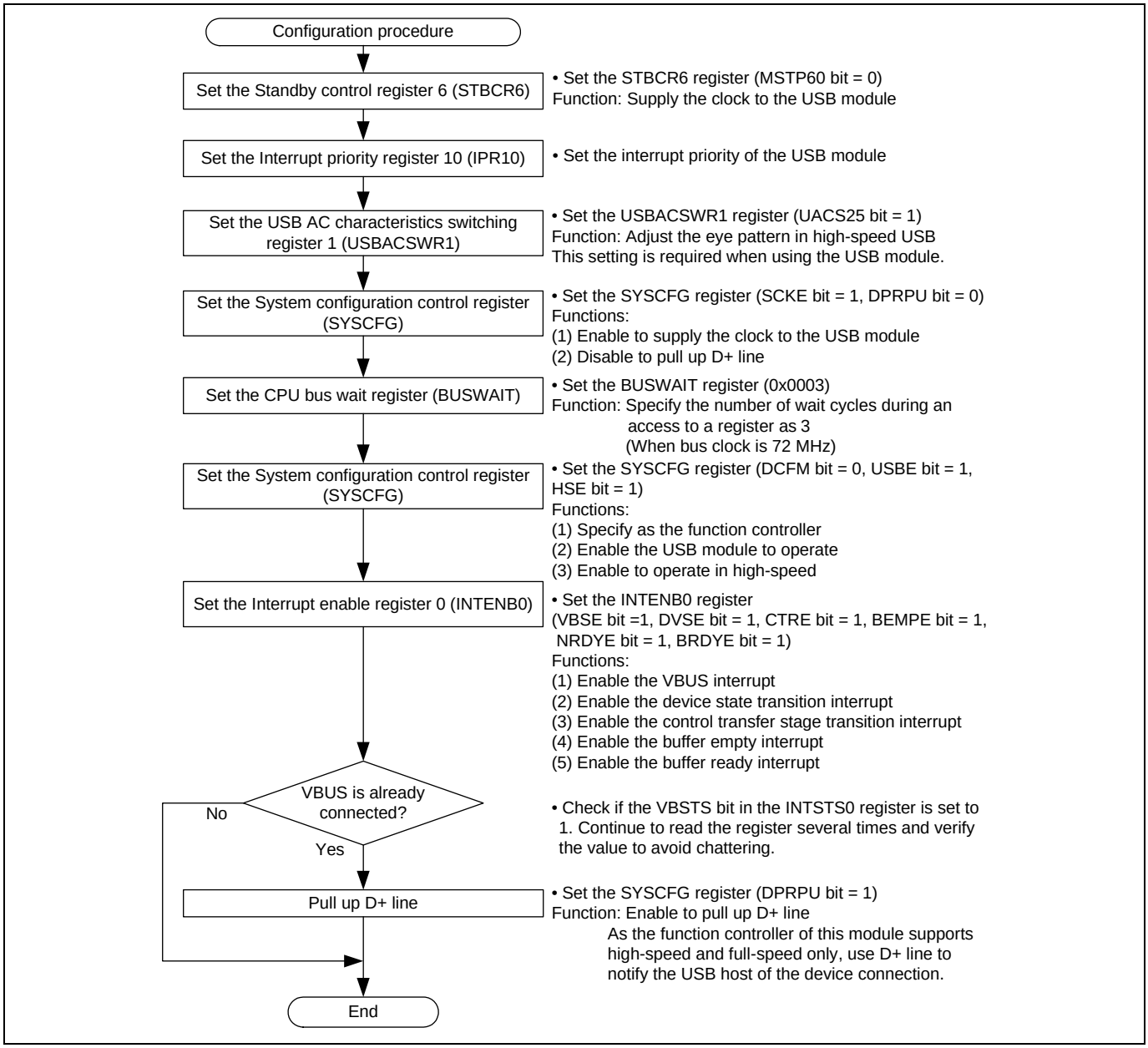


Figure 2 Configuration Flow Chart

2.2.2 USB Interrupts

Table 2 lists USB interrupts occur when enumerating with the USB host.

Table 2 USB Interrupts Occur in Enumeration

Interrupt Name	Cause
VBUS interrupt	When the VBUS state change is detected
Device state transition interrupt	When the device state transition is detected
Control transfer stage transition interrupt	When the control transfer stage transition is detected
Buffer state change (BEMP) interrupt	When all data in the buffer memory is transferred and the buffer is empty
Buffer state change (BRDY) interrupt	When the buffer is ready to be read or written (This interrupt occurs when the buffer is ready to be read in the control transfer)

(1) VBUS interrupt

Figure 3 shows the flow chart of the VBUS interrupt. VBUS interrupt detects the connection or disconnection of the VBUS pin, and pull up D+ line.

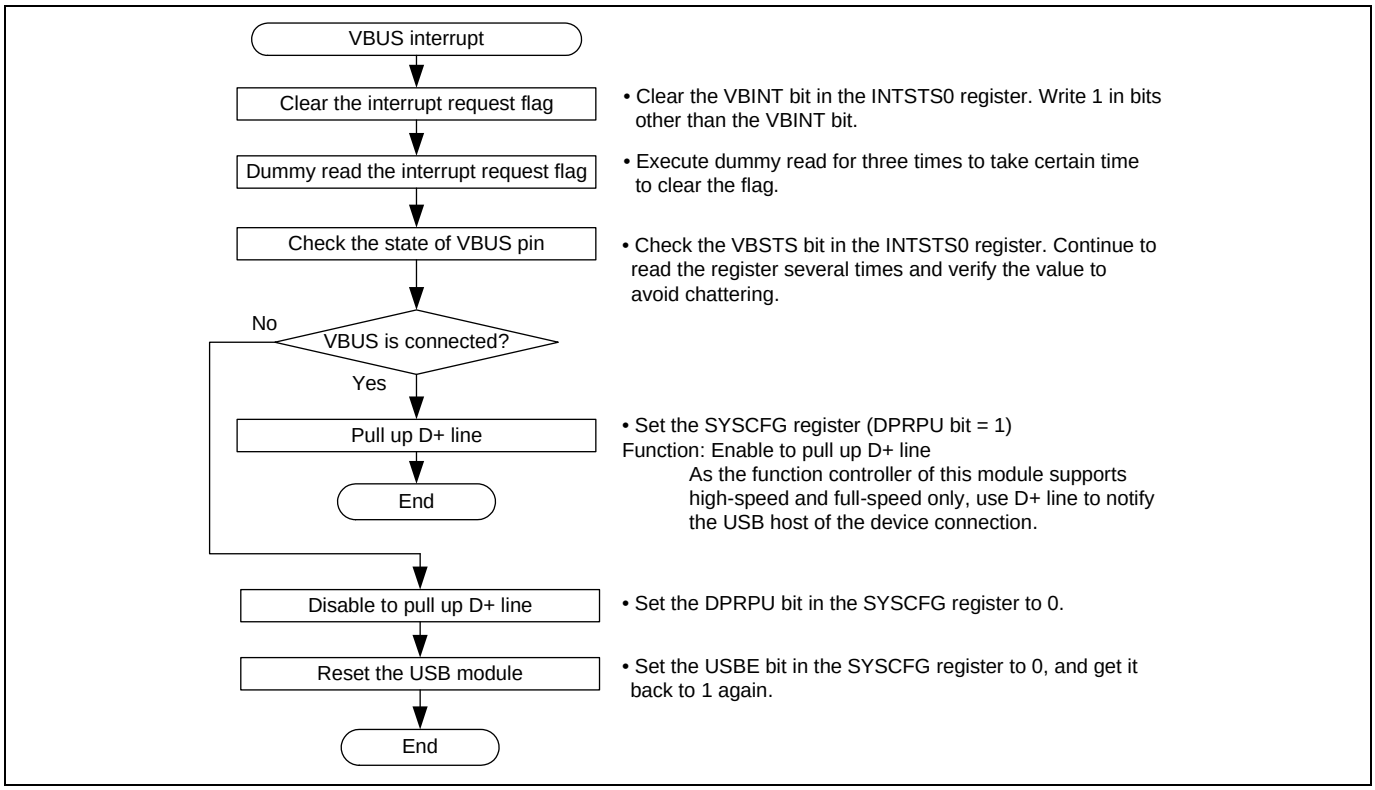
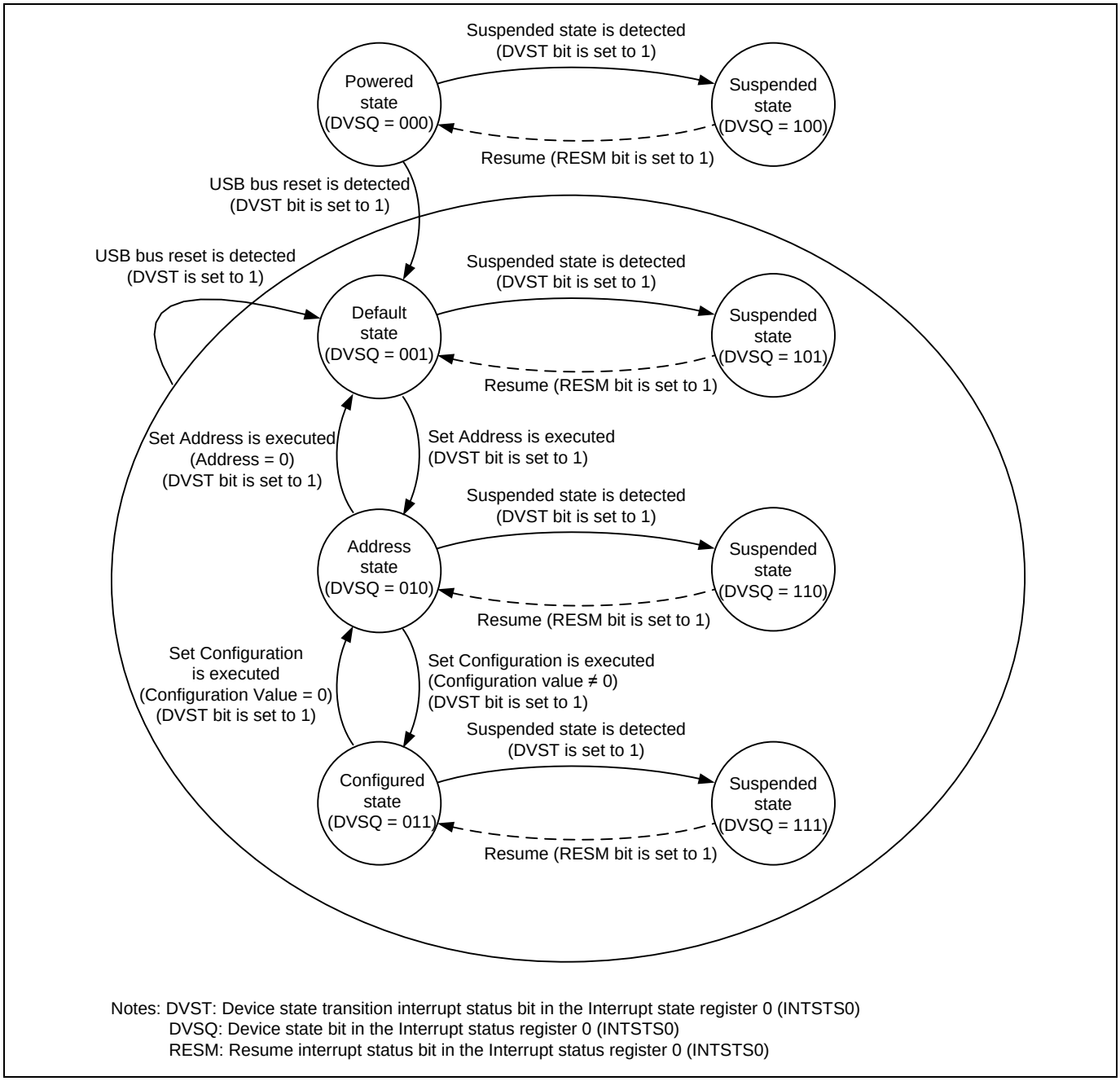


Figure 3 VBUS Interrupt Flow Chart

(2) Device State Transition

Figure 4 shows the device state transition. The state of a device transitions from the powered state to the configured state by an enumeration. As the USB module detects the transition of the device state by the interrupt, it executes the required process in each state.



Notes: DVST: Device state transition interrupt status bit in the Interrupt state register 0 (INTSTS0)
DVSQ: Device state bit in the Interrupt status register 0 (INTSTS0)
RESM: Resume interrupt status bit in the Interrupt status register 0 (INTSTS0)

Figure 4 Device State Transition

Figure 5 shows the flow chart of the device state transition interrupt. This application initializes the descriptor data and the default control pipe (DCP) when the device transitions to the default state. For more details on descriptors, refer to 2.3 Descriptors.

Figure 6 shows the flow chart of initializing the DCP. For more details on DCP, refer to 2.4 Control Transfer.

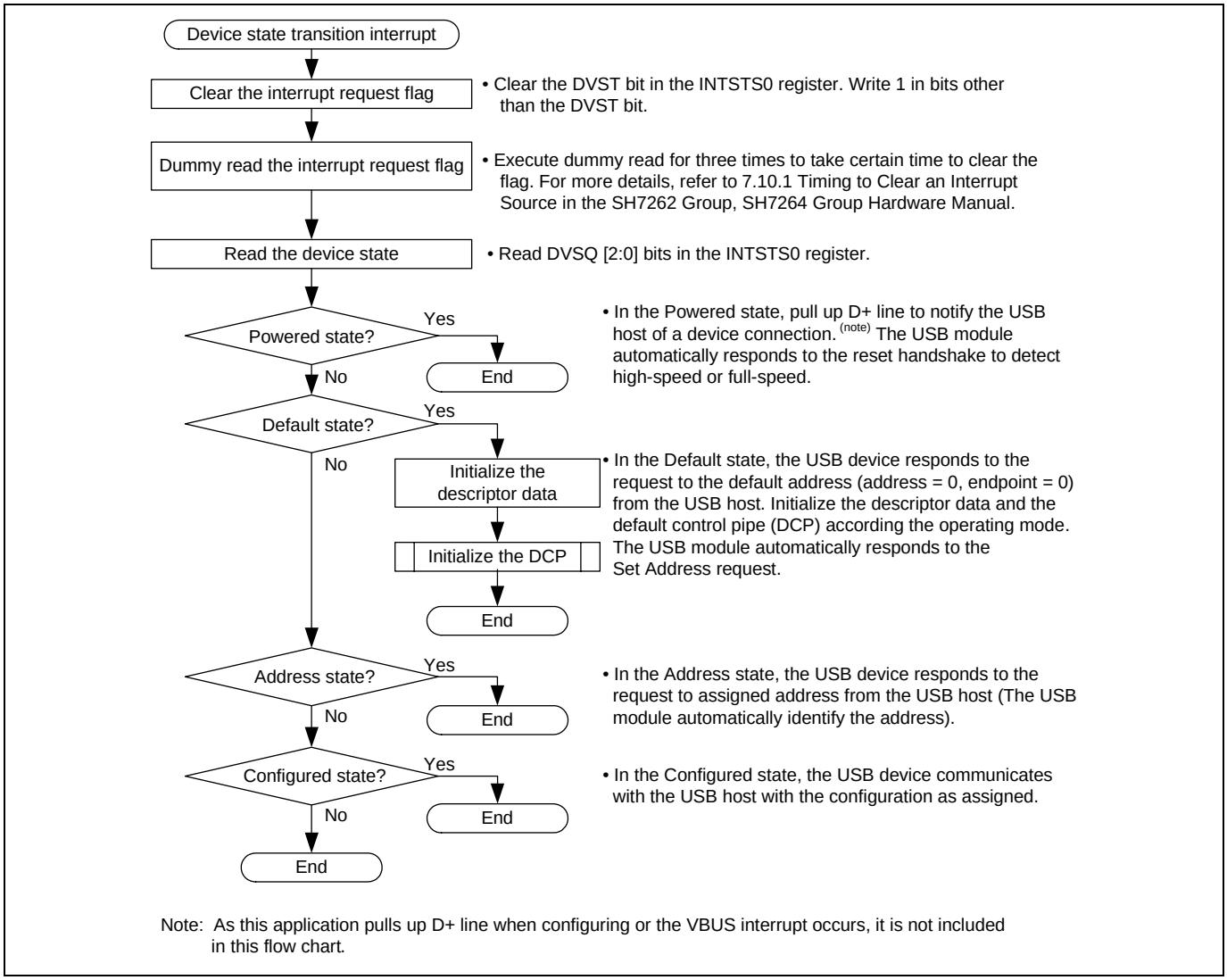


Figure 5 Device State Transition Interrupt Flow Chart

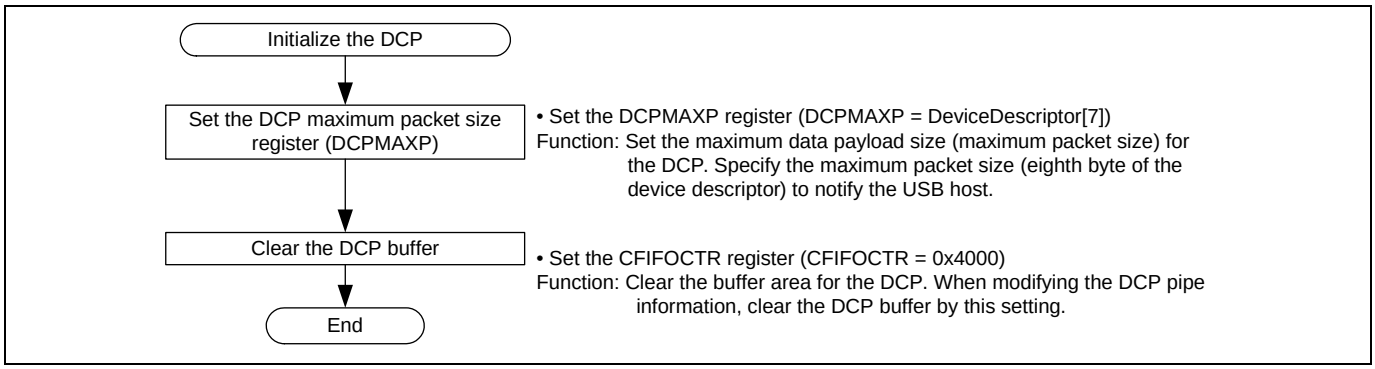


Figure 6 DCP Initialization Flow Chart

(3) Control transfer stage transition

Figure 7 shows the control transfer stage transition. As the USB module detects the state transition in the control transfer by the interrupt, it executes the required process in each state. For more details on the control transfer, refer to 2.4 Control Transfer.

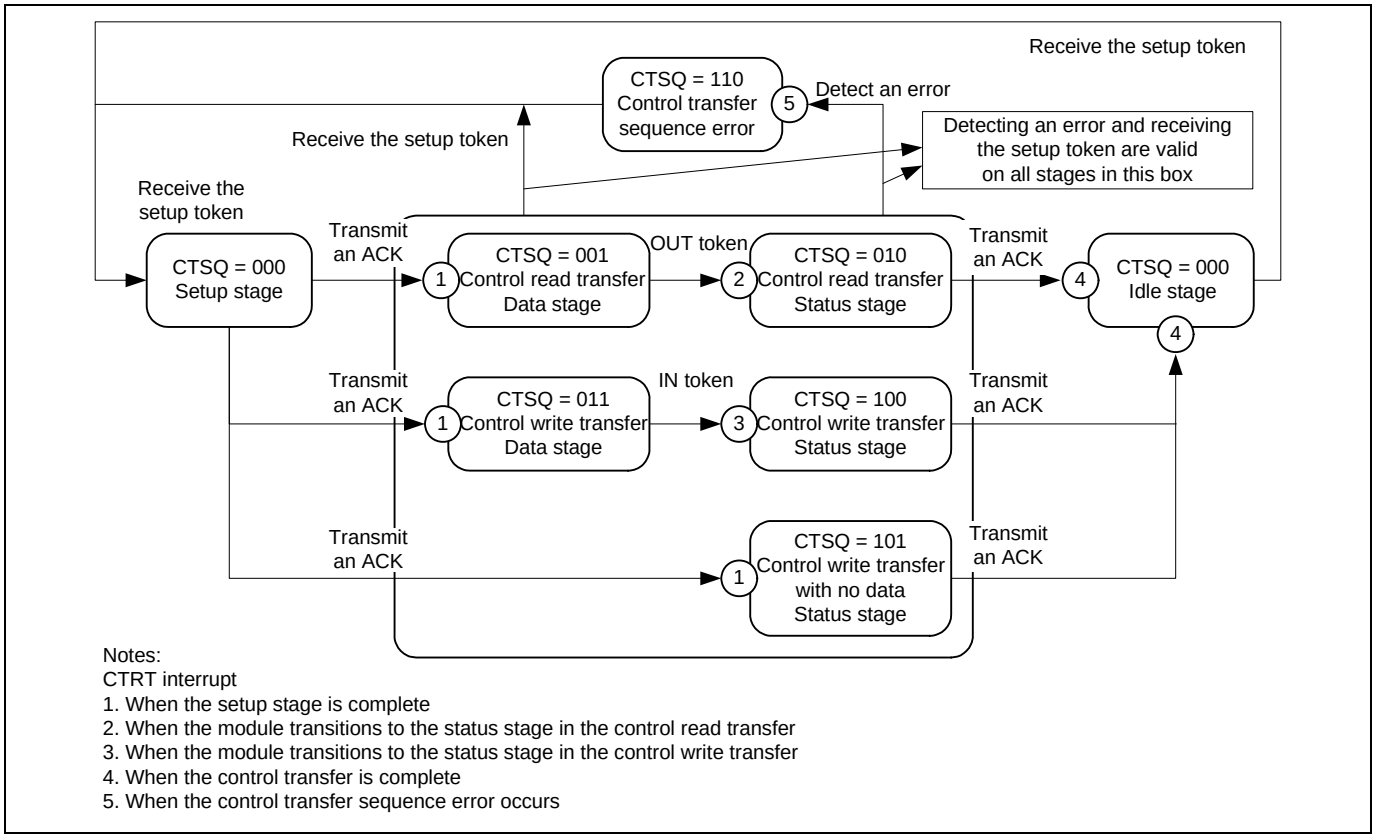


Figure 7 Control Transfer State Transition

Figure 8 shows the flow chart of the control transfer transition interrupt. This application uses the control read transfer and control write transfer with no data only. For more details on request, refer to 2.2.3 Response to Requests.

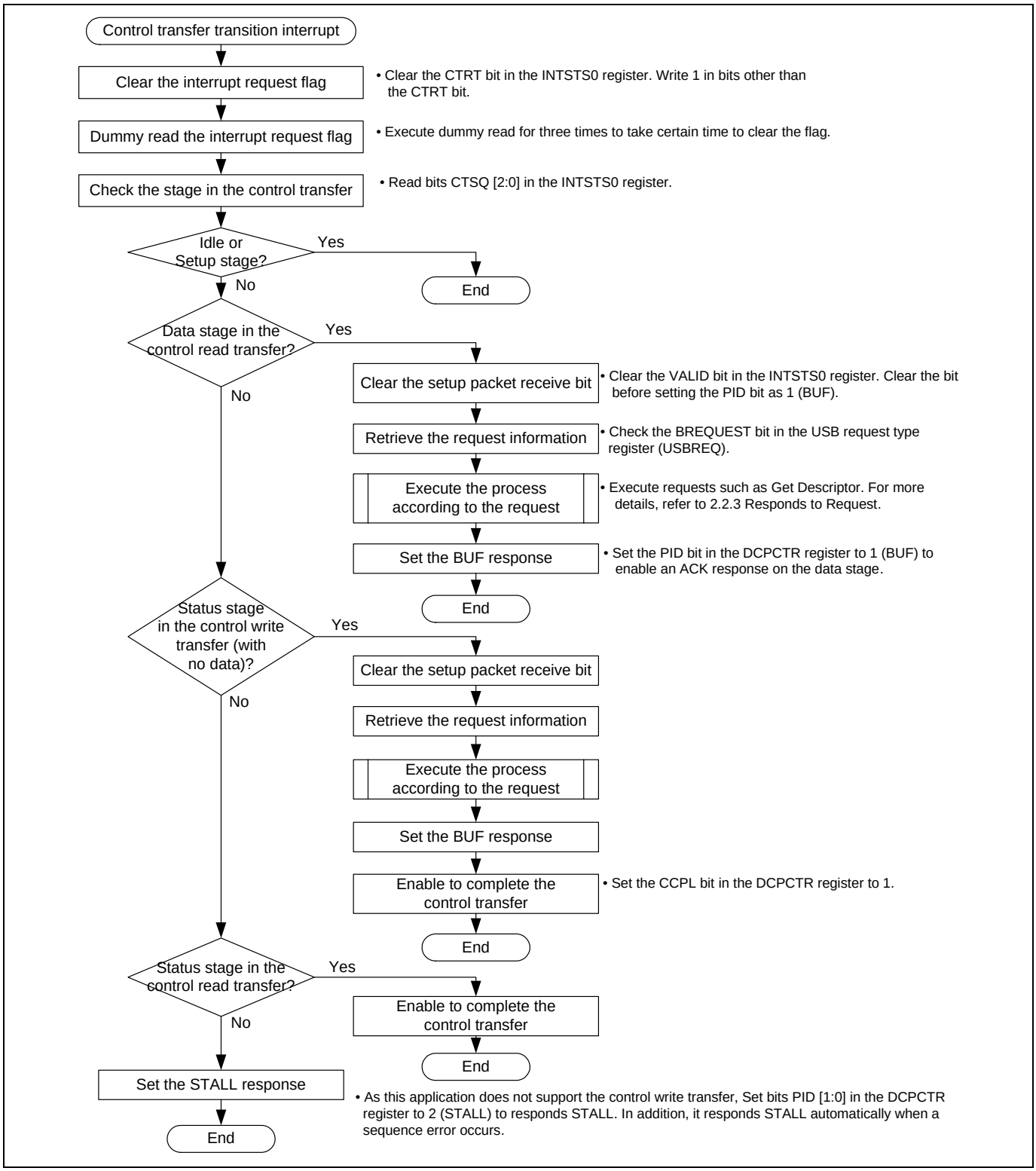


Figure 8 Control Transfer Transition Interrupt Flow Chart

(4) Buffer state is changed (BEMP)

Figure 9 shows the flow chart of the BEMP interrupt. This application uses the BEMP interrupt in the control read transfer. As this interrupt occurs when all data written in the buffer for DCP is transmitted, it transmits the remaining data. When the size of the transmit data is multiples of the MaxPacketSize, this interrupt transmits data first, and zero-length packet. For details to start the control read transfer, refer to 2.4.2 Control Read Transfer.

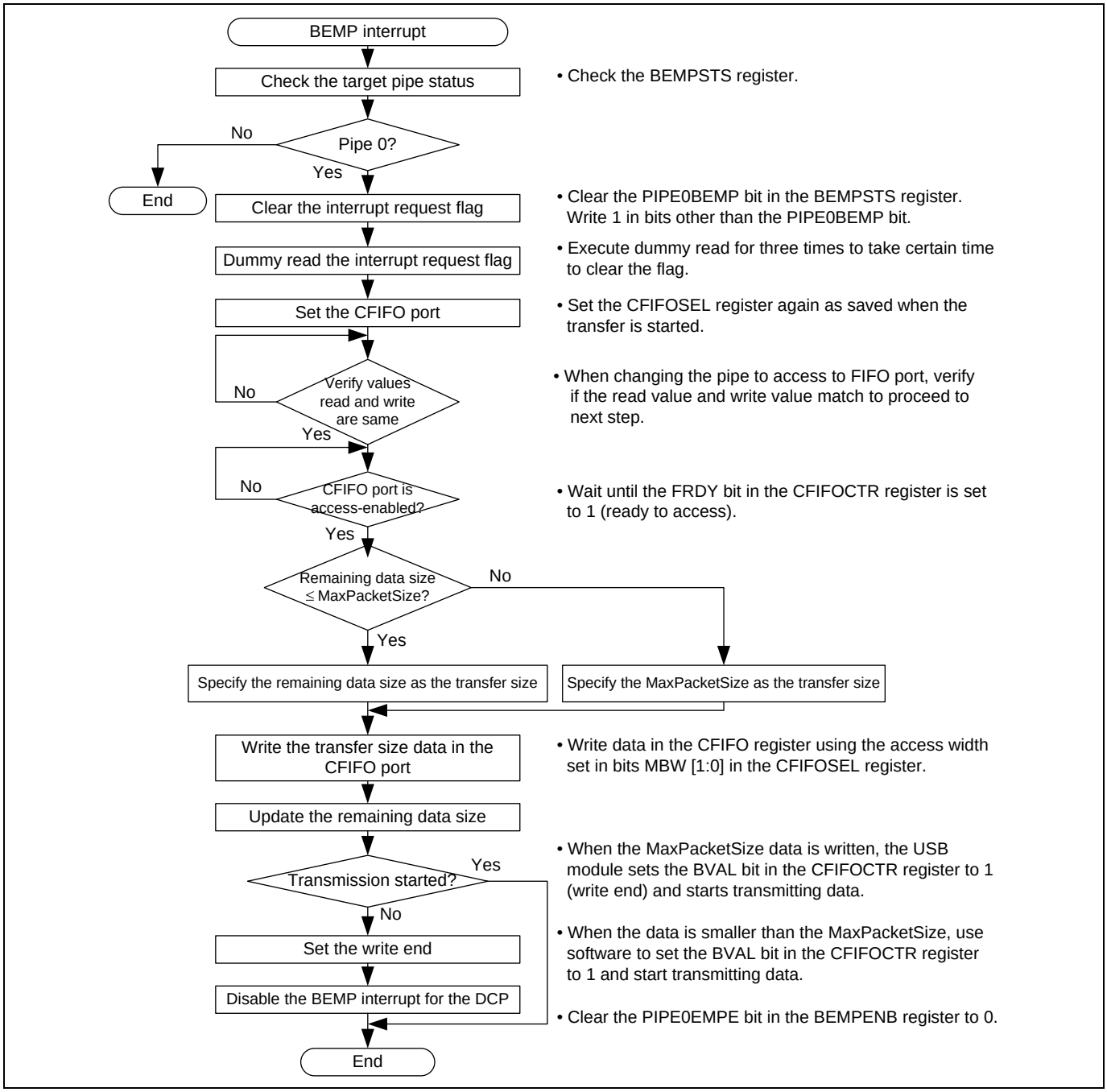


Figure 9 BEMP Interrupt Flow Chart

(5) Buffer state is changed (BRDY)
The BRDY interrupt detects a buffer is in read- or write-enabled state. This interrupt is used when receiving data from the USB host. As this application does not use the control write transfer, the BRDY interrupt is not used.

2.2.3 Response to Requests

Table 3 lists the USB standard requests used in this application. Request is a command transmitted from the USB host to the USB function, which is controlled by the control transfer. For more details on the control transfer, refer to 2.4 Control Transfer.

Table 3 USB Standard Requests Used in This Application

Request	Description	Direction to access on the data stage
Get Descriptor	Reads the descriptor	USB function to USB host (Control read transfer)
Set Address	Specifies the device address	No data
Set Configuration	Sets the device configuration	No data
Set Interface	Selects an alternate setting for the specified interface	No data

Figure 10 shows the request fields used in this application. Values in the request fields are stored in the USB module registers.

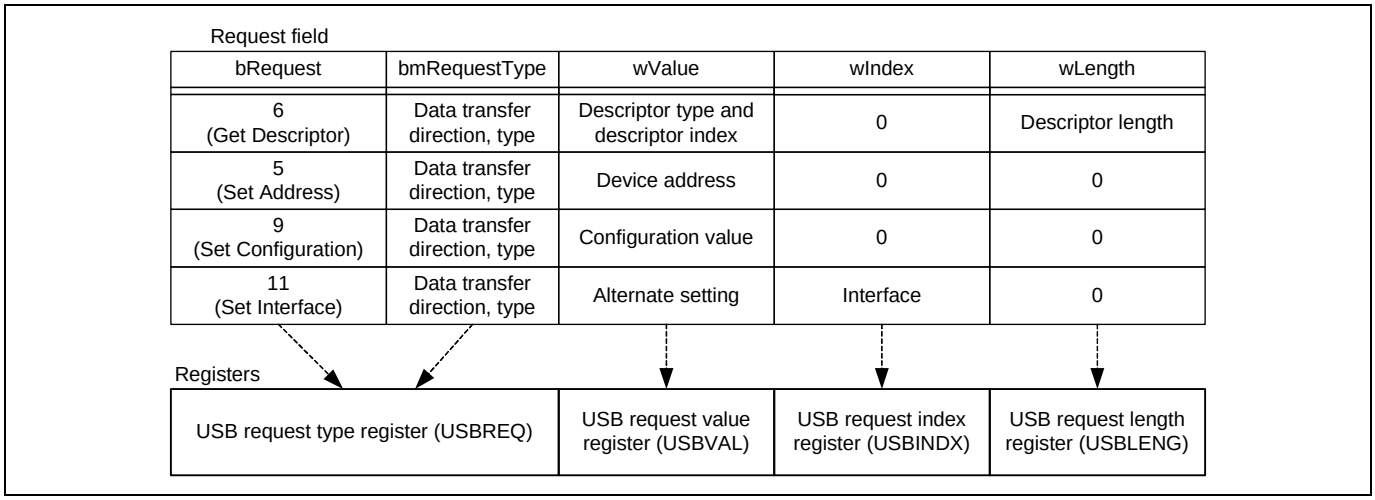


Figure 10 Request Fields Used in This Application

Figure 11 to Figure 14 show flow charts of major standard requests used in this application. Each request is executed by the control transfer stage transition interrupt. For the flow chart of the control transfer stage transition interrupt, refer to Figure 8.

Get Descriptor executes the control read transfer to transmit the specific descriptor information to the USB host. For details to start the control read transfer, refer to 2.4.2 Control Read Transfer.

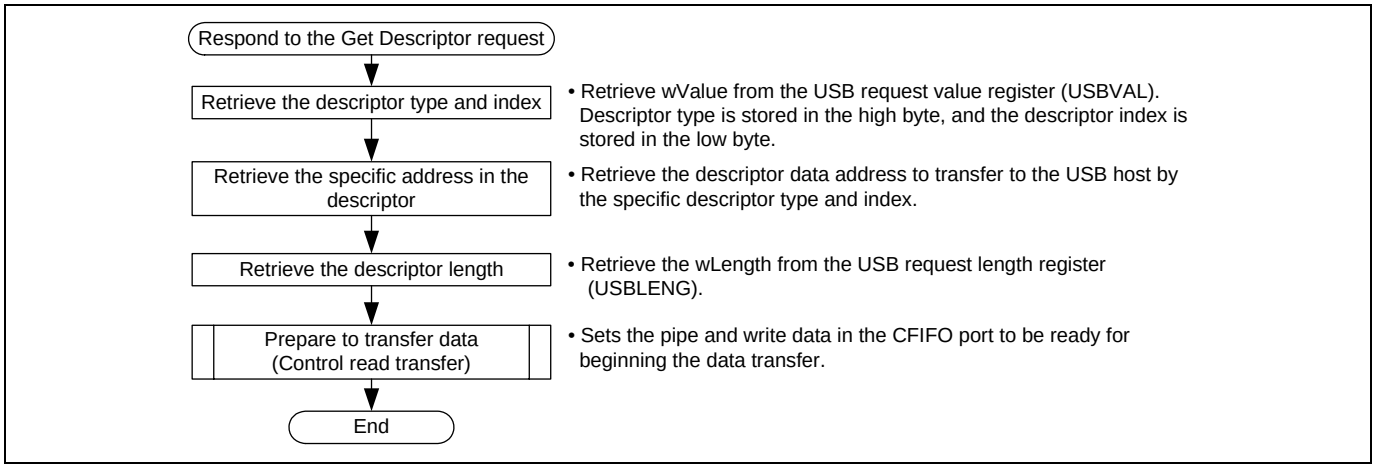


Figure 11 Flow Chart of Get Descriptor Request

As the USB module automatically responds to the Set Address request shown in Figure 12, developing the response process by software is not required.

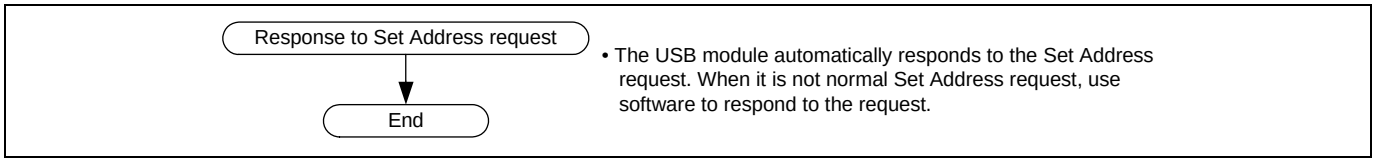


Figure 12 Flow Chart of Set Address Request

The response to the Set Configuration request shown in Figure 13 initializes pipe and buffer to communicate with the USB host subsequently by the specified configuration value (configuration index value). No data is transferred on the Data stage. For more details on configuration, refer to 2.3 Descriptors.

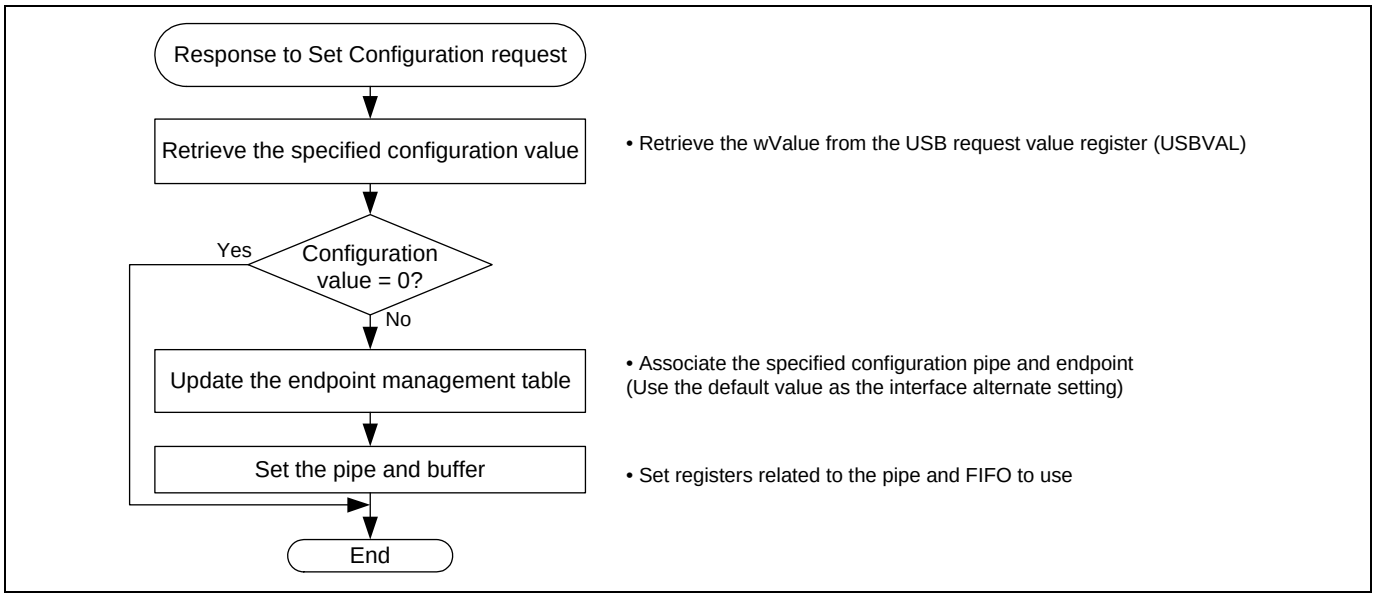


Figure 13 Flow Chart of Set Configuration Request

The response to the Set Interface request shown in Figure 14 reconfigures the pipe and buffer to transfer the specified interface by the alternate setting. No data is transferred on the Data stage. For more details on interface, refer to 2.3 Descriptors.

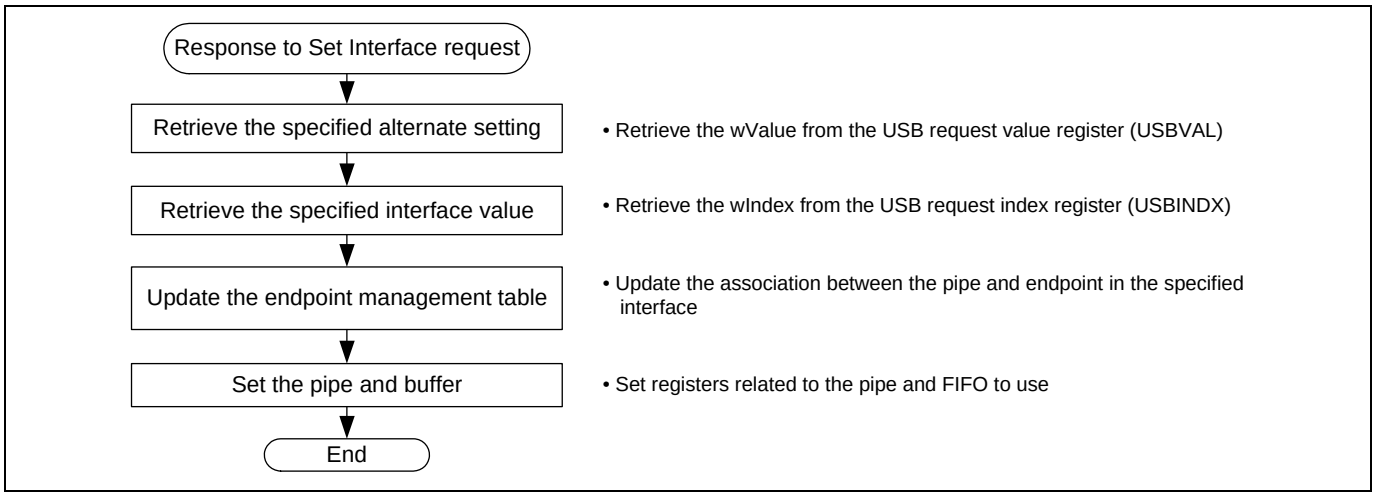


Figure 14 Flow Chart of Set Interface Request

2.3 Descriptors

Table 4 lists the overview of descriptors. A descriptor is the data that the USB host identifies the USB function module attribute correctly. The USB function module defines the descriptor statically, and responds to the Get Descriptor reuqest from the USB host to notify the descriptor information.

Table 4 Descriptor Overview

Descriptor Name	Description	Remarks
Device Descriptor	Defines the device attribute such as the USB version number, maximum packet size in endpoint 0, and vendor ID	
Configuration Descriptor	Defines the configuration (1) attribute. Multiple configuration descriptors can be defined in a device.	Configuration to use is specified by the Set Configuration request.
Interface Descriptor	Defines the interface (2) attribute. Multiple interface descriptors can be defined in a device. One or more alternate settings can be defined with a single interface.	Alternate setting is specified by the Set Interface request.
Endpoint Descriptor	Defines the endpoint (3) attribute. Multiple endpoint descriptors can be defined per alternate setting of the interface.	
String Descriptor	Stores the strings	
Device_Qualifier Descriptor	Defines operating mode other than the current operating mode. When the device is currently operating at high-speed, it defines the setting for high-speed and vice-versa.	At least one device_qualifier descriptor is required when enabling the operation in high-speed
Other_Speed_Configuration Descriptor	Defines operating mode other than the current operating mode. When the device is currently operating at high-speed, it defines the setting for high-speed and vice-versa.	At least one device_qualifier descriptor is required when enabling the operation in high-speed

Notes 1. Configuration is a set of interfaces. Normally, an interface is defined as not to use the same endpoint (other than endpoint 0) with other interface. However, already-defined endpoint can be assigned again to the interface when the configuration is newly defined.

2. Interface is a set of endpoints. Configuring the device driver in interfaces simplifies to manage software. Multiple alternate settings can be defined for interface to select endpoint parameter such as the maximum transfer size.
3. An endpoint is the logic number to identify the transfer type. When using multiple transfer types such as the bulk transfer and interrupt transfer to associate endpoints with each transfer type.

Figure 15 shows the descriptor relationships.

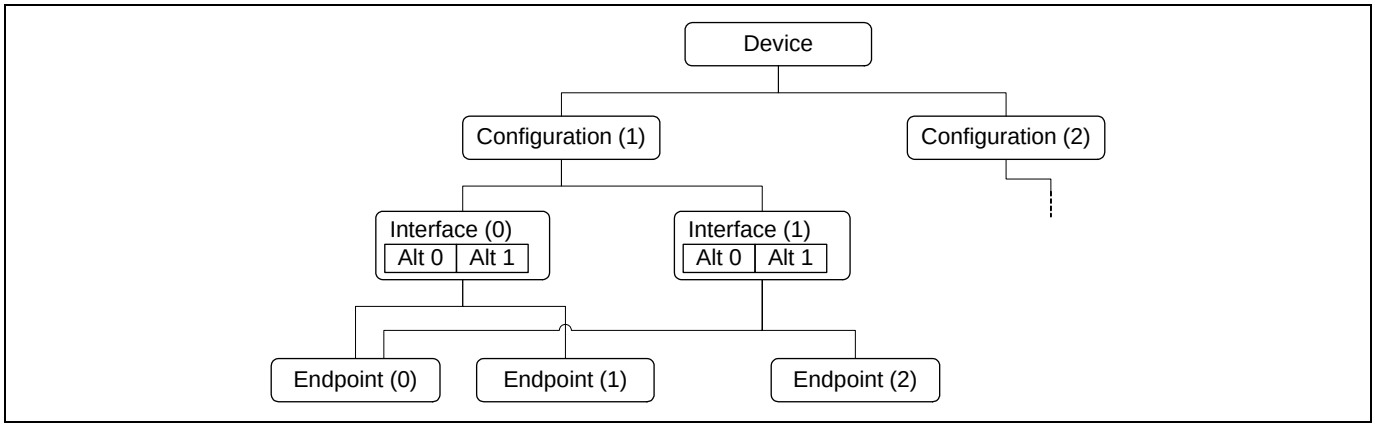


Figure 15 Descriptor Relationships

Figure 16 shows the descriptor data structure image. For more details, refer to the USB 2.0 Specifications listed in 3 References.

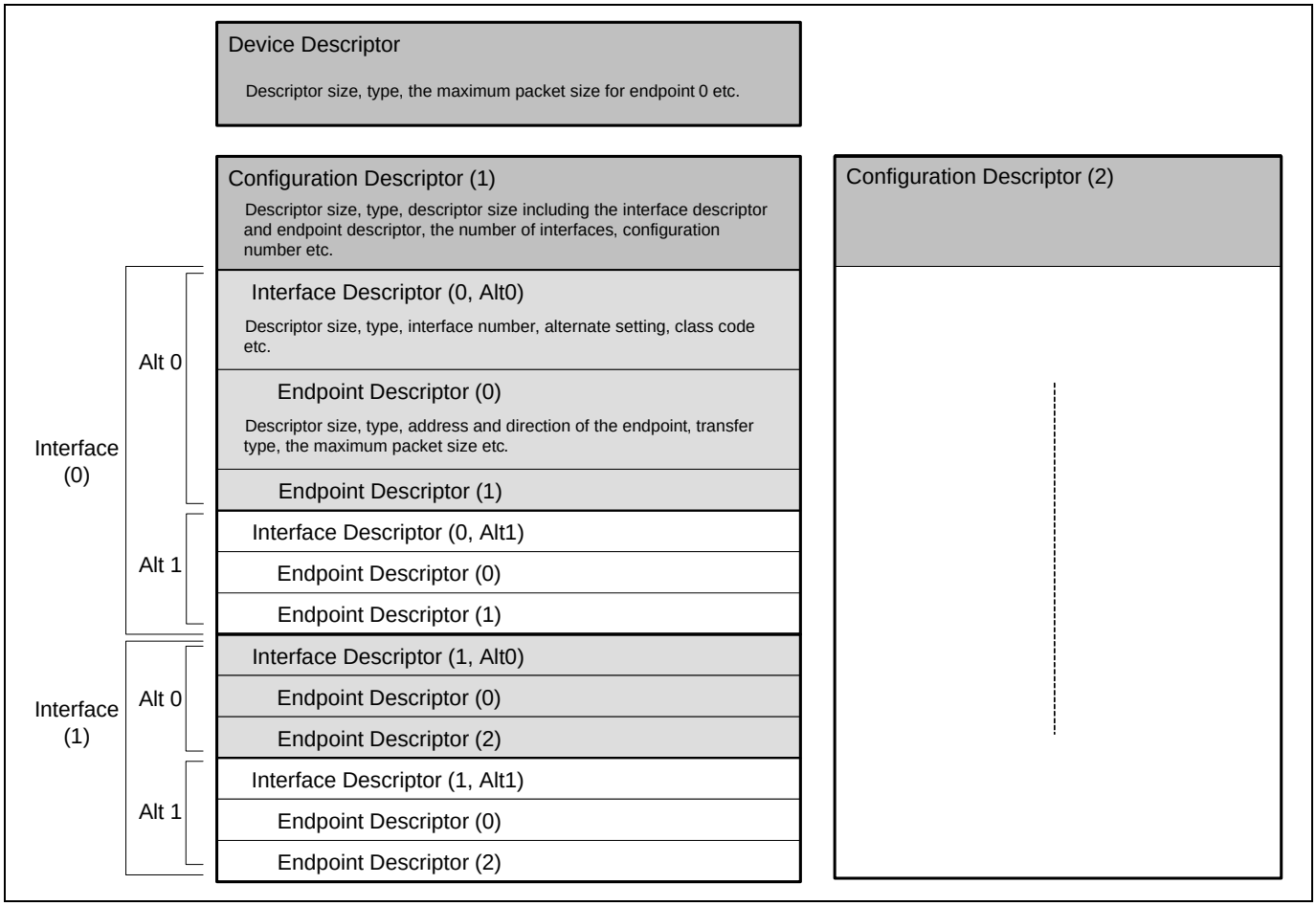


Figure 16 Descriptor Data Structure Image

2.4 Control Transfer

Control transfer is a transfer type to transmit requests and responds to requests using endpoint 0. The USB module executes the control transfer using the default control pipe (DCP) and DCP-dedicated buffer.

2.4.1 Operation Sequence

Control transfer is composed of three stages (setup stage, data stage, and status stage), and each stage is independent transaction. The USB host transmits a request from the USB host on the setup stage. The USB host transfers data upon request. And the USB host checks if the request ends normally.

Figure 17 shows the sequence diagram of the control read transfer. Control read transfer is to transmit data from the USB function to the USB host on Data stage.

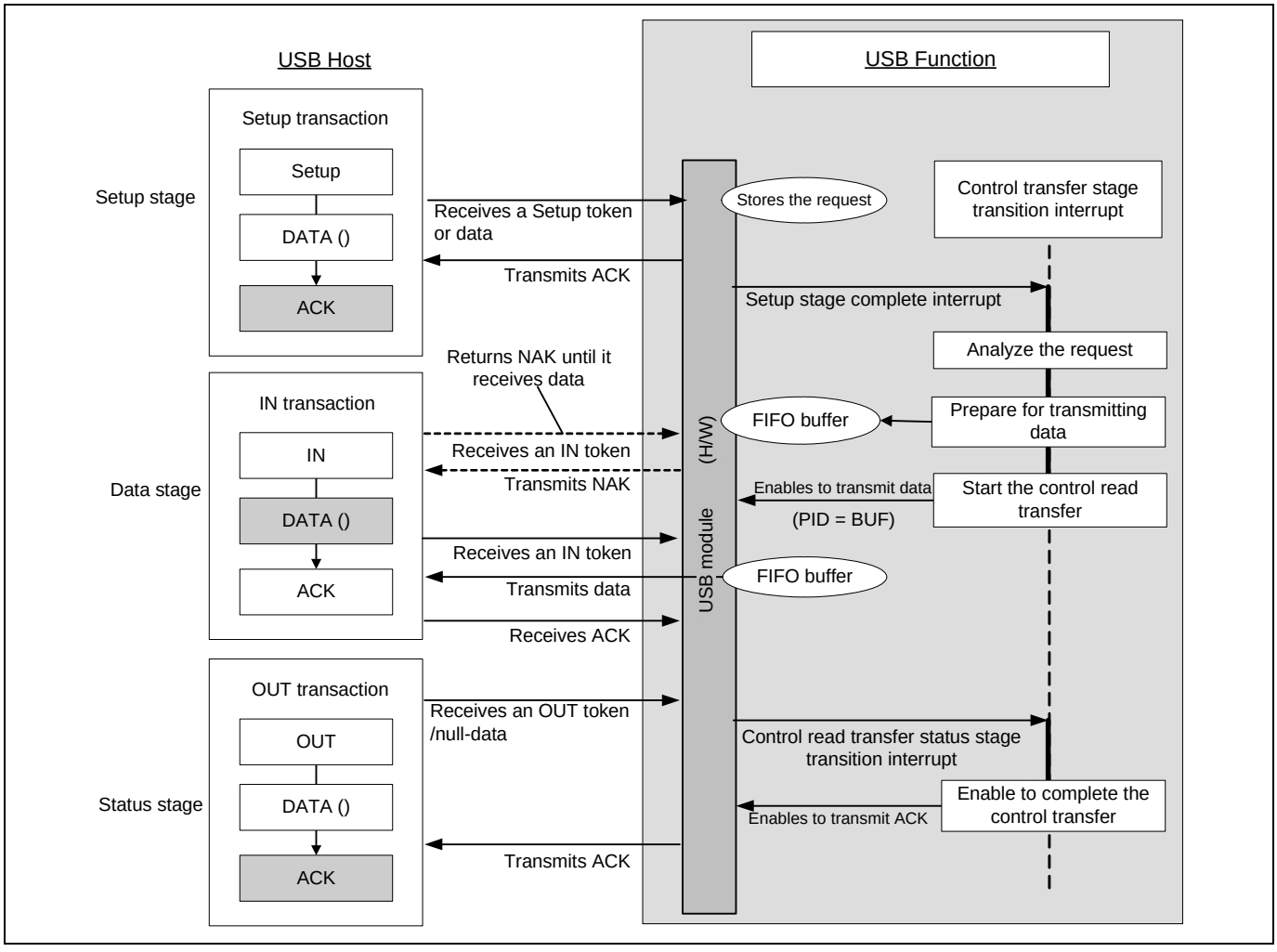


Figure 17 Control Read Transfer Sequence

Figure 18 shows the sequence diagram of the control write transfer. Control write transfer is to transfer data from the USB host to the USB function on Data stage.

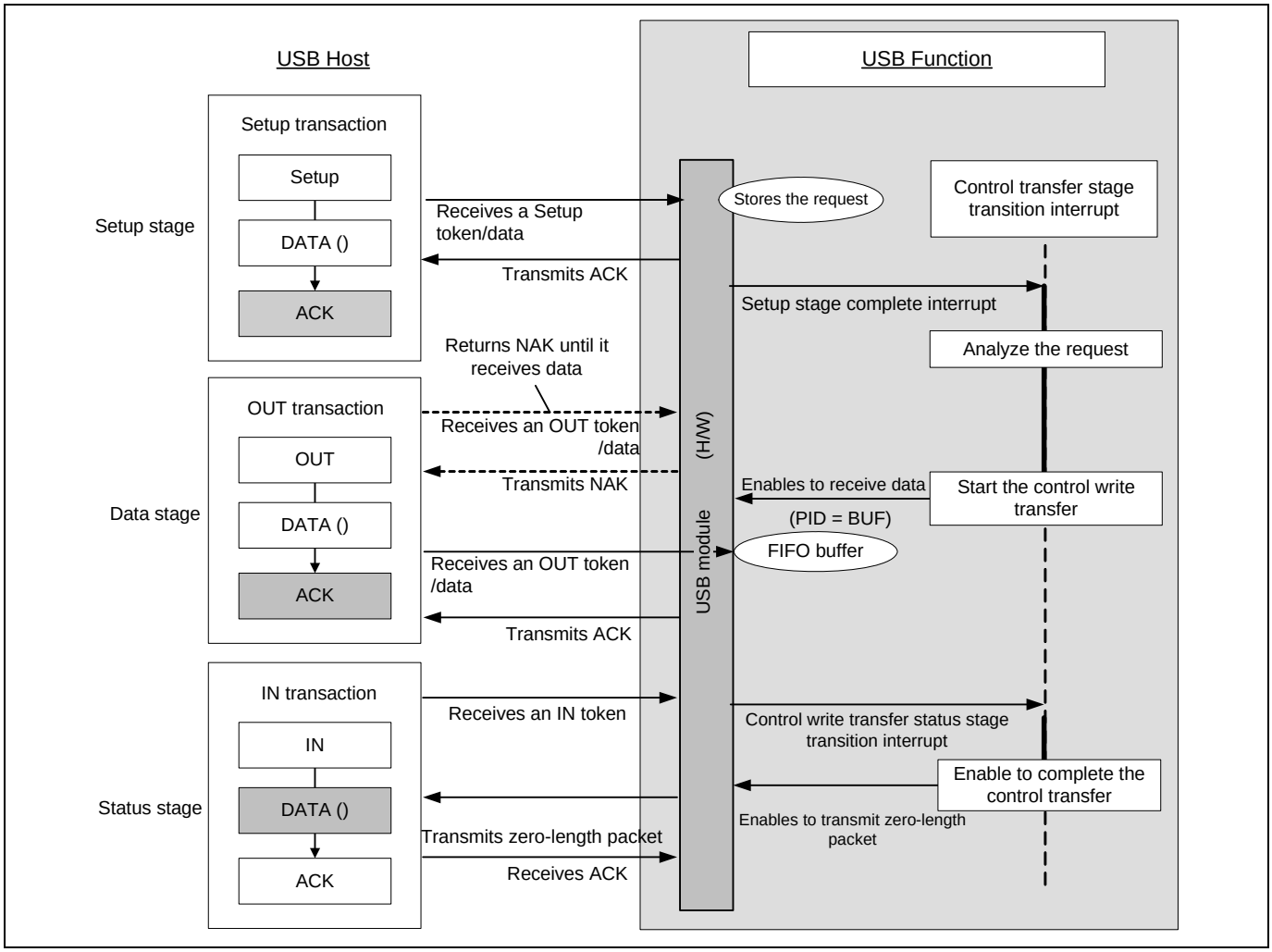


Figure 18 Control Write Transfer Sequence

Figure 19 shows the sequence diagram of the control write transfer with no data.

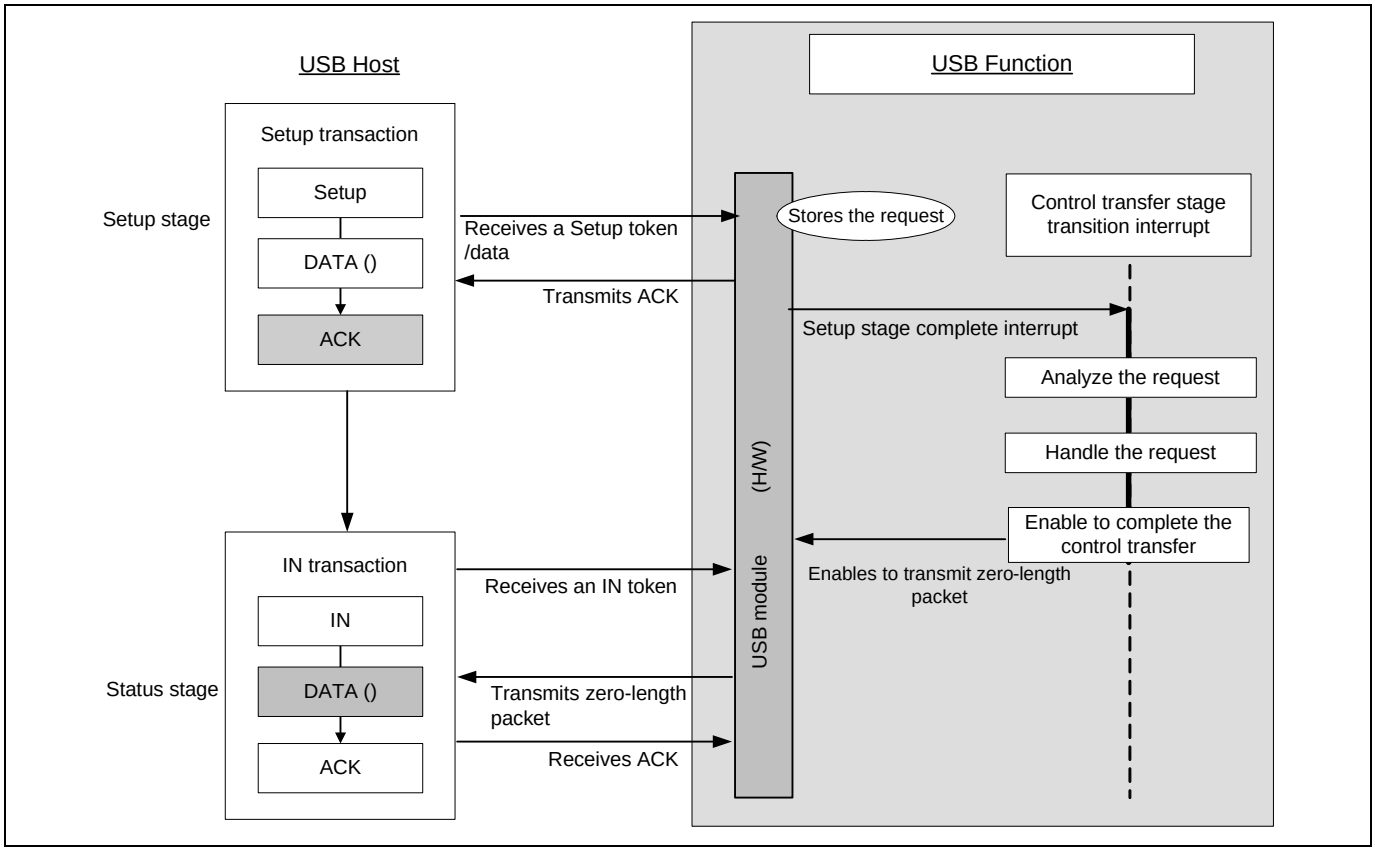


Figure 19 No-Data Control Write Transfer Sequence

2.4.2 Control Read Transfer

Figure 20 shows the flow chart of initiating the Control read transfer. Initiate the data transfer by this process, and transfer the remaining data by the BEMP interrupt.

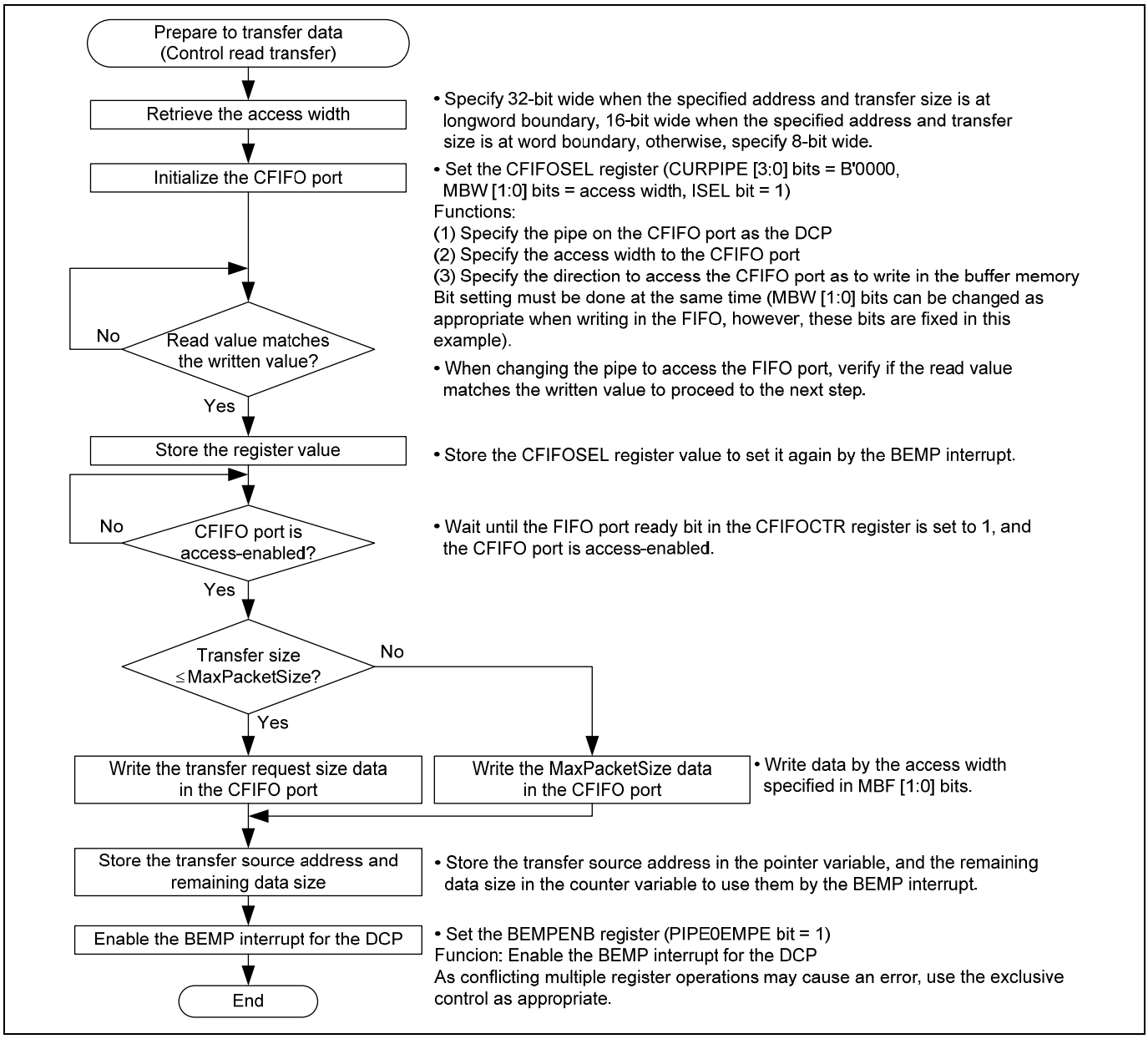


Figure 20 Flow Chart of Initiating the Control Read Transfer

3. References

- Software Manual
  SH-2A/SH-2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas website.

- USB 2.0 Specifications
  Universal Serial Bus Specification Revision 2.00
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