IGBT

Load Short Measurement Method

About this document

This application notes mainly to show the measurement method of load short circuit for IGBT.

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1. Introduction

1.1 Overview

The short circuit mechanism can be categorized into two types: Arm Short and Load Short. The distinction between these lies in where the short occurs, Arm Short refers to a short circuit internally within the inverter, while Load Short occurs at the output.

By conducting Load Short Circuit (LSC) measurements on IGBTs, engineers can evaluate their performance and robustness under such conditions. These tests are crucial for assessing factors like switching speed, current handling capabilities, and effectiveness of protection features. Additionally, load short-circuit testing helps identify and address issues such as excessive power dissipation, thermal stress, and potential failure modes, ensuring the reliability and durability of the IGBTs in practical applications.

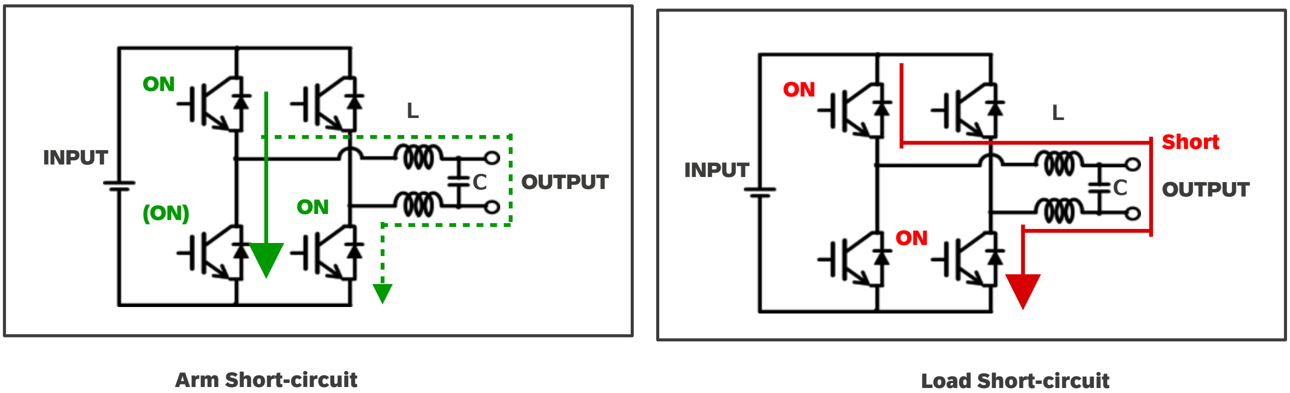

Figure 1-1 Short Circuit Mechanism

1.2 Arm Short-circuit

In a DC short circuit condition, current flows directly through the IGBT from the high side to the low side when both are turned on simultaneously. Figure 1.1. on the left-hand side illustrates the current flow diagram (Arm Short-circuit diagram).

1.2.1 Reason and counter measure

There are several reasons why short circuits occur. The table below outlines the main causes that can be prevented with appropriate margin and confirmation in the design.

Problem 1: Hi-side and Lo-side receiving ON signals simultaneously due to control IC miss operation.

Noise can disrupt the operation of the control IC and cause the simultaneous activation signals being sent to both the high-side and low-side components. Investigating and addressing the root cause of this miss operation, such as enhancing noise immunity or fine-tuning signal timing, can substantially lower the risk of short circuits occurring.

Problem 2: Hi-side and Lo-side switching times overlap.

When the switching times of the high-side and low-side IGBTs overlap, it can lead to short circuits or other unintended consequences. To prevent this, adjusting the deadtime between the switching of the IGBTs ensures that there is a sufficient delay between turning off one IGBT and turning on the other. Additionally, reducing the gate resistor (RG) helps to speed up the switching times of the IGBTs, minimizing the overlap period and improving the overall performance and reliability of the circuit.

Problem 3: High dv/dt causes an increase in VGE (gate-emitter voltage) and unintended turn-on of the IGBT.

High dv/dt conditions can lead to rapid changes in VGE, potentially triggering unintended turn-on of the IGBT. Applying a gate reverse bias during critical transitions helps to stabilize VGE and prevent unintended switching. Additionally, increasing the gate resistor (RG) slows down the switching times of the IGBT, which reduces the likelihood of dv/dt-induced turn-on, enhancing overall circuit reliability.

1.3 Load Short Circuit (LSC)

In an output short circuit, there is an unintended electrical path through the IGBT when it is conducting, allowing a current higher than normal to flow. This can lead to a short circuit, as illustrated in Figure 1.1. on the right (LSC diagram).

Load shorts usually occur due to end-user mistakes, which makes prevention challenging for design engineers. However, it's crucial to protect against such incidents even if they occur. Below are two methods that can help secure the circuits from damage

1.3.1 Method 1: IGBT with short circuit withstand capability

The short circuit withstand capability, often expressed as time short circuit (t_{sc}), refers to a component's ability to endure or handle a short circuit safely, without damage or posing a safety hazard. It measures how well the device can withstand the high currents and heat generated during a short circuit event without failing or breaking down. This capability depends significantly on factors such as gate-emitter voltage, case temperature, and power supply voltage. These factors should be carefully considered during circuit design.

Essentially, the IGBT is capable of withstanding a short circuit for a few microseconds. If the protective circuitry reacts within this timeframe, it can safeguard the inverter circuit.

1.3.2 Method 2: Utilize output inductance characteristics

An inductor is a passive electronic component that temporarily stores energy in a magnetic field when electric current flows through its coil. This characteristic allows the inductor to extend the period over which the current rises to levels that could potentially damage the IGBT.

Further, additional protection circuit can be adding to prevent the IGBT destruction before current rises to the short circuit failure level.

The graph below illustrates the conceptual of t_{sc} with inductor, which depends on the defined value of inductance.

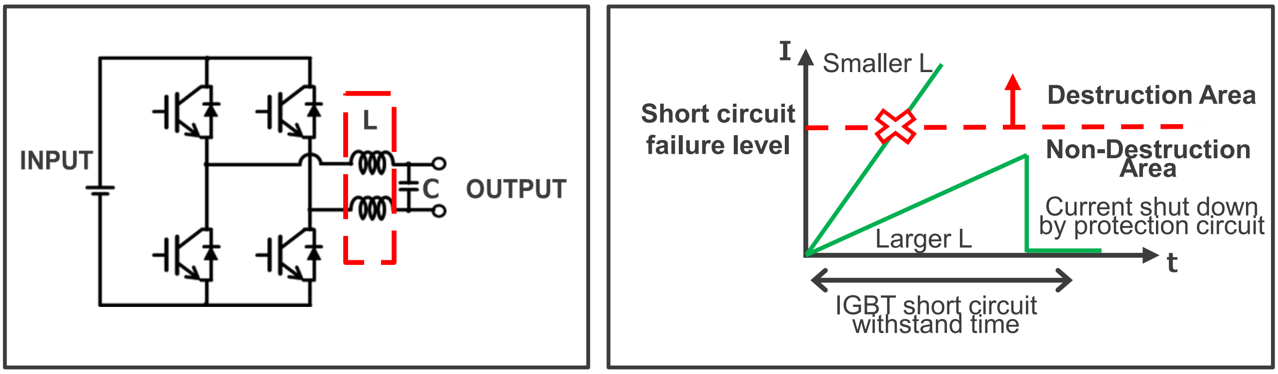

Figure 1-2 Conceptual of t_{sc} with inductor

1.4 LSC Test Methodology

Below is the circuit diagram that will be used to explain the procedure of the LSC test method.

Test condition: VCC = 600V, VGE = 15V, RG = 25 Ω, Tc = 25 °C

The forward bias voltage and pulse width (tsc) between the gate and emitter are adjusted to the specified values to turn the IGBT on. Subsequently, the IGBT is turned off by applying the specified reverse bias voltage between the gate and emitter. Changes in tsc are monitored during this process.

Next, the product undergoes validation to ensure the IGBT withstands the rated short circuit safe operating area, allowing observation of the IGBT's condition.

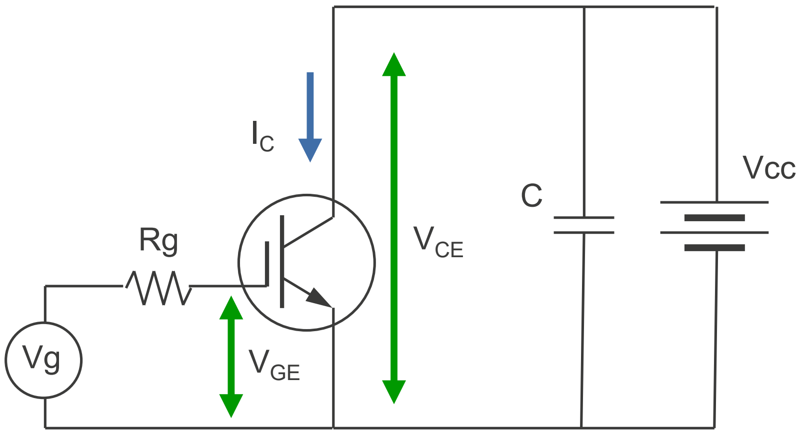

Figure 1-3 Circuit diagram for LSC

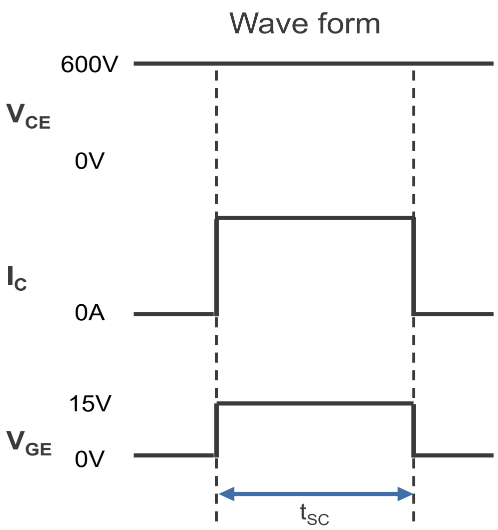

Figure 1-4 Theoretically Waveform

2. Output Result for LSC

2.1 Output Result comparison

Below are the output results of the LSC measurements captured from the oscilloscope. Figure 2.1.1. shows the output for a non-destruction result, while Figure 2.1.2. demonstrates a destruction result by configuring with the additional condition such as t_{sc}, RG and snubber circuit.

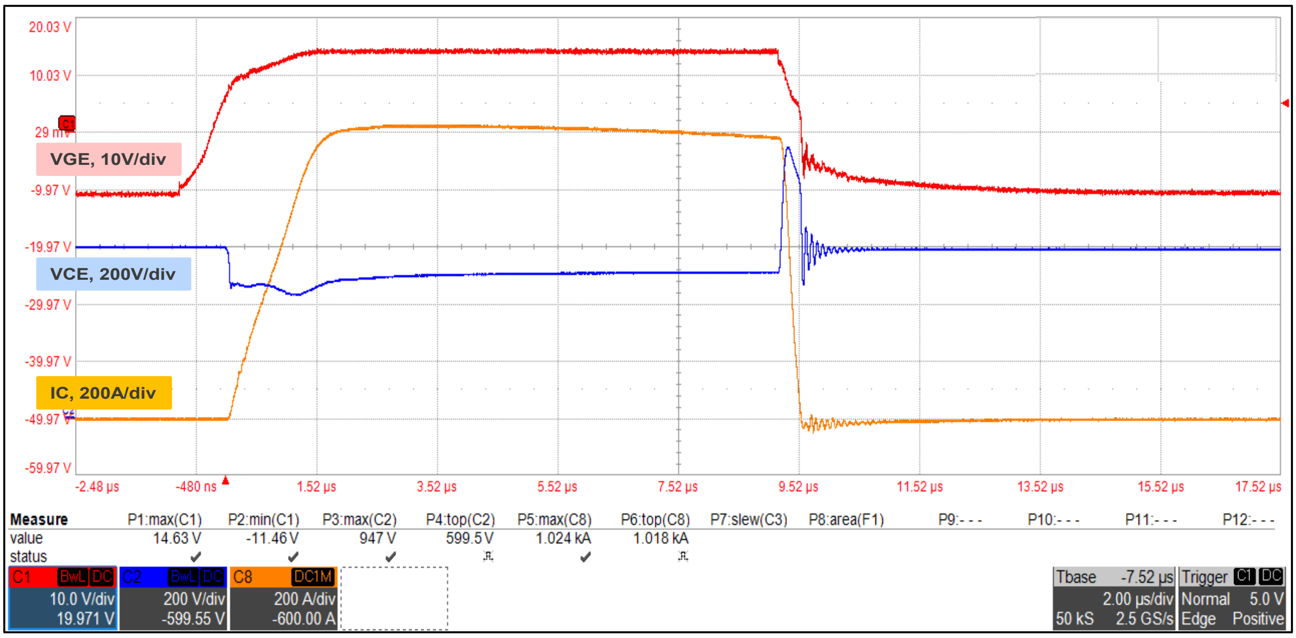

Figure 2-1 Non-destruction result

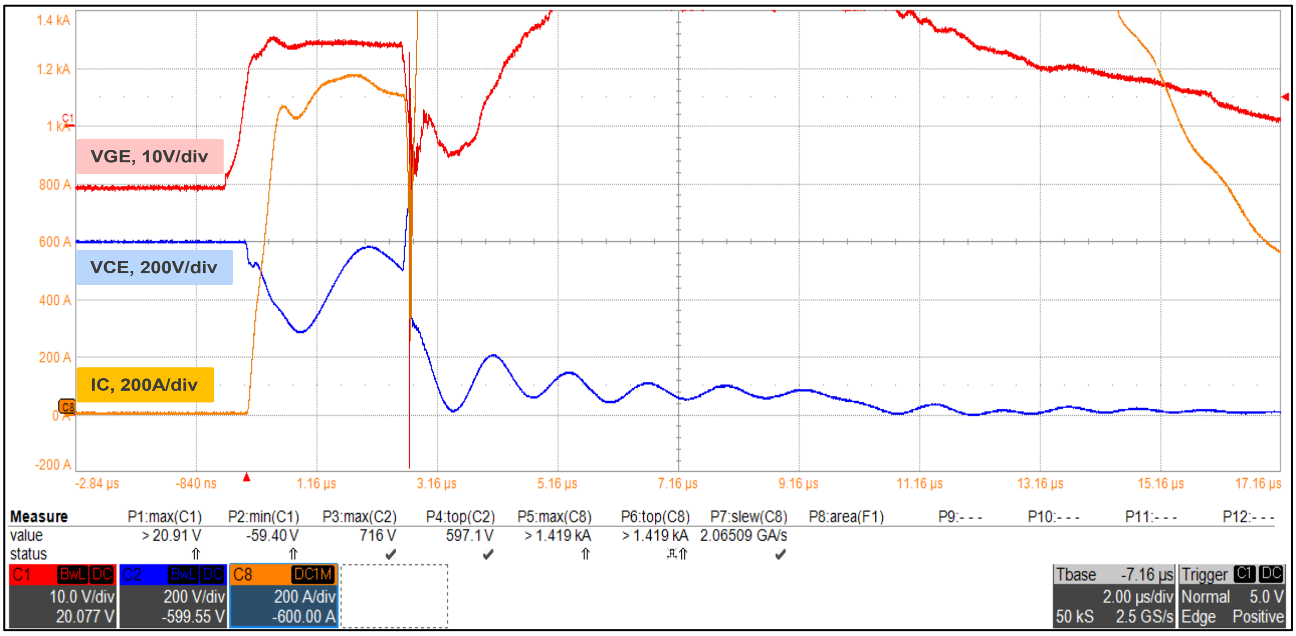

Figure 2-2 Destruction result

3. IGBT Introduction

The IGBT wafer (RJP1CS08DWA) has been selected for this LSC measurement, with a voltage capability of 1250V and a power switching capacity of 200A.

- Low collector to emitter saturation voltage VCE (sat) = 1.8V typ. (at IC =200A, VGE = 15V)
- High speed switching
- Short circuit withstands time (10 µs for min.)

3.1 IGBT Wafer Outline

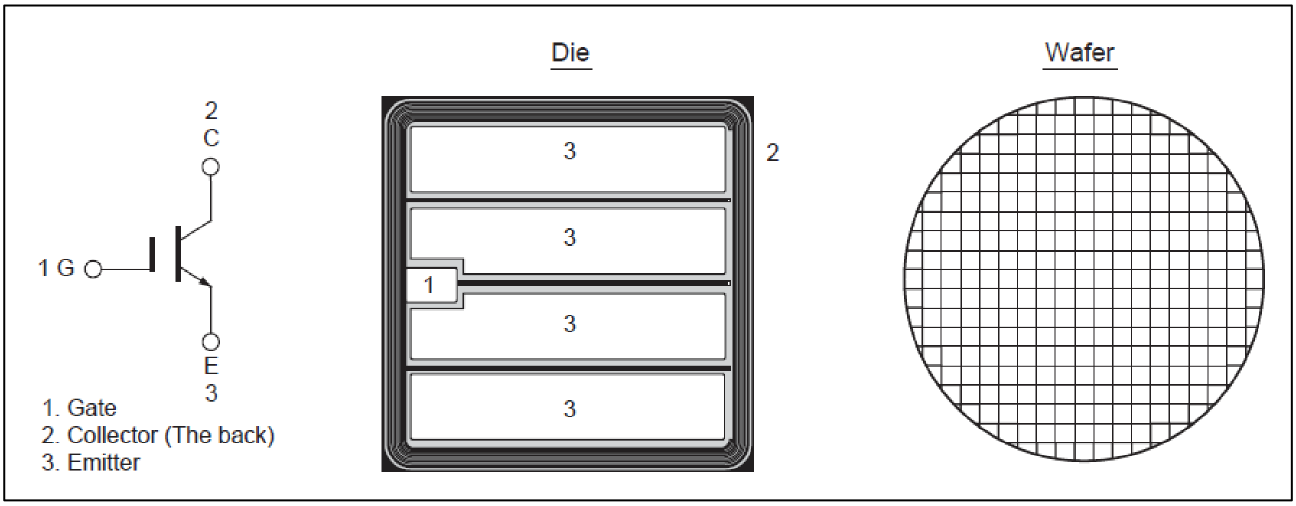

Figure 3-1 IGBT wafer outline

4. Conclusion

In conclusion, users have the option to select either the guaranteed IGBT or base their choice on the inductance characteristics to ensure circuit security. The decision should hinge on the specific design requirements, whether for 650V or 1250V applications, balancing considerations of reliability, performance, and cost. It is recommended, especially for high-capacity applications like 1250V, to prioritize the guaranteed IGBT short circuit withstand capability due to the potentially severe consequences of IGBT failure.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.29.24	-	First edition

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