

IGBT, FRD

Bonding Damage During Mounting

Introduction

This application note explains the wire bonding damage that occurs when users assemble IGBT products delivered by Renesas Electronics in bare die or wafer form.

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1. Overview

When assembling Renesas bare die or wafer IGBTs into packages such as modules, inappropriate wire bonding conditions can cause bonding damage, resulting in destruction to the IGBTs and/or surrounding components. There are various causes of bonding damage, including the following examples:

- Misaligned wire bonding resulting in short-circuited electrodes
- Scratched chip surface
- Inappropriate power, load, or other conditions during bonding

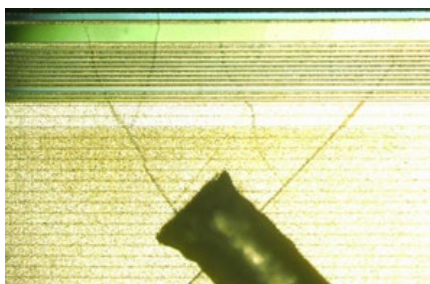
Always verify limitation conditions such as bonding damages when setting bonding conditions. These conditions, as well as handling methods, can greatly affect the characteristics fluctuation and reliability of user-assembled products. Also, wire bonding conditions vary greatly depending on the product specifications of our bare die/wafer, user substrate specifications, and wire bonding equipment. Keep in mind that wire bonding conditions also vary greatly depending on the Renesas bare die/wafer product specifications, user board specifications, and wire bonding equipment.

2. Bonding Damage Examples

Cells on chips may be damaged due to excessive bonding stress or product handling.

This is an example of visible damage on the chip surface.

Example of chip crack due to inappropriate bonding conditions



Example of chip surface damage due to incorrect product handling

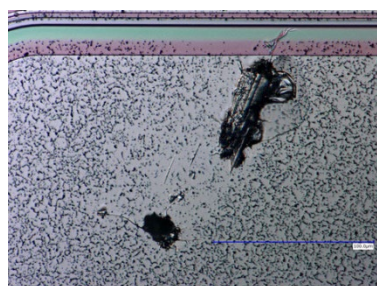
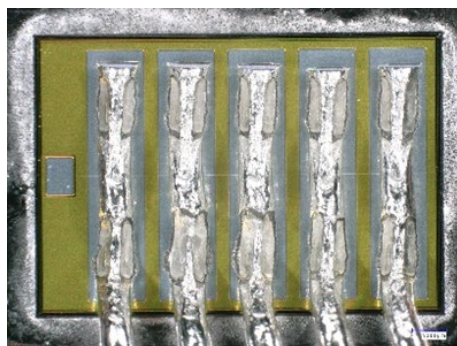


Figure 1 Example of Damage Visible on Chip Surface

Figure 2 shows an example of cell damage caused by bonding stress that is not externally visible.



Removal of aluminum wire and aluminum electrode layer

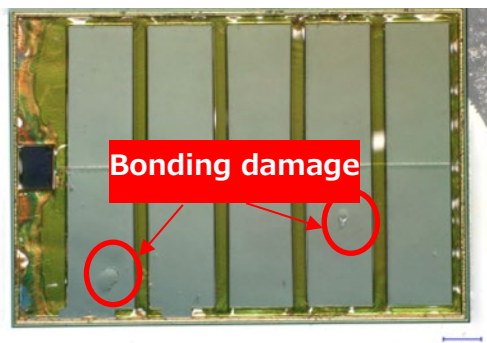


Figure 2 Example of Cell Damage that is Not Externally Visible

Figure 3 shows an example of localized damage caused by bonding stress.

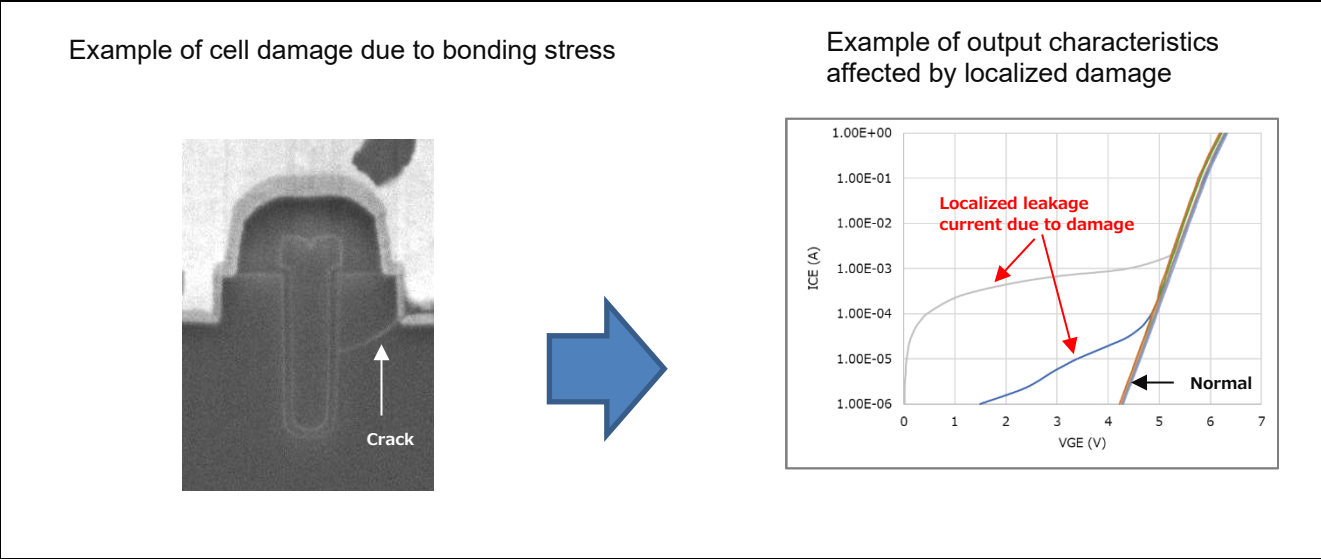


Figure 3 Example of Localized Damage

Figure 4 shows a case study in which we intentionally reproduced a turn-off failure to generate bonding damage.

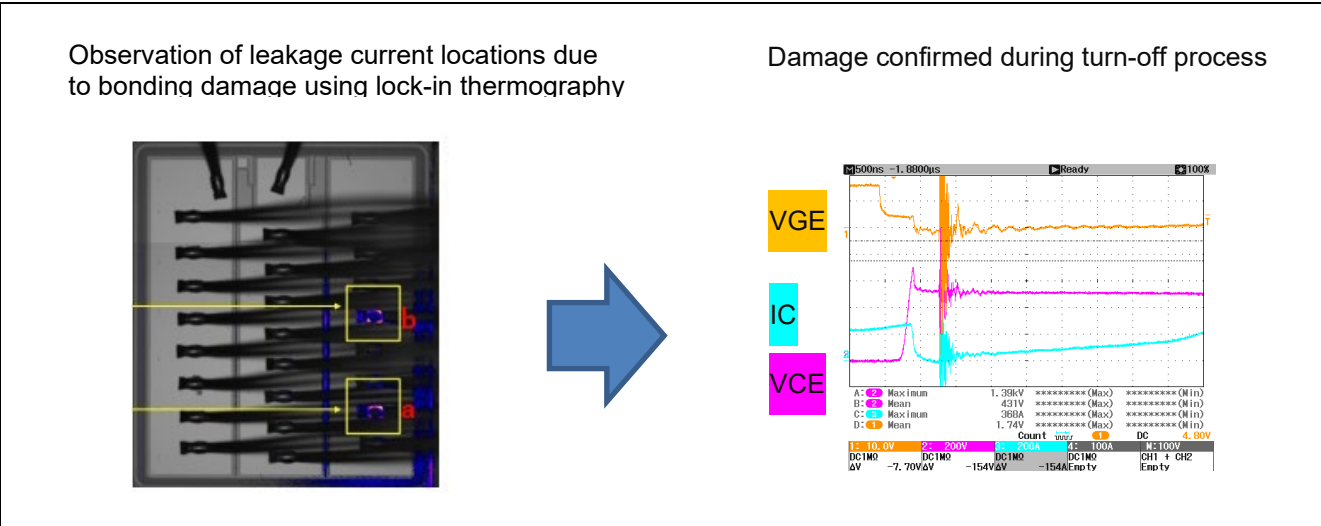


Figure 4 Reproduction of Turn-off Failure Due to Bonding Damage

3. Bonding Damage Limit Evaluation Example

We recommend that a limit evaluation of bonding crimping conditions be performed in advance to avoid bonding damage.

The following is an example of the Renesas limit evaluation.

In general, the likelihood of bonding damage increases as the power and force of the bonding machine are increased. Conversely, lowering both power and force will lead to insufficient bonding strength between wire and chip.

Fine adjustments to bonding conditions may be necessary due to changes in various conditions during the process of sample creation and mass production. For such cases, first estimate conditions (1) to (5) while considering the range of adjustment.

Then estimate (6) to (9) under slightly wider conditions than those in (5) and confirm that bonding damage and insufficient bonding strength do not occur even under these conditions. This verification provides the basis for securing margins.

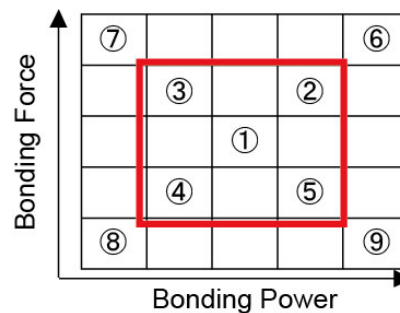


Figure 5 Example of Bonding Conditions

After the above verification, set conditions (1) to (5) as the conditions for sample creation and mass production.

4. Summary

When assembling IGBT or FRD products delivered by Renesas Electronics as bare die or in wafer form, we encourage you to check the bonding conditions carefully to avoid the problems presented in this application note and ultimately improve the yield rate of your module assembly.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.2.2024	-	First edition

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(Rev.5.0-1 October 2020)

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