IGBT

Design Considerations for Short Circuit Withstand Time (t_{sc})

Introduction

This document explains the design considerations for the short-circuit withstand time (t_{sc}) of Renesas IGBTs.

Contents

1. Load Short-Circuit Test

Elements used for bridge circuits such as inverters must include a short circuit (overcurrent) protection circuit that withstands conditions and prevents breakdown for the period until the gate voltage is cut off, even if the set is short circuited.

The length of withstand time in the event of a short circuit differs from product to product and must be verified with a load short-circuit test.

Figure 1.1 shows the short circuit used for the load short-circuit test.

A specified voltage is applied between the collector and emitter, and a pulse is applied between the gate and emitter to turn the IGBT on for a specified time. (Click Load Short Measurement Method for details on load short-circuit test method.)

During this ON period, a large current flows between the collector and emitter, and the load short-circuit withstand time (t_{sc}) is defined by Renesas as the on-time from the 10% point at which the collector current starts to flow to the 10% point at which it is cut off. (See Figure 1-2.)

The t_{sc} value is an important characteristic that indicates a product's robustness and reliability.

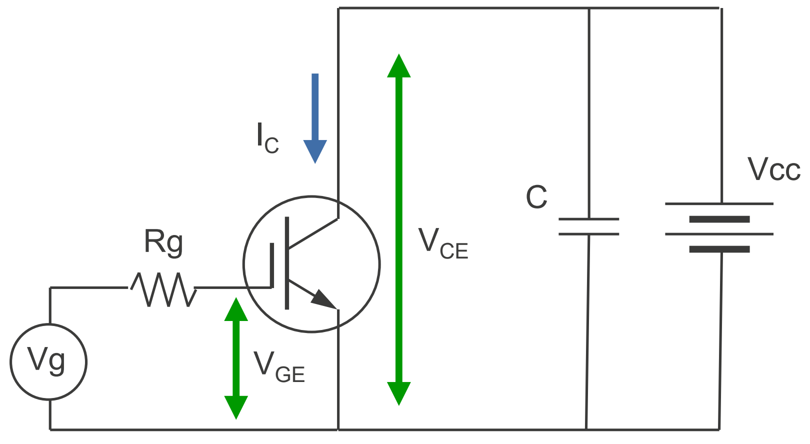


Figure 1-1 Short Circuit Used for the Load Short-circuit Test

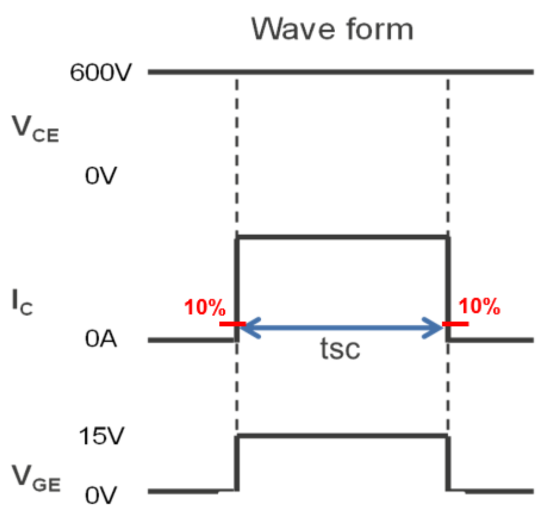


Figure 1-2 Simplified Example of Short-circuit Wave Form

2. Renesas Design Concepts

Figure 2-1 shows the breakdown points confirmed by the load short-circuit test.

Typical short-circuit breakdown points are after the short circuit (Mode A), during the ON period (Mode B), at turn-off (Mode C), and after turn-off (Mode D).

Products with short-circuit withstand capability are designed to cut off current without device damage (including breakdown after turn-off in Mode D) by meeting data sheet conditions and remaining within the t_{sc} range.

Renesas adjusts the IGBT current capability and other specifications so that breakdown modes A through C do not occur before current is cut off.

For Mode D, Renesas also verifies that the short-circuit withstanding time for which current can be cut off has ample margin for t_{sc}, while considering process variations.

Products that are not covered by a short-circuit guarantee tend to break down early on in failure modes A and B. This increases the risk of a short circuit during actual operation. Exercise caution when selecting products, as use of such products in applications that are sensitive to short-circuit events can be extremely hazardous.

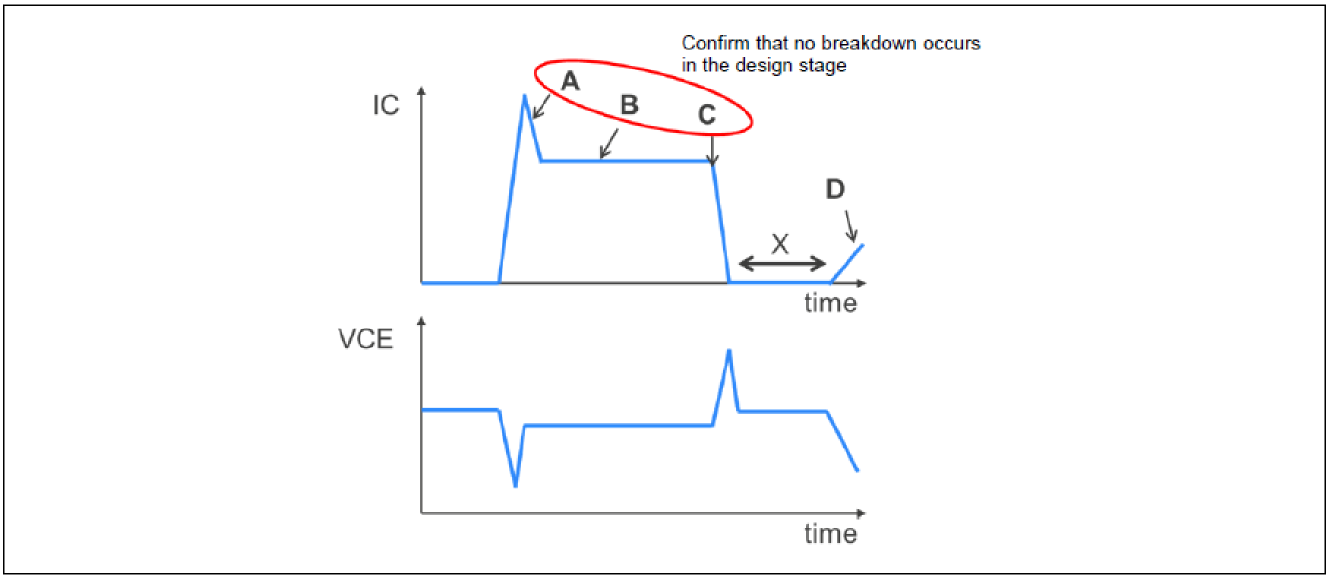


Figure 2-1 Breakdown Points in Short-Circuit Test

2.1 Mode A: Breakdown Immediately Following Short Circuit

As shown in Figure 2-1, Mode A indicates "breakdown immediately following short circuit."

This type of breakdown is usually caused by latch-up due to surge current.

Renesas IGBTs are designed with a sufficient margin for each parameter to prevent surge currents, ensuring they do not reach the Mode A breakdown point.

2.2 Mode B: Breakdown During ON Period

Mode B indicates "breakdown during the ON period."

This type of breakdown can result in latch-up due to excessive current and the formation of hot spots within the components/cells.

Renesas IGBTs are designed with a homogeneous cell layout and a sufficient margin to prevent latch-up so that they do not incur Mode B breakdown.

2.3 Mode C: Breakdown at Turn-off

Mode C indicates “breakdown at turn-off.”

This type of breakdown is usually caused by latch-up triggered by excessive off-surge voltage or rapid turn-off.

Renesas IGBTs are designed with appropriate wafer thickness and a sufficient margin to prevent latch-up so that they do not incur Mode C breakdown.

2.4 Mode D: Thermal Runaway After Turn-off

Mode D indicates “thermal runaway after turn-off.”

This type of breakdown is mainly caused by thermal runaway due to leakage currents that occur during the X period shown in Figure 2-1.

Renesas IGBTS are designed with optimal wafer thickness and threshold $V_{GE(th)}$ that guarantee the appropriate t_{sc} to prevent Mode D breakdown.

3. Indirect Control of tsc

In general, verification of short-circuit withstand t_{sc} cannot be done during the screening of wafer tests.

Therefore, we conduct “indirect control of t_{sc}” at the design stage.

Wafer thickness correlates with t_{sc}, as shown in Figure 3-1.

We set the optimum wafer thickness to provide a sufficient margin for the guaranteed t_{sc} value as stated in the datasheet.

As shown in Figure 3-2, the lower the $V_{GE(th)}$, the higher the short-circuit current IC and the shorter the t_{sc}.

Renesas has conducted load short-circuit tests on corner samples with $V_{GE(th)}$ and confirmed that there is an optimum margin for t_{sc} specifications even for samples with low $V_{GE(th)}$.

Short-circuit withstand time t_{sc}, is an important indicator of IGBT robustness.

The relationship between t_{sc} and Si heat capacity C, and applied power W, is given by equation (1).

$$t_{sc} \propto \frac{C}{W} \quad (1)$$

Since heat capacity C is the product of wafer thickness z and die size A,

and W is the product of $I_{c\,sat}$ and $V_{cc\,max}$, equation (1) can be expressed by equation (2).

$$t_{sc} \propto \frac{z \times A}{I_{c\,sat} \times V_{cc\,max}} \quad (2)$$

Furthermore, since $I_{c\,sat}$ correlates with $V_{GE(th)}$, t_{sc} includes the parameters of wafer thickness z and $V_{GE(th)}$, as shown in equation (3).

$$t_{sc} \propto \frac{z}{V_{GE\,(th)}} \times \frac{A}{V_{cc\,max}} \quad (3)$$

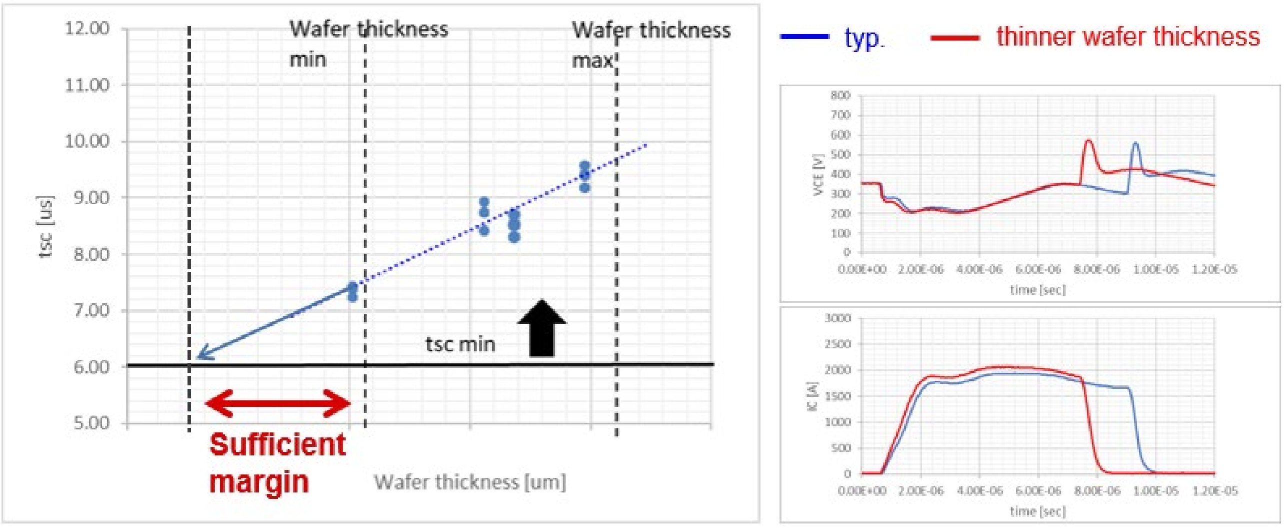
Z: wafer thickness, A: die size

Therefore, wafer thickness z and $V_{GE(th)}$ are important trade-off parameters for t_{sc}, a measure of robustness.

Renesas IGBTs are designed to optimize the parameters of wafer thickness and $V_{GE(th)}$, ensuring a design that achieves a sufficient t_{sc} margin.

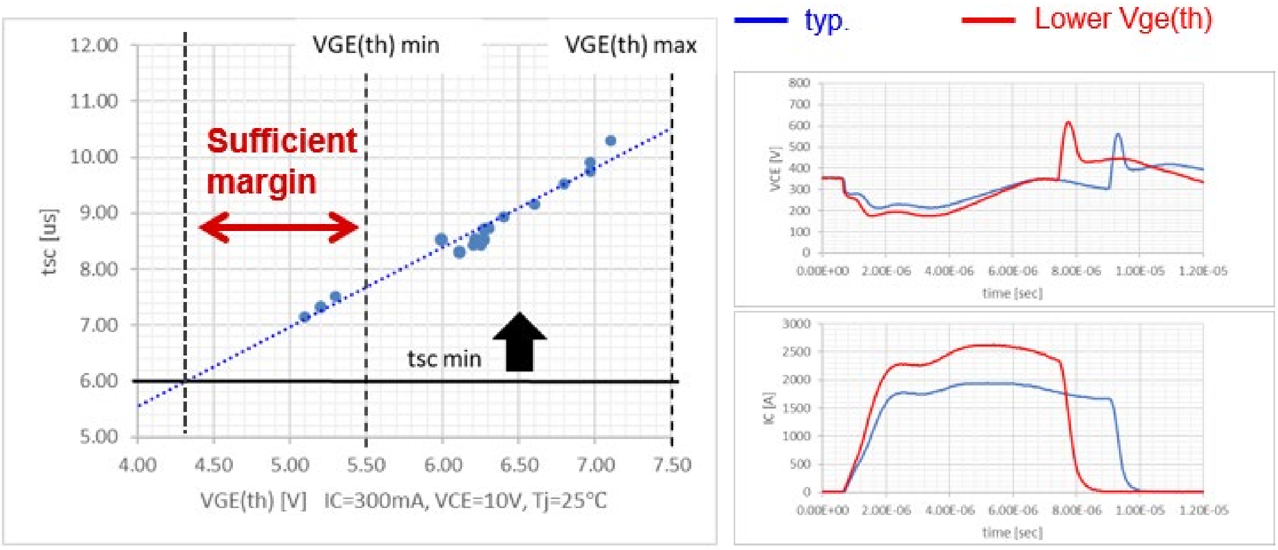
By performing tolerance design verification of characteristic items and process parameters that correlate with the short-circuit withstand t_{sc}, we can satisfy the t_{sc} specification during product development.

At Renesas, we implement this method to indirectly control t_{sc} and provide safer products.



(a) Relationship of t_{sc} and wafer thickness (b) Short-circuit waveform vs. wafer thickness

Figure 3-1 Relationship Between t_{sc} and Wafer Thickness and Short-circuit Waveform Examples



(a) Relationship of t_{sc} and $VGE_{(th)}$ (b) Short-circuit waveform vs. $VGE_{(th)}$

Figure 3-2 Relationship Between t_{sc} and $V_{GE(th)}$ and Short-circuit Waveform Examples

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.19.2024	-	First edition

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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