ClockMatrix™ Family

IEEE P3335 Time Card: Clock Tree Design Overview

Introduction

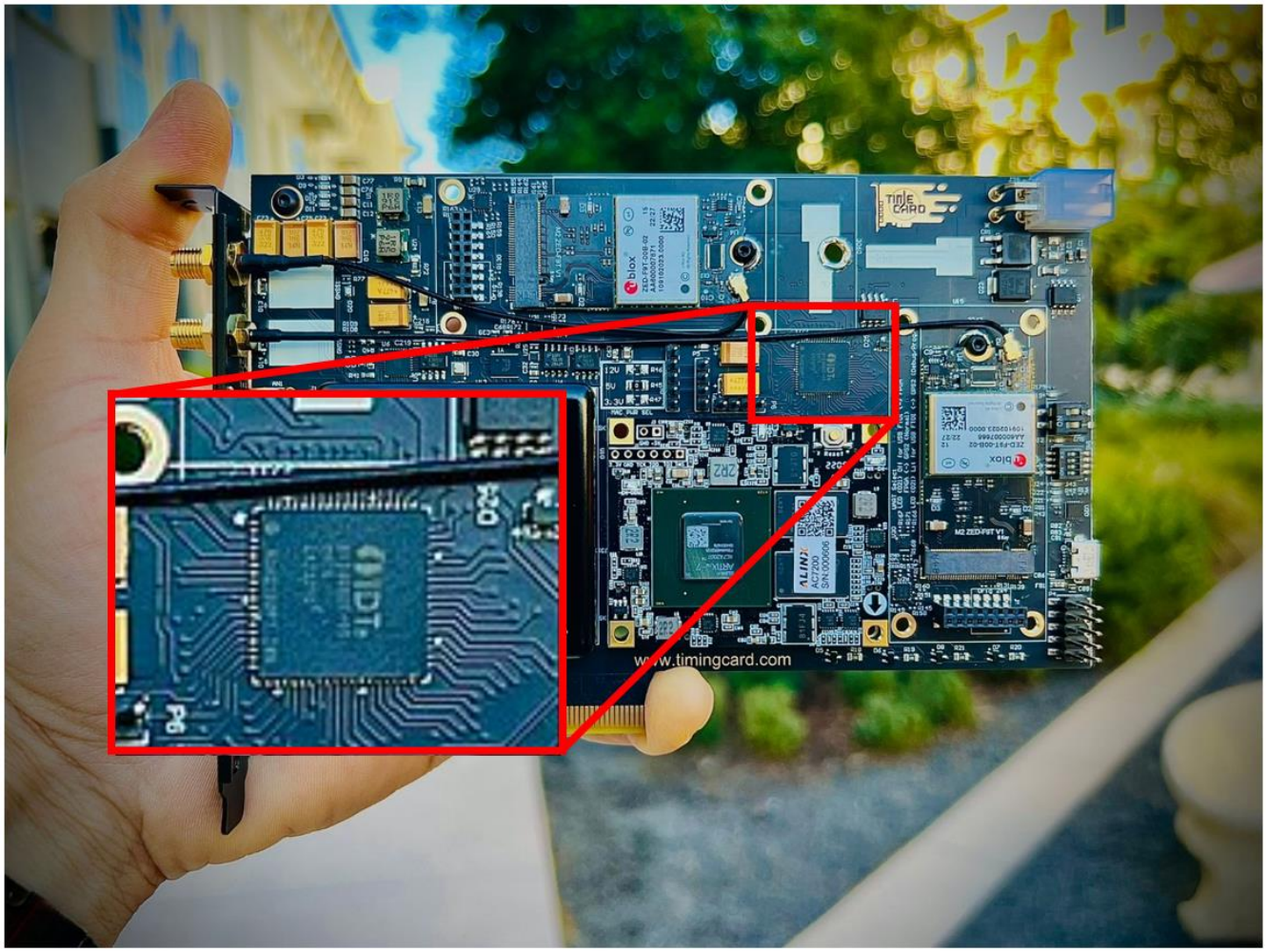
This document discusses the critical role of clock tree design in the functionality of IEEE P3335 Time Cards, emphasizing the integration and support provided by the ClockMatrix family of devices. Time Cards are essential for delivering accurate and traceable time synchronization in applications such as telecommunications, industrial automation, and financial trading. A robust clock tree ensures stability, precision, and compliance with stringent specifications. ClockMatrix serves as the cornerstone of this architecture, enabling frequency synthesis, jitter filtering, and phase alignment.

This document outlines the requirements for clock tree design, explores the capabilities of ClockMatrix, and provides practical guidance for developing high-performance Time Cards that meet future IEEE P3335 requirements.

Contents

1. Overview of Time Synchronization

Time synchronization plays a critical role in modern systems, particularly in applications requiring precision, such as telecommunications, industrial automation, and financial trading. IEEE P3335 Time Cards, designed to deliver reliable and traceable time synchronization, depend heavily on robust clock tree designs to maintain precision and stability. At the heart of this architecture is Phase-Locked Loop (PLL) silicon, which provides the essential functionality needed to distribute and stabilize clock signals.



Source: OCP-TAP Time Card V10 (www.timingcard.com)

Figure 1. Time Card Example

This document explores the clock tree requirements for a Time Card, how PLL silicon supports these requirements, and design considerations to meet IEEE P3335 specifications.

2. Overview of the Clock Tree in a Time Card

The clock tree is the backbone of any time synchronization system, responsible for distributing clock signals to various functional blocks within the Time Card. It ensures that all internal components operate in harmony and maintain synchronization with external time sources, such as Global Navigation Satellite Systems (GNSS).

2.1 Key Functional Blocks of the Clock Tree

1. Reference Clock Input:
   - Receives the primary timing signal from external sources (e.g., GNSS or atomic clocks).
   - Requires low jitter and high stability to ensure traceability to Coordinated Universal Time (UTC).
2. Clock Generation:
   - Converts the reference signal into multiple frequencies for different components.
   - Provides phase alignment and filtering to minimize jitter and noise.
3. Clock Distribution:
   - Delivers synchronized clock signals to various internal modules, including timestamping units, synchronization protocols, and local oscillators.
4. Monitoring and Calibration Units:
   - Continuously verify the accuracy of clock signals.
   - Adjust for drift or deviations using feedback from reference sources.

2.2 Requirements for the Clock Tree

The clock tree must meet stringent requirements to comply with future IEEE P3335 specifications. Low jitter is essential to ensure minimal phase noise for accurate timekeeping. A wide frequency range is necessary to support multiple output frequencies for different subsystems. Scalability is important to accommodate additional outputs without compromising performance. Traceability ensures a direct link to the external time reference, maintaining alignment with UTC. Finally, but most importantly, redundancy includes failover mechanisms to maintain synchronization during reference signal interruptions.

3. Role of ClockMatrix in Clock Tree Design

ClockMatrix is a critical component in the clock tree, enabling precise frequency synthesis, phase alignment, and noise filtering. It serves as the cornerstone for generating and distributing synchronized clock signals within the Time Card.

3.1 Core Functions of ClockMatrix

ClockMatrix performs several core functions. Frequency synthesis converts the reference clock frequency to desired output frequencies with high accuracy. It supports fractional-N synthesis for non-integer frequency ratios, enhancing flexibility. Jitter filtering suppresses high-frequency noise from the reference signal, delivering a clean output and ensuring low phase noise to meet timing precision requirements. Phase alignment aligns the output clock phase with the reference signal, maintaining synchronization, and supports phase adjustment to compensate for delay variations in the distribution clock tree. Dynamic reconfiguration enables on-the-fly adjustment of output frequencies and phases, supporting adaptive systems that respond to changes in synchronization conditions. Precise clock measurement in picosecond resolution to accurately monitor and calibrate the accuracy of clock signals.

3.2 Advantages of ClockMatrix in Time Cards

ClockMatrix offers several advantages for Time Cards. It provides high precision with femtosecond jitter performance for ultra-precise timing. Low power consumption makes it optimized for energy efficiency, which is essential for embedded systems. Compact integration combines multiple PLLs on a single chip, reducing board space. Flexibility supports a wide range of reference frequencies and output configurations. In addition, ClockMatrix natively supports ePPS clocks, making it a perfect fit for interfacing the Time Synchronization Mode per OCP NIC 3.0.

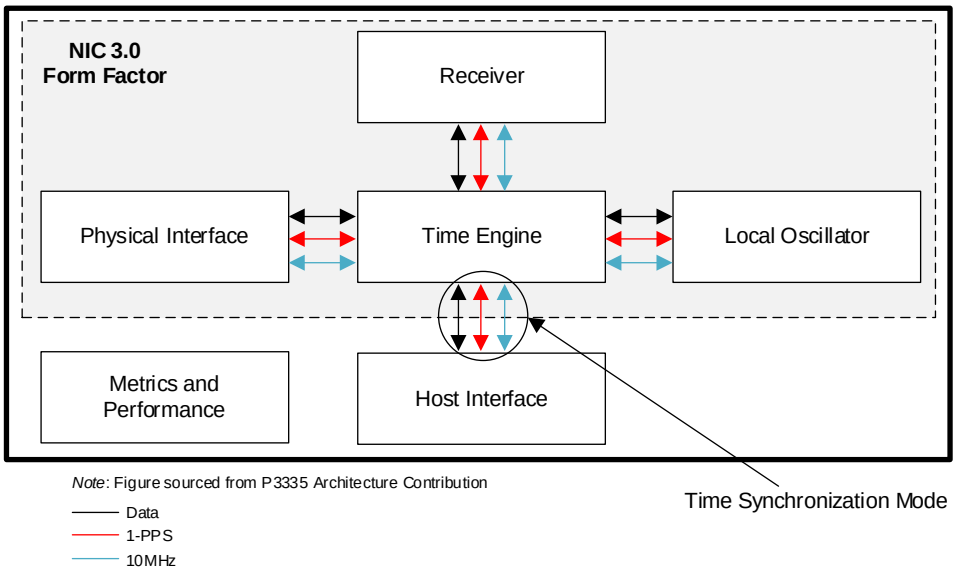


Figure 2. Time Card Supporting OCP NIC 3.0

ClockMatrix supports multiple clock input and output options for clocking and adheres to many synchronization standards and recommendations. Available Linux-based drivers based on the PTP Hardware Clock (PHC) subsystem allow for quick integration of software on the host, supporting open-source software such as Linux PTP (ptp4l).

4. Clock Tree Design Using ClockMatrix

A Time Card requires synchronization to a GNSS reference with a primary clock frequency of 10MHz and multiple output frequencies, including 125MHz for Ethernet PHYs and 156.25MHz for high-speed communication links. The system must achieve sub-nanosecond synchronization accuracy.

To design a robust clock tree for a Time Card, the process begins with defining system requirements. Input reference signal characteristics, such as frequency, stability, and jitter, must be determined. Output frequencies for all subsystems need to be identified. Timing accuracy targets for jitter, phase noise, and synchronization precision should be established, along with redundancy plans for backup reference sources and failover mechanisms. This includes multi-output capability for simultaneous generation of multiple frequencies, low jitter performance for clean and stable clock signals, a wide frequency range to cover the desired input and output frequencies, and dynamic reconfiguration for real-time adjustments to maintain synchronization.

Designing the clock distribution network involves using low-skew buffers and fanout devices to distribute clock signals without introducing significant delay or noise. Minimizing trace lengths and using controlled impedance routing helps reduce signal degradation, and termination resistors are included to match impedance and prevent signal reflections. Implementing monitoring and feedback mechanisms involves integrating phase detectors and drift correction units to monitor synchronization accuracy, along with feedback loops to dynamically adjust PLL parameters based on reference signal variations. Finally, validating and optimizing the design involves performing simulations to evaluate jitter, phase noise, and frequency stability under different conditions, conducting hardware testing to verify performance and compliance with IEEE P3335 requirements, and optimizing power consumption and thermal performance.

5. Conclusion

The clock tree is a vital component of IEEE P3335 Time Cards, ensuring precise and traceable time synchronization. ClockMatrix plays a pivotal role in enabling the required performance, offering capabilities such as frequency synthesis, jitter filtering, and dynamic reconfiguration.

By carefully designing the clock tree and leveraging advanced ClockMatrix features, engineers can meet the stringent requirements of IEEE P3335 and deliver reliable, high-performance Time Cards for critical applications. Whether in telecommunications, industrial automation, or financial trading, a robust clock tree design is essential for achieving precise and traceable time synchronization.

6. Revision History

Revision	Date	Description
1.00	Feb 25, 2025	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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