The IDTP95020 Integrated Circuit was designed for portable and non-portable applications. The device can be used in a stand alone manner and easily manage multiple power rails, audio, and be used for charging single cell Lithium Ion batteries, but it is also just as easily used in custom systems where on the fly changes to outputs or functionality is necessary. The ideal way to achieve this is to connect an EEPROM device with a startup sequence installed and connected to the I2CM (M is for master) SCL and SDA lines to initiate the default, or startup configuration and then use an application processor connected to the I2CS (S is for slave) SDA and SCL lines. It should be noted now that the IDTP95020 is not an I2C master and can be used as a slave only.

The IDTP95020 I2C bus operates in compliance with I2C Standard Communication Protocol but there are a couple of important steps that need to be adhered to in order to make sure the correct register is being accessed while using the I2C bus to read and write registers within the IDTP95020 device. The device has 768 8-bit registers available for reading and writing. Since standard I2C programming involves an 8-bit address, a global register has been implemented allowing the programming of each of the 3 – 256 register sets. These three sets of 256 registers have been named pages, and they can be found by looking at the main prefix of the desired address:

The register prefix is as follows-

- 0xA0nn Page 0 register bank
- 0xA1nn Page 1 register bank
- 0xA2nn Page 2 register bank

Furthermore, the computation of each register is as follows:

Register address computation: address = Base_address + Offset Address

See Register Mapping Explanation (Figure 3) in the Appendix for more information on the registers and their mapped location.

Additionally, the default Chip ID of the IDTP95020 is 0x55h. This can be changed if desired during the startup script. Now as an example, in order to read the contents of the BUCK1000 programmed output voltage register (0xA084).

Output Voltage Registers

(See Table 144 above for addresses: 0xA080, 0xA082 and 0xA084).

The Output Voltage Register contains the Enable bit and the Output Voltage setting bits.

Table 145. Output Voltage Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	VALUE	DESCRIPTION / COMMENTS
[6:0]	VOUT	See [Note 1]	RW	(See Table 146)	Output Voltage = VOUT * 0.025V + 0.75V
7	ENABLE	0h	RW	1 = Enable 0 = Disable	Enable Output

Note 1: The default settings for the output voltage are BUCK500_0 = 3.3V, BUCK500_1 = 1.8V and BUCK1000 = 1.2V.

Figure 1 - IDTP95020 BUCK Output Voltage registers

The bus must be programmed in the following order:

Address Device (Chip ID), Address Page ID (0x01h), Program Page ID to 0.

now, subsequent I2C writes and reads involving the IDTP95020 will all take place within Page-0 registers. Therefore, in order to change the BUCK1000 output voltage to 3V, this sequence should be implemented:

Address Device (Chip ID), Address Output Voltage Register (0x84h), Program Voltage (0xDA).

PAGE_ID Register

I²C Address = Page-x: 01(0x01), µC Address = 0xA001

Table 236. PAGE_ID Register

BIT	BIT NAME	DEFAULT SETTING	USER TYPE	DESCRIPTION / COMMENTS
[1:0]	PAGE	00b	RW	Page ID
[7:2]	RESERVED	000000b	RW	RESERVED

Figure 2 - Page ID register, used for setting which set of 256 registers is used for R/W operations

Of course, sequential programming is supported. See Figure 4 in the appendix for more information on incremental or selective register programming. Finally, the first 16 registers of each page are the global registers, this will avoid contention between reading and writing to the Page ID

register or other global register versus a R/W to the register of interest. If there are still any questions, feel free to contact your IDT applications engineer for further guidance.

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Integrated Device Technology, Inc.
APD – Applications Engineering
March 3, 2012

Appendix:

Table 11 – Register Address Global Mapping

MODULE	SIZE (BYTES)	BASE ADDRESS (I²C)	BASE ADDRESS (6811 µP)	REGISTER DEFINITION LOCATION	MODULE DESCRIPTION
Global Registers	16	Page-x: 000(0x00)	0xA000	Page 144	Global registers are used by the Access Manager, the first 16 registers of each page are global for all the pages.
ACCM	16	Page-0: 016(0x10)	0xA010	Page 149	Access manager, including an I²C slave and bus arbiter
PCON	32	Page-0: 032(0x20)	0xA020	Page 131	Power controller, including registers that control the on/off of the regulators, and control/sense of the GPIO, power states
				Page 76	Clock Generator Registers
RTC	32	Page-0: 064(0x40)	0xA040	Page 79	Real Time Clock
LDO	32	Page-0: 096(0x60)	0xA060	Page 155	Linear regulators, including regulators for external and internal usage
DC_DC	16	Page-0: 128(0x80)	0xA080	Page 88	Switching regulators and Class-D BTL driver consisting of three bucks, one 5V boost , one white LED driver and one Class-D BTL driver
CHARGER	16	Page-0: 144(0x90)	0xA090	Page 63	Battery Charger, including a dedicated switching buck regulator, an ideal diode, a precision reference and thermal sensor
GPT	16	Page-0: 160(0xA0)	0xA0A0	Page 86	General purpose timers
RESERVED	16	Page-0: 176(0xB0)	0xA0B0		RESERVED
ADC_TSC	64	Page-0: 192(0xC0)	0xA0C0	Page 117	Touch-screen (ADC, pendown detect and switches, temperature and battery voltage monitoring), and GPIOs
AUDIO	240	Page-1: 000(0x00)	0xA100	Page 41	Audio subsystem, excluding class-D amplifier
CLASS_D_DIG	240	Page-2: 000(0x00)	0xA200	Page 31	Class-D amplifier digital processing part
RESERVED	240	Page-3: 000(0x00)	0xA300		RESERVED

Figure 3 - Register Mapping Explanation

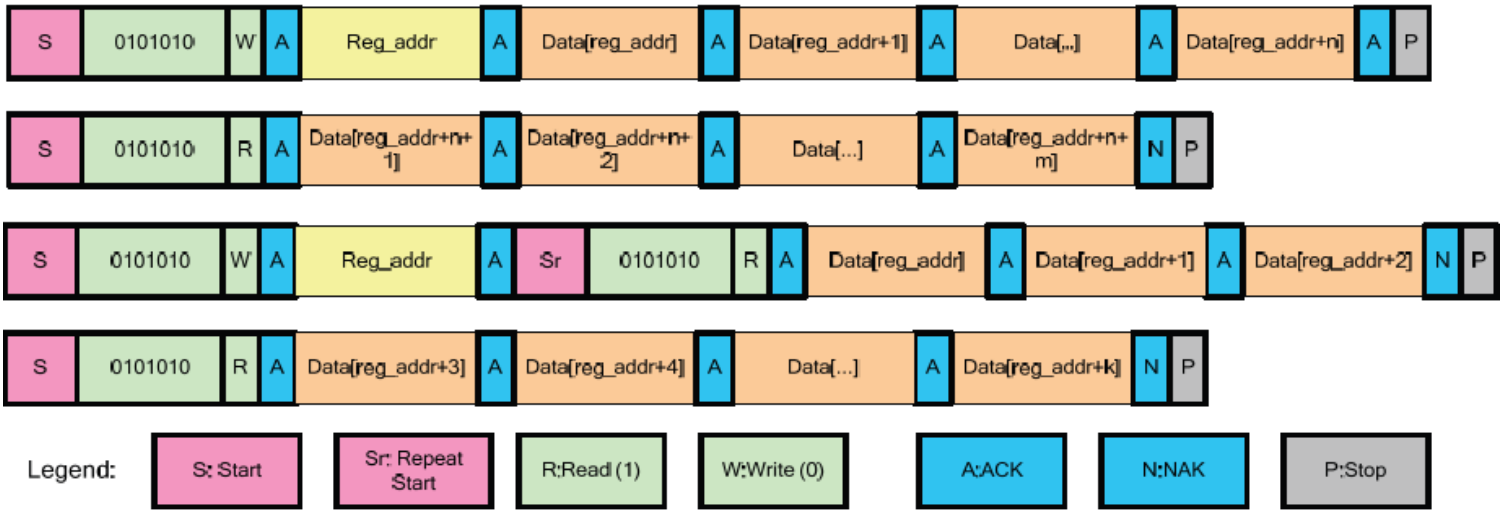

Figure 4 - I2C Read/Write Operation

References:

1. “The I2C-BUS Specification.” Version 2.1. Phillips Semi-conductors, January 2000. Web. 03 March, 2012.

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