I3C/I²C Bus Multiplexer, IO Expander

The I²C bus is a standard bidirectional interface between master and slave devices. The I3C interface improves upon the features of the I²C interface, while maintaining backward compatibility. It is a two-wire bidirectional serial bus, optimized for multiple slave devices and is controlled by only one I3C master device at a time.

In most I3C/I²C applications, there is the potential need to access I3C/I²C slave devices that share two masters, to isolate slave devices that have similar addresses, or to provide more external I/O ports. Renesas provides an I3C/I²C Bus Multiplexer and I/O Expander to meet these different application requirements.

Contents

1. Features

- Supports I3C basic spec and backward compatible with I²C
- Two-wire programmable I3C/I²C bus serial interface
- Single device load on the host bus
- Single 1.8V power supply
- Up to 12.5MHz I3C transfer rate
- Integrated on-die LDO, 1.0V VLDO output at VIO pin
- Support Internal pull-up with internal VLDO
- Supports 1.0V, 1.1V, and 1.2 V push-pull IO levels
- Supports 1.0V, 1.2V, 1.8V, 2.5V, and 3.3V open-drain IO levels
- Integrated Temperature Sensor; 0.5°C accuracy with 0.25°C resolution
- Bus reset function
- Packet Error Check (PEC) function
- Parity Error Check function
- Up to 8 unique addressing (except IMX3102 which has a static address)
- Programmable I3C, I²C Bus Addressing Scheme
- 9-pin thermally enhanced 2 × 3 × 0.75mm DFN package
- Temperature: Industrial range of -40° to 125°C

2. I3C/I²C Multiplexer Applications

Table 1. I3C Multiplexer Part Numbers and Feature Summary

Part Number	Bus Multiplexer	Internal Thermal Sensor	I3C/I²C Address (xxx = HID, 000 to 111)
IMX3102	2:1	Yes	0001 111
IMX3112	1:2	Yes	1110 xxx

2.1 IMX3102 – 2:1 Bus Multiplexer

The IMX3102 is a 2-to-1 I3C basic bus multiplexer switch with integrated Temperature Sensor. It is designed to be used for various motherboard applications. There are two master ports (Master port 0 and Master port 1) and one slave port. Either master port can be selected as active Master, which has the control of the slave port as well as the IMX3102. By default, at power on, the master port 0 is selected as active master and it can hand over the control to master port 1 at any time by setting bit 7 in MR65.
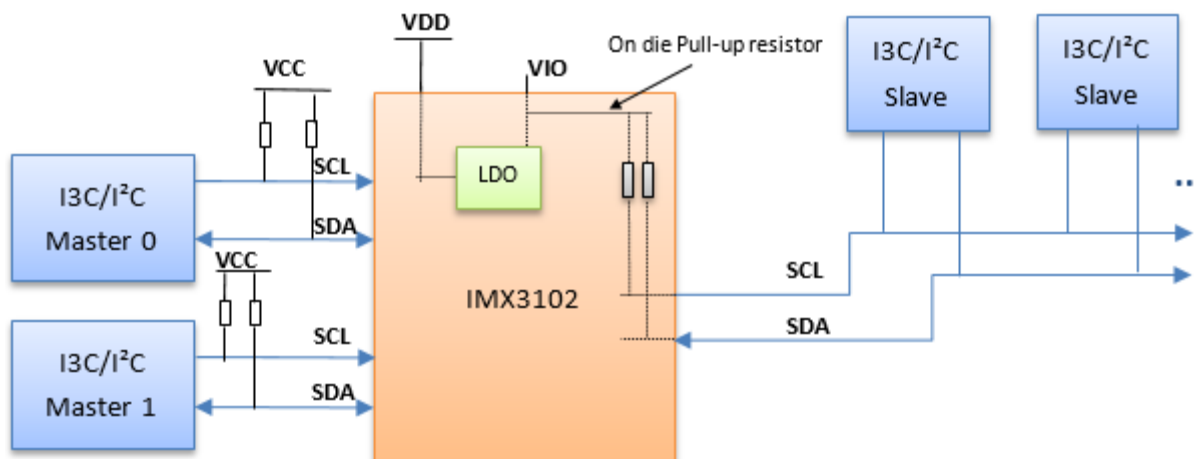

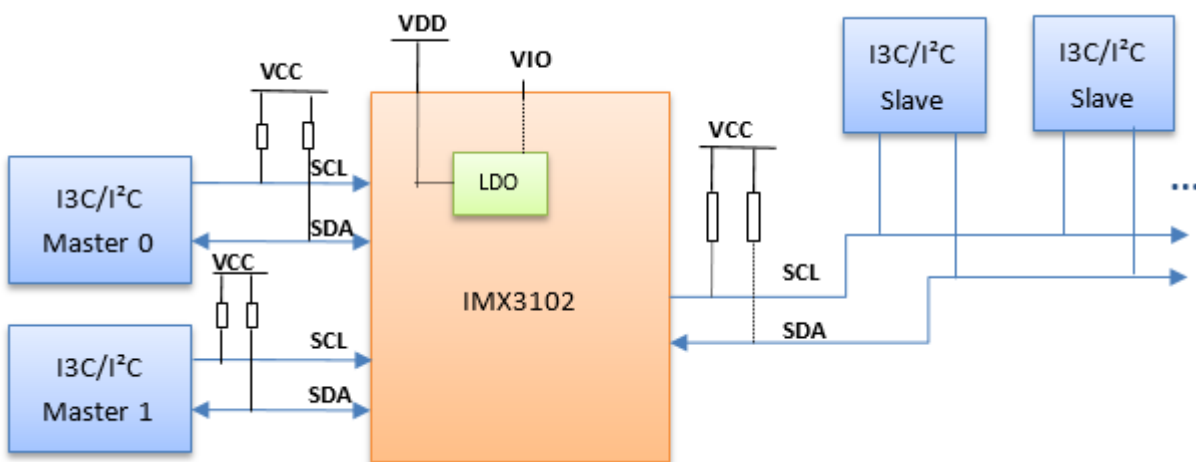**Figure 1. I3C/I²C Bus 2:1 Multiplexer with Slave Devices (Using Internal On-die Pull-up Resistor)**

Figure 2. I3C/I²C Bus 2:1 Multiplexer with Slave Devices (Using External Pull-up Resistor)

2.2 IMX3112 – 1:2 Bus Multiplexer

The IMX3112 is a dual bidirectional 1-to-2 translating multiplexer for the I3C/I²C bus. The input SDA/SCL pair can fan out to two output pairs (or channels), and either individual output channel can be selected. Applications with slave devices that share the same address can use the multiplexer to prevent slave address conflicts. By selecting the proper output channel, the I3C/I²C master can communicate with more slave devices.
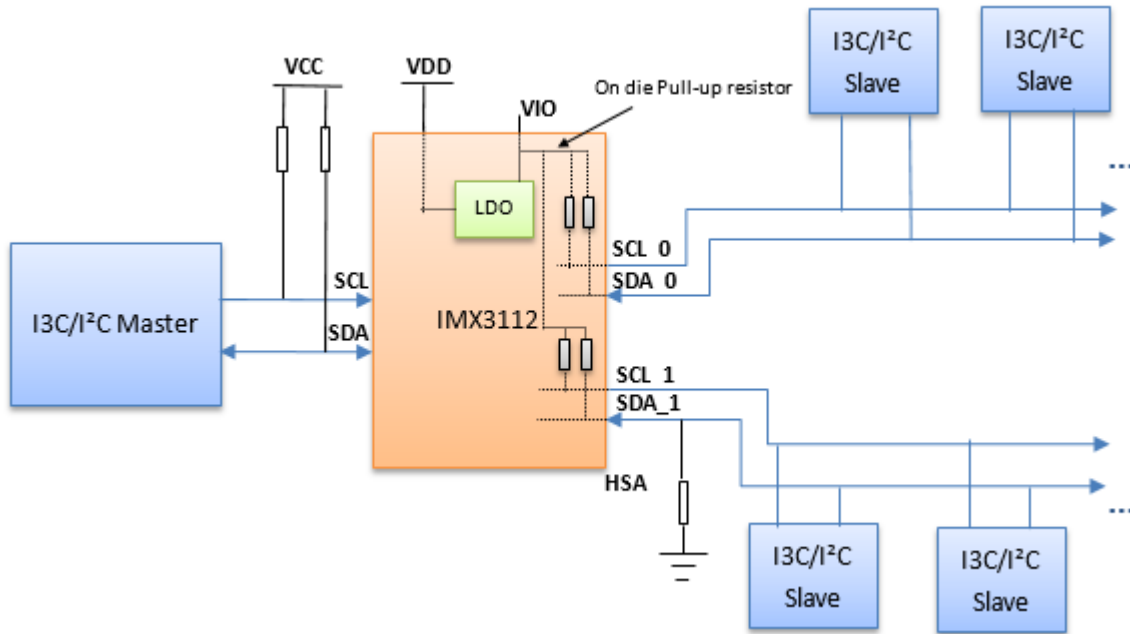

Figure 3. I3C/I²C Bus 1:2 Multiplexer with Slave Devices (Using Internal On-die Pull-up Resistor)
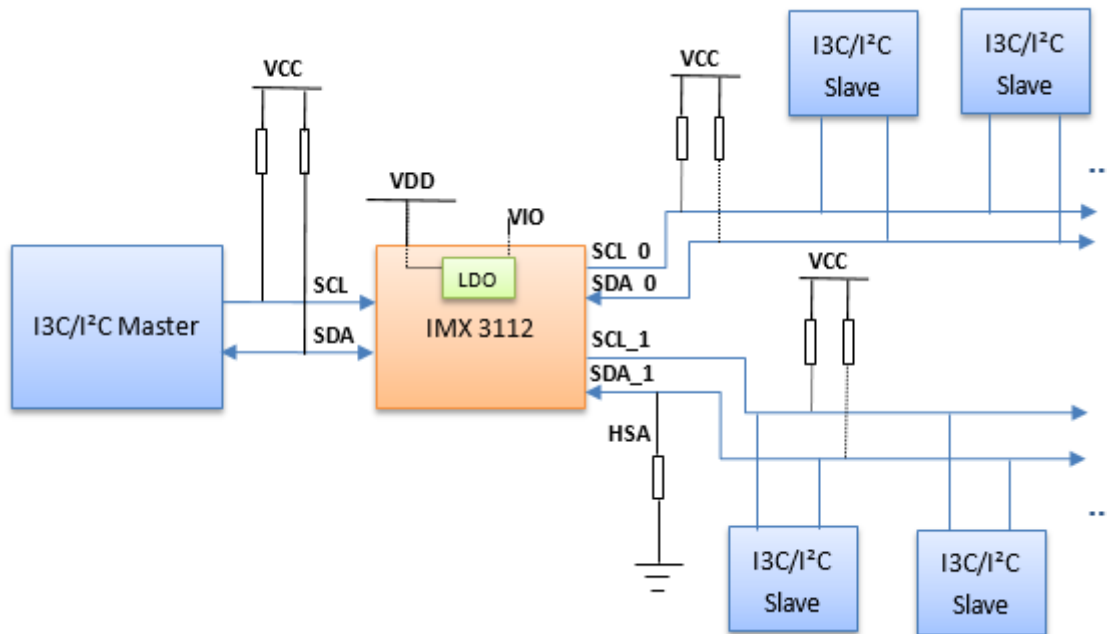

Figure 4. I3C/I²C Bus 1:2 Multiplexer with Slave Devices (Using External Pull-up Resistor)

2.3   IO Level Support

On the master side, the IMX3112/3102 can support open-drain IO levels from 1.0V to 3.3V depending on the supply rail master that pulled up the resistor. On output side, the IMX3112/3102 can support open-drain IO levels from 1.0V to 3.3V with an external pull-up resistor or support push-pull IO levels from 1.0V to 1.2V with an internal pull-up resistor. The IO voltage level is configurable through register MR14 [4:2].

	Open Drain	Push Pull
Support IO Voltage	1.0V to 3.3V	1.0V, 1.1V or 1.2V

2.4   IMX3102 Active Master Selection

The IMX3102 (2:1 multiplexer) has two registers, MR64 and MR65, that are used to select the active master port and enable the slave port. These registers can be written and read via the I3C/I²C bus. For more information, see the *IMX3102 Datasheet*.

2.5   IMX3112 Local Channel Selection

The IMX3112 (1:2 multiplexer) provides two control registers for the master to select one of the downstream channels as an output local channel – MR64 (IO port switch configuration) and MR65 (bus mux selection). These registers can be written and read via the I3C/I²C bus. For more information, see the *IMX3112 Datasheet*.

2.6   I3C/I²C Address

The 7-bit device I3C/I²C address of the IMX3102 is static 0001 111b, which can be any unique address and be programmed by Renesas before shipping. However, the IMX3112 always samples the status of the HSA (Host Address) pin on power-up (the HSA pin is used in conjunction with SDA_1, and is tied to GND via a resistor value). The status of the HSA pin determines the unique host ID (HID) of the device. The host identifier value is merged with the device type **1110 xxxb** to establish the 7-bit address for this device on the I²C or I3C bus as shown in Table 3. For example, if the value sensed on HSA pin identifier 2 (010 binary), then the unique address for this device is 1110 010b.

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Table 2. 7-bit Address of the IMX3112/3102 Device

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Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	HID2	HID1	HID0	R/W
Multiplexer Device Type ID				Host ID (HID)			Read/ Write

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Table 3. HSA Pin Resistor Value and ID

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HSA Pin Connection[1]	Device ID	Comment
10.0KΩ to GND	HID = 000	
15.4KΩ to GND	HID = 001	
23.2KΩ to GND	HID = 010	
35.7KΩ to GND	HID = 011	1% Resistor
54.9KΩ to GND	HID = 100	
84.5KΩ to GND	HID = 101	

HSA Pin Connection[1]	Device ID	Comment
127KΩ to GND	HID = 110	
196KΩ to GND	HID = 111	

1. If there is no resistor between the HSA pin and GND, the IMX3112 will sense a device HID of 111.

2.7   I3C/I²C Mode Switch

By default when the IMX3112/3102 first powers on, it operates in I²C mode. The IMX3112/3102 can operate in I²C mode indefinitely. The host puts the IMX3112/3102 in I3C mode by issuing *SETAASA* CCC. The host can put the IMX3112/3102 back in I²C mode from I3C mode at any time by issuing *RSTDAA* CCC.

Table 4. SETAASA CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x29 (Broadcast)								T	P

Table 5. RSTDAA CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x06 (Broadcast)								T	Sr or P

2.8   Temperature Sensor

The IMX3112/3102 has an integrated termperature sensor that provides thermal capability of $0.5°C$ accuracy with $0.25°C$ resolution. All thermal registers are 16-bit quantities stored in two consecutive registers – low byte and high byte. The device always returns 0 in Reserved (RSVD) bits when the host reads from the low and high byte. Units for all thermal registers are $°C$. The format of the thermal registers is displayed in the following tables.

Table 6. Thermal Register - Low Byte and High Byte

Register		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR49	Low Byte	8	4	2	1	0.5	0.25	RSVD	RSVD
MR50	High Byte	RSVD	RSVD	RSVD	Sign	128	64	32	16

Table 7. Thermal Register Examples

High Byte	Low Byte	Value	Unit
000 0 0101	1111 00 00	+95.00	°C
000 0 0101	0101 00 00	+85.00	°C
000 0 0100	1011 00 00	+75.00	°C
000 0 0000	0001 00 00	+ 1.00	°C

High Byte	Low Byte	Value	Unit
000 0 0000	0000 11 00	+ 0.75	°C
000 0 0000	0000 10 00	+ 0.50	°C
000 0 0000	0000 01 00	+ 0.25	°C
000 0 0000	000 0 0000	0.00	°C
000 1 1111	1111 11 00	-0.25	°C
000 1 1111	1111 10 00	-0.50	°C
000 1 1111	1111 01 00	-0.75	°C
000 1 1111	1111 00 00	-1.00	°C
000 1 1111	1101 10 00	-40.00	°C

2.9 Comparison between I²C and I3C Basic

The following table compared the key feature differences between I²C and I3C basic.

Table 8. Comparison between I²C and I3C

Parameter	I²C	I3C
Number of wires	2-wire	2-wire
Data Rate	3.4MHz (Hs) / 1MHz (Fm+) / 400KHz (Fm)	Up to 12.5MHz
IO Voltage	1.0V ~ 3.3V	1.0V, 1.1V, or 1.2V
In-Band Interrupt	No (An additional wire is required for interrupt support)	Yes (No additional signal required)
Packet Error Check (PEC)	No	Yes
Parity Error Check	No	Yes
In-band Integrated Commands (CCC) Support	No	Yes
Slave Address	7 bit, Static	7 bit, Dynamic (Assigned during initialization, static I²C address at start)
Data Signal	Open Drain	Open Drain or Push-pull (Changed dynamically)
Clock Signal	Open Drain	Push-pull

3. Revision History

Revision	Date	Description
1.0	Sep 17, 2021	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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