

## How to Use the FemtoClock 3 Wireless (FC3W) Time-of-Day Counter

## Introduction

This document describes how to configure the Time-of-Day Counter for FemtoClock™ 3 Wireless (FC3W) devices.

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# 1. Overview

FemtoClock 3 Wireless (FC3W) devices have an internal Time-of-Day Counter (TOD) for accurate and precise time stamping. The TOD can be configured to reference the output clock from any of the fractional output dividers (FOD). The TOD reference clock requires a minimum frequency of 500MHz and maximum 625MHz coming from the chosen FOD.

There are two internal counters labeled as the Time Clock (sync\_counter) and Time Sync (sub\_sync\_counter). The Time Clock speed is configured using the **time\_clock\_gen\_count (0xA00[5:0])** register set, which represents the number of FOD input clock cycles (minus one) in a Time Clock period. The Time Sync speed is configured using the **sub\_sync\_count (0xA04[30:0])** register set, which represents the number of Time Clock cycles (minus one) in a Time Clock period.

The **time\_clock\_gen\_count** has a maximum integer value of 64, allowing a range of frequencies between 7.8125MHz – FOD input frequency. The sub\_sync\_count register set has a maximum value of  $(2^{31}) - 1$ , allowing the counter to have frequencies less than 1Hz.

There is a 1µs update rate for both count values. The counts increment internally and can be read at the 1µs interval.

## 2. RICBox GUI Setup

To configure the TOD in RICBox, open the FemtoClock 3 Wireless user interface and go to the block diagram view.

1. Click on the TOD and Synthesis block.



Figure 1. Open TOD and Synthesis Block

2. Click the Enable Time Sync TOD Block checkbox.

*Note*: This enables the TOD to start counting if configured during run-time.



Figure 2. Enable Time Sync TOD Block

3. Select the FOD input reference from the dropdown menu in the upper left corner.

Enable	Time Sync TOD Block	
Time Sync Channel Source FOD Select	FOD2 V	đ
	FOD0	
5000	FOD1	annel Source
FOD1	FOD2	uency
FOD2	Reserved	pne

Figure 3. Select TOD Reference Clock

4. Configure the *Time Clock Frequency Goal* and *Time Sync Frequency Goal*. RICBox automatically fills in the value for the **time\_clock\_gen\_count** and **sub\_sync\_count**.

TOD

Time Clock Source	Sub-Sync	: Pulse Counter
	Synchronous Load Request	Sub-Sync Counter Load Enable
	Sub-Sync Counter Load Value	0x0000000
Time Clock Generation Counter	Time Sync Generation Counter	0x00000C34
Time Clock Frequency Goal 25MHz	Time Sync Frequency Goal	1Hz

Figure 4. Set Time Clock and Time Sync Frequencies

## 3. Run-time

To start or stop the counters, write to the **TOP.TIME\_SYNC\_TOD.TOD\_ENABLE\_CTRL.enable** bit (0xA0A[0]). This is done in the RICBox by connecting to a device with the connection interface and using the command line interface (CLI).

1. After a connection is established, click on the Tools menu and select CLI.

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File	Tools	Help			
0-	С	LI			
	S	tatus Monitor			
Ovi	R	egister Write Export			
Po	<b>/</b> ower				

Figure 5. Open RICBox CLI

- 2. Type "write TOP.TIME\_SYNC\_TOD.TOD\_ENABLE\_CTRL.enable 1" to start the count.
- 3. Use "write TOP.TIME\_SYNC\_TOD.TOD\_ENABLE\_CTRL.enable 0" to stop the count.

Figure 6. Enable the TOD Count

## 3.1 Reading the Count with Serial Connection

Since the counters are updated every 1µs, it is possible the count could get updated while it is also being read. Issue a read to the **tod\_counter\_rd\_req (0xA5F[0])** to temporarily stop counter updates, ensuring the updates are blocked and the data can be read atomically. This also ensures that the Time Clock and Time Sync values are consistent with one another.

- The Time Clock count is stored in sync\_counter\_value (0xA60[82:31]).
- The Time Sync count is stored in sub\_sync\_counter\_value (0xA60[30:0]).
- 1. In RICBox CLI, type "read TOP.TIME\_SYNC\_TOD.TOD\_COUNTER\_READ\_REQ.tod\_counter\_rd\_req".

Renesas	RICBox CLI	—	×
> read TOP.TIME_SYNC_TOD.TOD_COUNTER_ 0x0	READ_REQ.tod_counter_rd_req		
1			

### Figure 7. TOD Read Request

2. Then type "read TOP.TIME\_SYNC\_TOD.TOD\_COUNTER\_STS.sync\_counter\_value" to read the Time Clock count.



Figure 8. Read Time Clock Count

3. Type "read TOP.TIME\_SYNC\_TOD.TOD\_COUNTER\_STS.sub\_sync\_counter\_value" to read the Time Sync count.



Figure 9. Read Time Sync Count

### 3.2 Updating the Counters Synchronously

The Time Clock and Time Sync counters can be updated synchronously. A new Time Clock counter value can be stored in the **sync\_counter\_load\_val (0xA10[82:31])** register set.

1. Issue a write command in the RICBox CLI:

"write TOP.TIME\_SYNC\_TOD.TOD\_SYNC\_LOAD\_VAL\_CTRL.sync\_counter\_load\_val <NEW VALUE>"



Figure 10. Set Time Clock Counter Value Buffer

2. Enable a synchronous load to the Time Clock with the sync\_load\_enable bit (0xA20[1]).

"write TOP.TIME\_SYNC\_TOD.TOD\_SYNC\_LOAD\_EN\_CTRL.sync\_load\_enable 1"

RENESAS	RICBox CLI	-	×
> write TOP.TIME_SYNC_TOD.TOD_SYNC_L Wrote 1 byte(s) to offset 0xA20	OAD_EN_CTRL.sync_load_enable 1		

Figure 11. Enable Time Clock Synchronous Load

3. Store the new Time Sync counter value in the sub\_sync\_counter\_load\_val (0xA10[30:0]) register set.

"write TOP.TIME\_SYNC\_TOD.TOD\_SYNC\_LOAD\_VAL\_CTRL.sub\_sync\_counter\_load\_val <NEW VALUE>"

Renesas	RICBox CLI	-	×
> write TOP.TIME_SYNC_TOD.TOD_SYNC_ Wrote 16 byte(s) to offset 0xA10	LOAD_VAL_CTRL.sub_sync_counter_load_val 0		

Figure 12. Set Time Sync Counter Value Buffer

4. Enable a synchronous load to the Time Sync with sub\_sync\_load\_enable bit (0xA20[0]).

"write TOP.TIME\_SYNC\_TOD.TOD\_SYNC\_LOAD\_EN\_CTRL.sub\_sync\_load\_enable 1"



#### Figure 13. Enable Time Sync Synchronous Load

5. Issue a synchronous load request by writing a 1 to the **sync\_load\_req** bit (**0xA21[0]**). This will wait for the next Time Sync edge and synchronously load the value to both the Time Clock and Time Sync counters.

### "write TOP.TIME\_SYNC\_TOD.TOD\_SYNC\_LOAD\_REQ\_CTRL.sync\_load\_req 1"

RENESAS	RICBox CLI	—	×
> write TOP.TIME_SYNC_TOD.TOD_SYNC_LC Wrote 1 byte(s) to offset 0xA21	AD_REQ_CTRL.sync_load_req 1		

Figure 14. Issue Synchronous Load Request

## 3.3 Updating the Counters Asynchronously

The Time Sync can be asynchronously updated with the value stored in **async\_adjust\_val (0xA0C[12:0]**). Write a 1 to the **async\_adjust\_req** bit **(0xA0E[0])** to update the Time Sync counter as soon as it is possible to do so.

"write TOP.TIME\_SYNC\_TOD.TOD\_ASYNC\_ADJUST\_VAL\_CTRL.async\_adjust\_val <NEW VALUE>"

"write TOP.TIME\_SYNC\_TOD.TOD\_ASYNC\_ADJUST\_REQ\_CTRL.async\_adjust\_req 1"

 RICBox CLI
 ×

 > write TOP.TIME\_SYNC\_TOD.TOD\_ASYNC\_ADJUST\_VAL\_CTRL.async\_adjust\_val 0
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Figure 15. Asynchronous Time Sync Adjustment

## 4. Outputting the Count Signals

The counts can be outputted as clock signals from either the GPIO or output pins. The output pins can divide the frequency down further if needed, allow flexibility in output signal type, and have configurable Time Sync clock pulse widths. The GPIOs only output 1.8V CMOS signals with unchangeable pulse width.

### 4.1 Output From GPIO

1. Enable the time sync TDC.

	Time Sync TDC
None	Time Sync TDC
	Time Sync TDC Enable 🗹 🔒
	TDC Measurement Start
	TDC Measurement Mode Continu V
	MUX 1 Source Select 🐠 ref_clk< 🔻
	MUX 2 Source Select 🐠 REF<0> 🗸 🖬

Figure 16. Enable Time Sync TDC

2. Enable TOD clocks to the TDC.

inte syne roe	
Time Sync TDC Enable	<b>8</b>
TDC Measurement Start	aî .
TDC Measurement Mode Contin	nu
MUX 1 Source Select 🔥 ref_clk	
MUX 2 Source Select	0> v <b>d</b>
DPLL FB to TDC config	Time Clock/Sync Config
DPLL FB to TDC config TDC Mux sel DPLL0 f ~ 1	Time Clock/Sync Config Time Clock Divided to TDC enable
DPLL FB to TDC config TDC Mux sel DPLL0 f v ff	Time Clock/Sync Config Time Clock Divided to TDC enable Time Sync to TDC enable
DPLL FB to TDC config TDC Mux sel DPLL0 f v f enb f setb f	Time Clock/Sync Config       Time Clock Divided to <ul> <li></li></ul>

Figure 17. Allow TOD Clocks as Input to Time Sync TDC

3. Set the TDC references to the TOD counters.

Ti	ne Sync TDC	
Time Sync TDC Enab	le 🗹 🔒	
TDC Measurement	Node Continu V	
MUX 1 Source Selec	time_sync 🖌 🔒	
MUX 2 Source Select	time_clk 👻 🔒	
	REF<1>	
	REF<2>	
	REF<3>	
	ref_clk<5>	
	ref_clk<6>	
DPLL FB to TDC config	dpll_fb_to_tdc (as selected by dpll_fb_tdc_mux_sel, undivided) dpll_fb_divided_to_tdc (as selected by dpll_fb_tdc_mux_sel, divided)	
TDC Mux sel DPLL0 f v	time_clk_divided	1
	time_sync	
		_

### Figure 18. Select TDC Input Clocks

 Set GPIO function to either tdc\_clk[6] or tdc\_clk[7] depending on which clock needs to be outputted from the GPIO. The tdc\_clk[6] corresponds to the mux source 1 and tdc\_clk[7] is mux source 2 in the TDC block.

RENESAS		GPIO2			×
i 🗄 💀 🤤 🔍					
	GPIC	02 options			
function mode / drive strength disable disable p enable i	tdc_clk[6] (outp CMOS Output moo e pull up  f  f  ull down  f  a  b  c  f  f  f  f  f  f  f  f  f  f  f  f	ut) (set gpio_resync to 0) le and power supply of 1 enable resync [ deglitcher bypass ]	8V. ×	â	

#### Figure 19. Set GPIO Output as TDC Reference



Figure 20. 1Hz Count GPIO Output



Figure 21. 3Hz Count GPIO Output

## 4.2 Output From Out Pin

The Time Clock and Time Sync counters can be outputted using Out8–11 pins.

- 1. Select the **iod\_mux\_sel** source of the corresponding output as Time Clock or Time Sync in RICBox. Then configure the output frequency goal in the main block diagram. The counters can be divided down using the corresponding integer output divider (IOD).
- 2. In RICBox, click on Out8–11 block and select the IOD input reference from the drop-down menu on the left side of the pop-up page.



Figure 22. Configure Out8 to Use TOD Reference

3. The pulse width for the Time Sync outputs is configured using **time\_sync\_width (0xA02 [5:0])** register set. This can be configured in RICBox using the dropdown menu in the TOD and Synthesis block.

				TOD			
	Ті	ime Clock Source	Sub-Sy	nc Pulse Counter			Sync
			Synchronous Load Request	Sub-Sync Counter Load Enable		Synchron Req	ous Load
			Sub-Sync Counter Load Value	0x0000000	B	Sync Cou	nter Load Value
	Time Clock Generation Counter	0x13	Time Sync Generation Counter	0x017D783F	ſ	•	
	Time Clock Frequency Goal	25MHz 🔒	Time Sync Frequency Goal	1Hz	1 time clock cy 2 time clock cy	cle cle	
					4 time clock cy	cle cle	
					16 time clock c	ycle 👔	
					32 time clock c	ycle	
: Delay t	to TDC				64 time clock c	ycle	
Delay					128 time clock	cycle	
					256 time clock	cycle	time
(	0x0				512 time clock	cycle	<b>→</b> :
					1024 time cloc	k cycle	
e Clock 🛛	Delay Bypass 🗹 🖬				2048 time cloc	k cycle	
					4096 time cloc	k cycle	
					8192 time clock	k cycle	
					16 384 time clo	ock ovela	То
				Time Sync Pulse Width Select	1 time clock cyc	e 🎽 🖬	



# 5. Revision History

Revision	Date	Description
1.00	May 7, 2025	Initial release.

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