How to Steer FemtoClock3-Wireless Outputs with a 1Hz Input Clock

This document describes how to control phase and frequency accuracy of outputs in relation to a 1Hz input clock to FemtoClock3-Wireless (FC3W) devices.

Contents

1. Overview

FC3W devices can measure a 1Hz input clock phase with respect to an internal 1Hz reference clock. This information can be used to offset the phase and frequency of the outputs using digital control. The phase measurement should run continuously to maintain the input to output phase relationship.

External software is needed to control the phase measurement, interpret measurement information, and control output phase and frequency. Other device configuration settings can be set statically in the device memory. Continuous phase measurements are necessary to maintain the input to output phase relationship.

Note: FC3W devices cannot use a 1Hz input clock as a direct input to an internal DPLL. The minimum DPLL input reference frequency is 1KHz.

To configure the device, three functional blocks must be set up. The Time-of-Day Counter (TOD), the Time Sync Channel Time to Digital Converter (TSTDC), and the Time Sync Channel Digitally Controlled Oscillator (TS_DCO). The TSTDC will perform the input phase measurement and the TS_DCO can apply a phase and frequency control to the APLL or FODs. The TOD is used to generate the internal 1Hz and essential time-stamp information.

Note: Serial communications in this document are formatted as 2 bytes with the address followed by the data. Writes are <2-byte offset>, <data to be written>. Reads are <2-byte offset>, <estimated data read back>.

Note: All registers in this document can be found in the device programming guide.

1.1 Time-of-Day Counter (TOD)

The TOD has two count values that are based on the rising edges of two internal clocks: The time clock and the time-sync clock. These clocks are derived from an FOD output. The TOD can get its reference from any of the FODs in the device, but the FOD must be outputting between 500MHz to 625MHz to meet the TOD input requirement.

The time clock is an integer divided frequency from FOD reference with a maximum divider value of 64. The time-sync clock frequency is integer-divided from the time clock and can be configured to 1Hz. The time-sync clock is used for the phase measurement comparison to the 1Hz input.

1.2 Time Sync Time to Digital Converter (TSTDC)

FC3W devices can use the internal TSTDC for an input phase measurement. The phase difference is measured between two separate input references. Both input references must be the same frequency and less than 33MHz.

The TSTDC uses two measurement clocks: TDC coarse and TDC fine. The number of rising edges of each measurement clock is counted between one rising edge of each input reference clock. The TDC fine measurement clock comes directly from the TDC APLL output. The TDC coarse measurement clock is divided down from an FOD input reference.

Note: The same FOD used for input to the TOD should also be used as reference for the TDC course clock.

Once coarse and fine values have been read, the offset between the two input clocks can be calculated as:

$$Offset = \left(\frac{tdc\_coarse\_meas}{F_{TDCCoarse}} \times\right) + \left(\frac{tdc\_fine\_meas}{62 \times F_{TDCFine}}\right)$$

Figure 1. TSTDC Measurement Formula

Where:

- tdc_coarse_meas is read from TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_coarse; this value is **signed**.
- tdc_fine_meas is read from TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_fine; this value is **signed**.

- $F_{TDCCoarse}$ is TDC coarse measurement clock frequency.
- $F_{TDCFine}$ is the TDC APLL clock frequency.

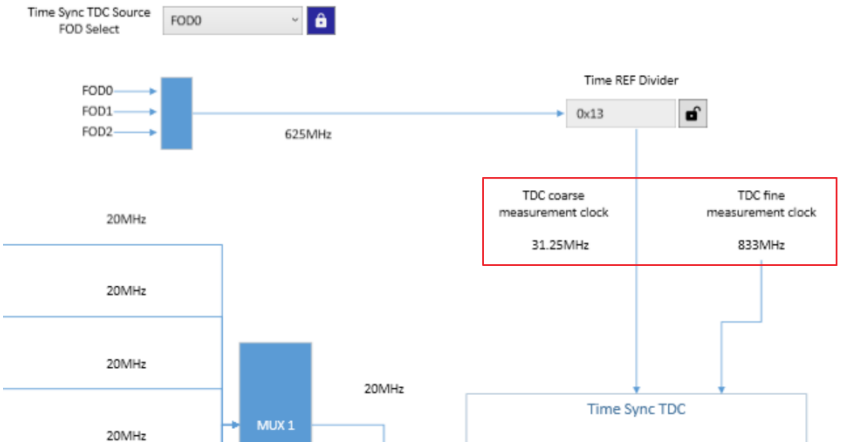

Figure 2. TDC Coarse and TDC Fine Clocks

Note: TSTDC measurements read backs are not always error-free. Data that is read back from the TSTDC should be monitored for accuracy and repeated measurements may be necessary.

1.3 Time Sync Digitally Controlled Oscillator (TS_DCO)

The TS_DCO is used to digitally control the phase and frequency of the FODs and APLL through the combo bus. Phase and frequency information can be applied using either instantly or through a timed adjustment. The initial locking procedure will require timed adjustments to gradually change the output characteristics.

2. RICBox Setup

2.1 RICBox TOD Setup

The TOD can be configured in RICBox from the “TOD and Synthesis” block in the block diagram. Ensure that a FOD is configured for 500MHz to 625MHz and enabled before setting up the TOD. In RICBox:

1. Click the block diagram button on the tool bar pane then the TOD and Synthesis block.

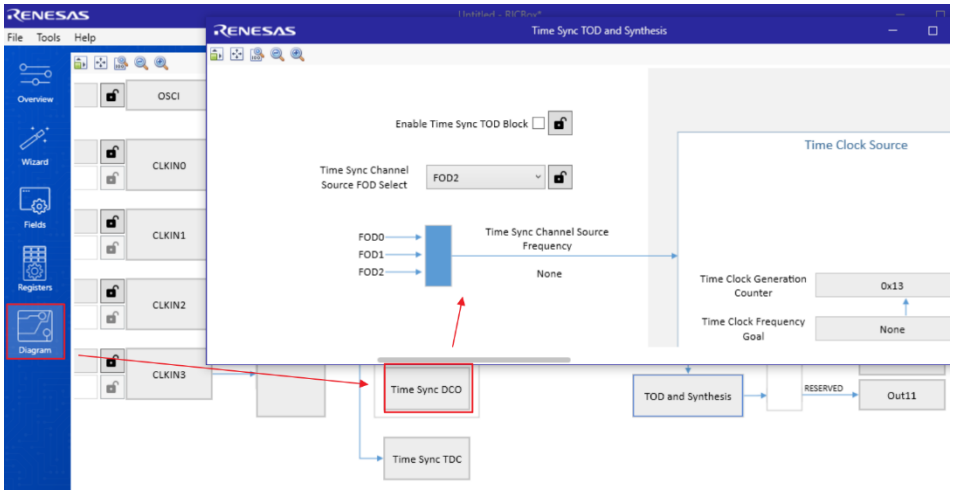

Figure 3. TS_DCO Block

2. Enable the time sync and TOD block.

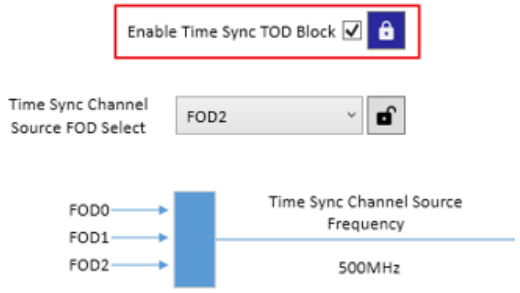

Figure 4. Enable Time Sync TOD Block

3. Select the FOD reference.

   Note: This must be an enabled FOD that is outputting from 500MHz to 625MHz.

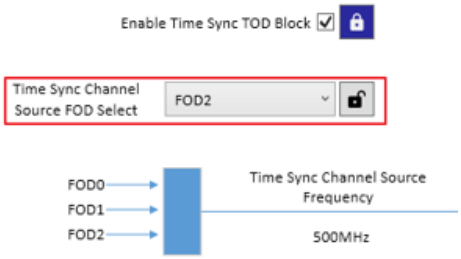

Figure 5. Select TOD Reference Clock

4. Configure the Time Clock Goal Frequency.

   Note: A RICBox error is triggered when the Time Clock Goal Frequency is set initially. This forces users to configure the Time Sync Frequency Goal as well.

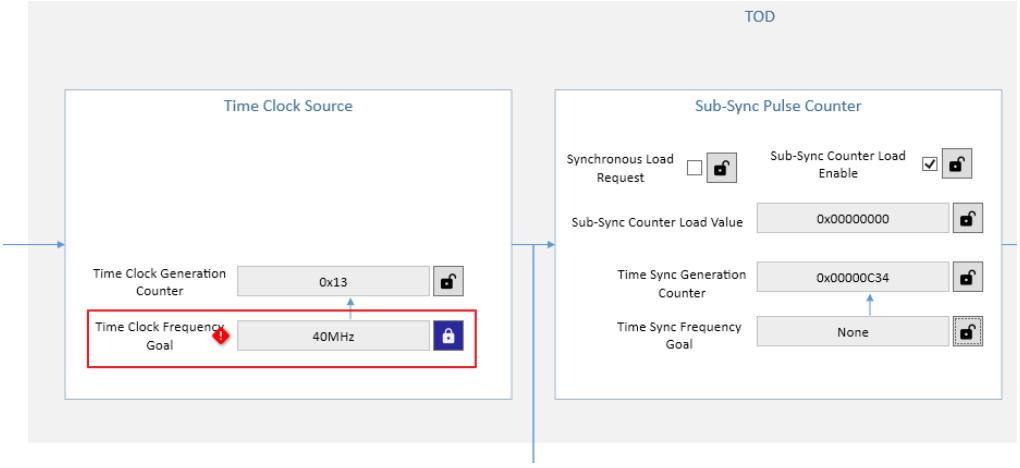

Figure 6. Set Time Clock Frequency Goal

5. Configure the Time Sync Goal Frequency to 1Hz.

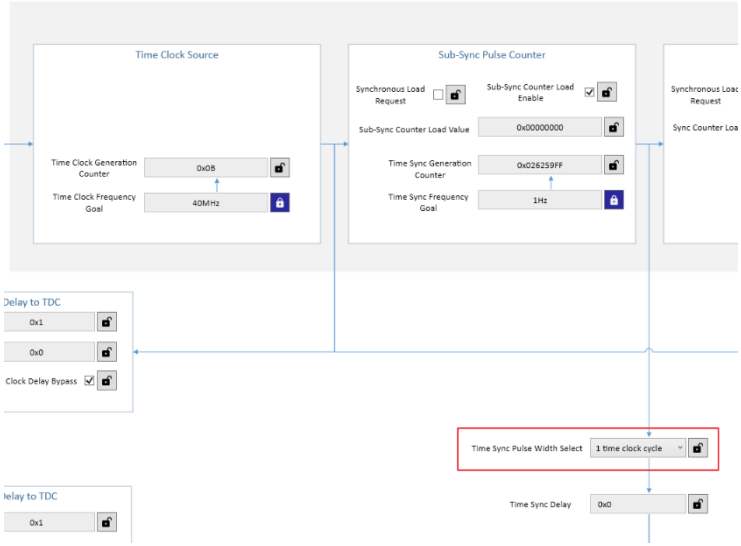

Figure 7. Set Time Sync Frequency Goal

6. *Optional*: Adjust the pulse width of the 1Hz time sync clock. The pulse width defaults to one time clock cycle.

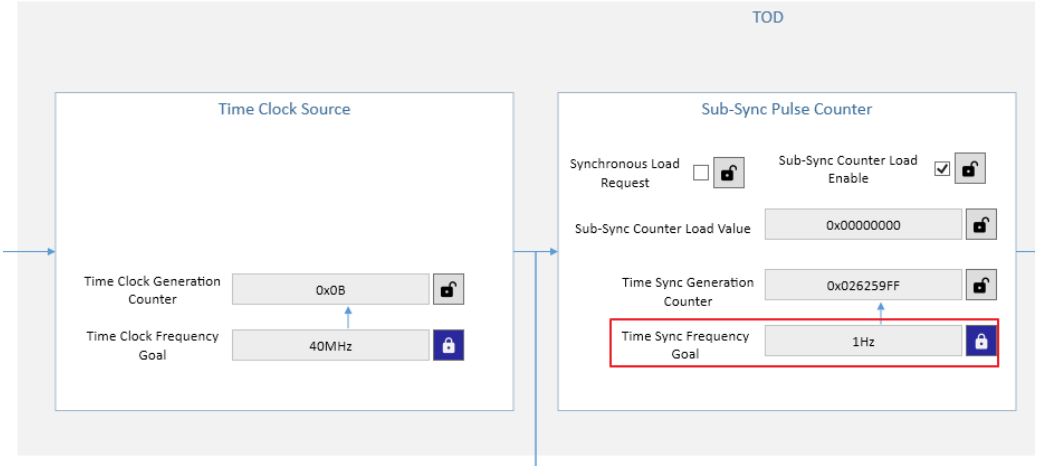

Figure 8. Change Time Sync Pulse Width

2.2 RICBox TSTDC Setup

Before setting up the TSTDC, ensure a CLKIN input reference is configured for comparison. For 1Hz inputs, use LVCMOS DC coupled input type. REF 5 and REF 6 in the references block are reserved for TSTDC input.

To set up the TSTDC for measurement in RICBox, configure the following:

1. Go to the Time Sync TDC block.

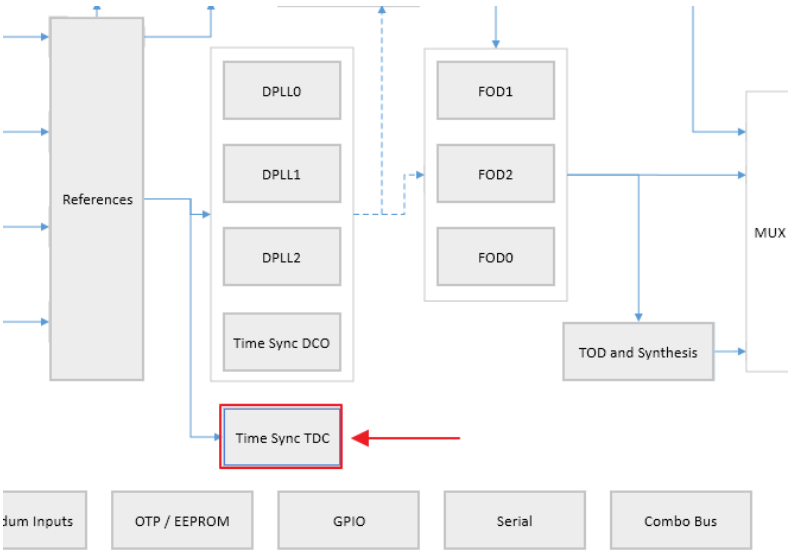

Figure 9. TSTDC Block

2. Set up the TDC coarse clock by selecting an FOD input reference. RICBox will configure the divider value automatically.

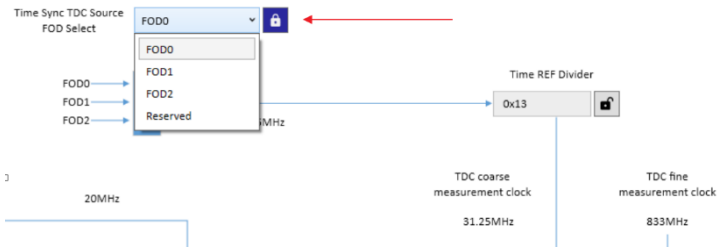

Figure 10. Select TSTDC Reference Clock

3. Enable the time sync TDC.

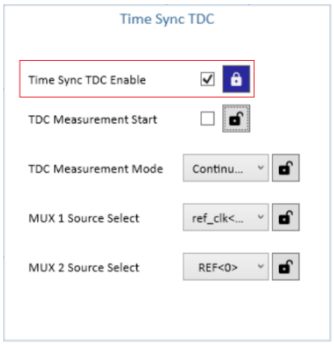

Figure 11. Time Sync TDC Enable

4. Select Continuous for TDC Measurement Mode.

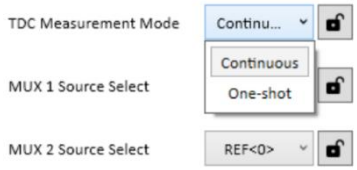

Figure 12. TDC Measurement Mode Continuous

5. Select time sync as a reference to compare to the 1Hz TOD time sync clock that was previously set up. Then select the input reference that corresponds to the external 1Hz clock for the other mux source.

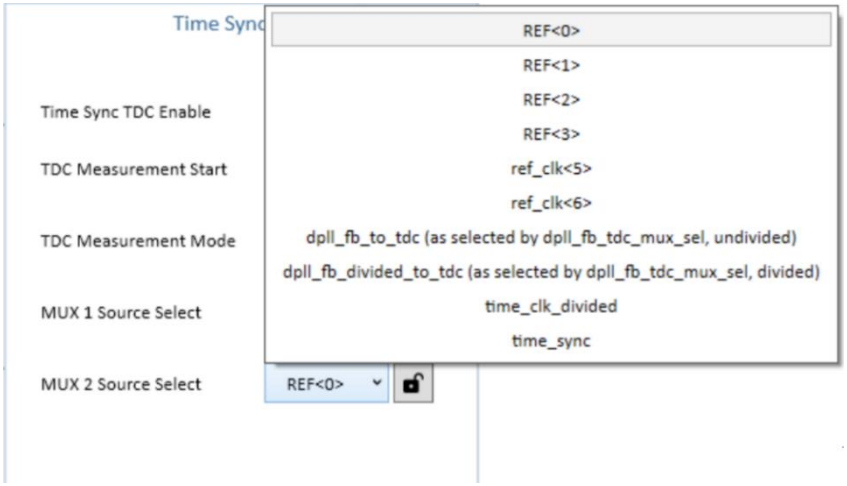

Figure 13. Select TSTDC Measurement Clocks

6. Check off the Time Sync to TDC Enable box.

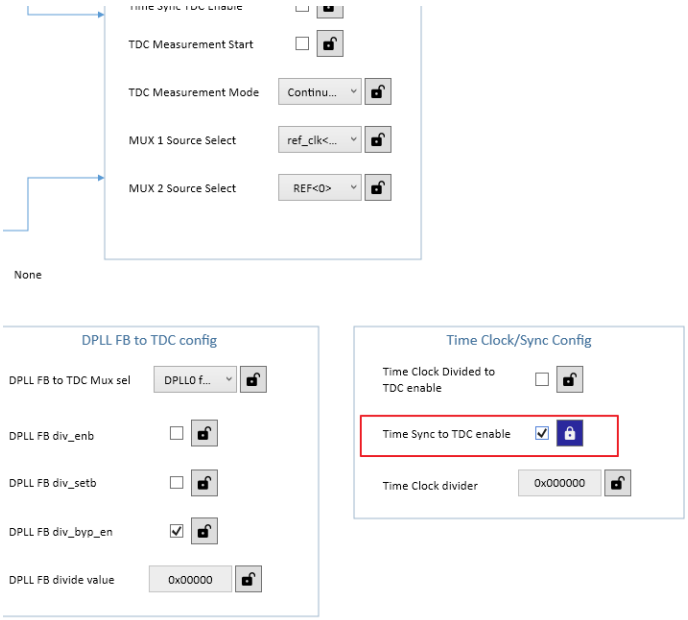

Figure 14. Time Sync to TDC Enable box

2.3 RICBox TS_DCO Setup

The TS_DCO can be accessed from the Time Sync DCO block in the main GUI diagram.

1. Go to the Time Sync DCO block.

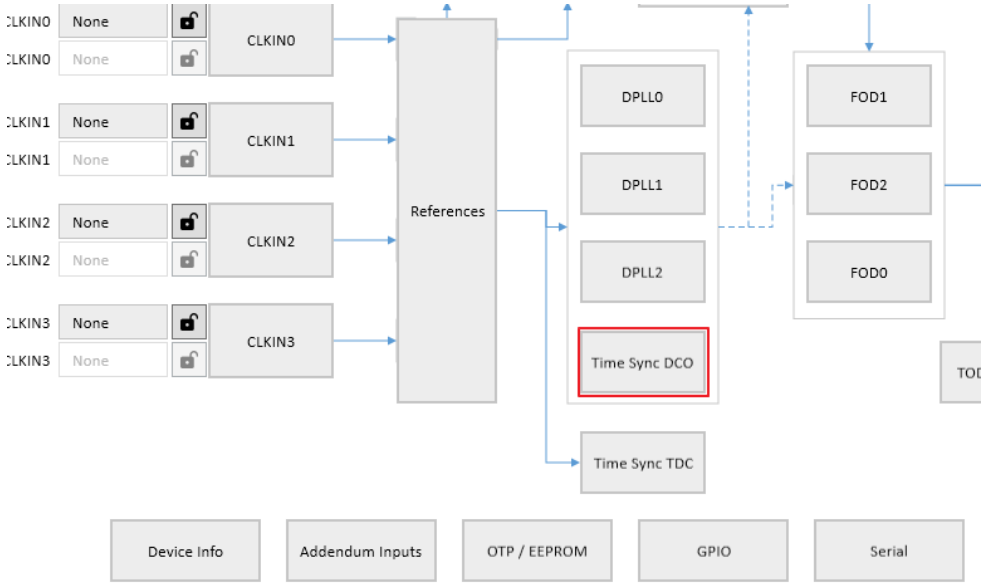

Figure 15. TS_DCO Block

2. Change the TS DCO mode to “Forces the filter into Write Frequency mode”.

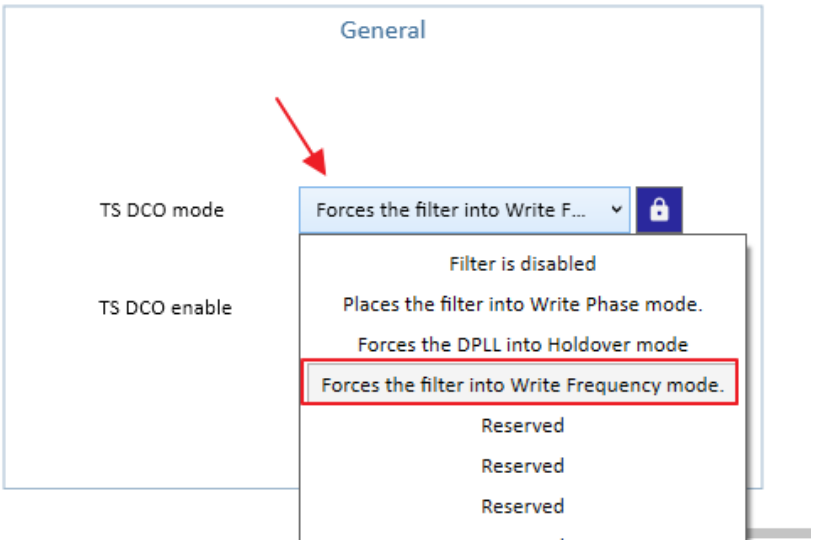

Figure 16. TS_DCO Mode Selection

3. Check the TS DCO enable box.

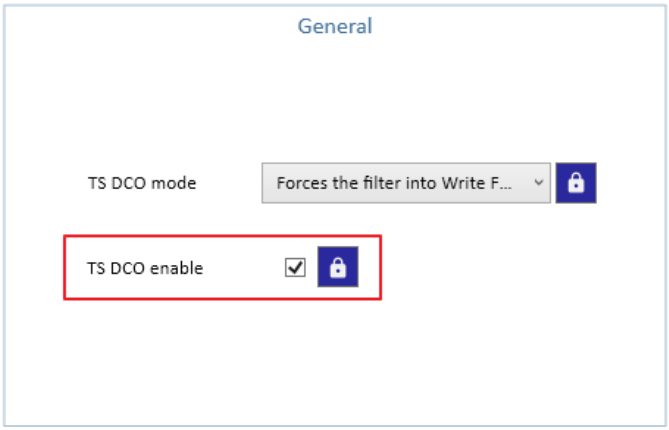

Figure 17. TS_DCO Enable

4. Click on the TS to LPF for Write Phase block.

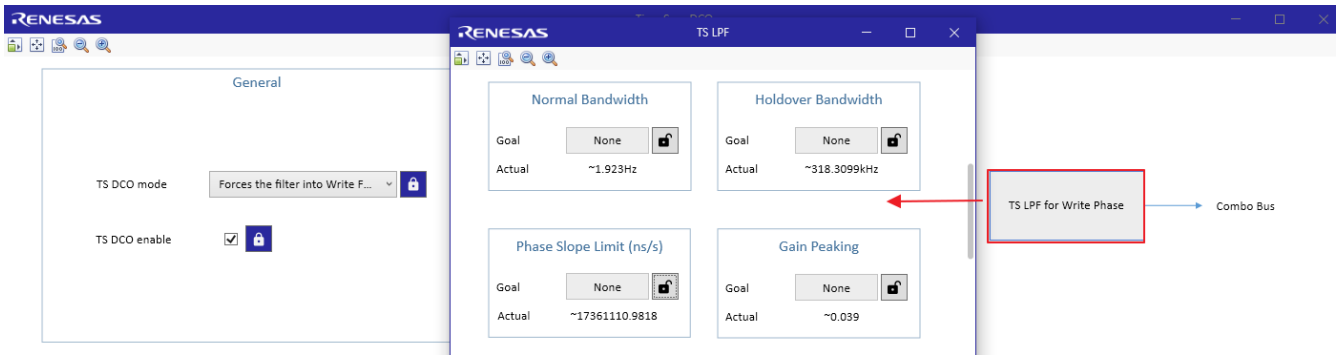

Figure 18. TS_DCO LPF Settings

5. Set up the normal bandwidth, Holdover Bandwidth, Phase Slope Limit, and Gain peaking for the 1Hz phase lock requirements.
6. From the main block diagram, click on the Combo block.

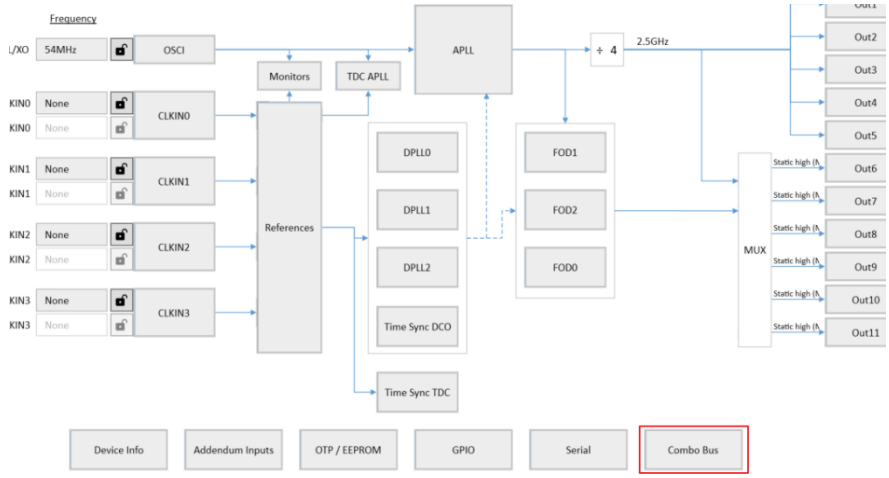

Figure 19. Combo Bus Block

7. Check off the box to allow the TS_DCO to control the FOD that the TOD uses as its reference.

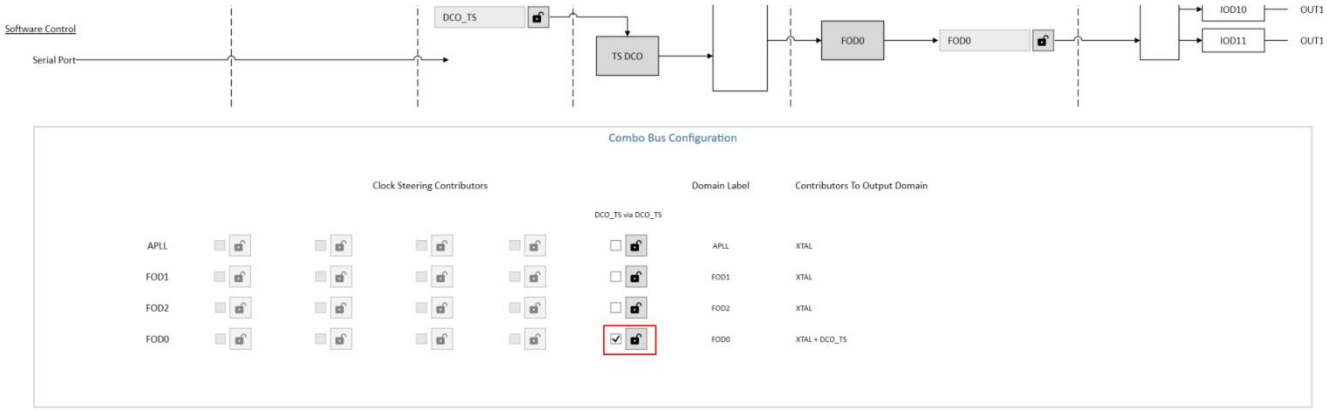

Figure 20.Combo Bus Settings

3. Register Writes Setup Examples

3.1 TOD Setup Serial Writes Example

This is a serial writes example that selects FOD0 as the TOD input, divides 625MHz to 32.5MHz time clock, configures time sync clock to 1Hz, and enables the TOD block.

```
# write TOP.TIME_SYNC_TOD.TIME_CLOCK_GEN_CNFG.time_clock_src: 0x0
write 0A 00, 13 00
# write TOP.TIME_SYNC_TOD.TIME_CLOCK_GEN_CNFG.time_clock_gen_count: 0x12
write 0A 00, 12 00
# write TOP.TIME_SYNC_TOD.SUB_SYNC_GEN_CNFG.sub_sync_count: 0x01EFE91F
write 0A 04, 1F E9 EF 01
# write TOP.TIME_SYNC_TOD.TOD_ENABLE_CTRL.enable: 0x1
write 0A 0A, 01
```

The enable bit is written last. This is so the device's function is unaffected if the TOD is being configured in real-time.

The value for "time_clock_gen_count" is the calculated as (FOD frequency / desired time clock frequency) - 1. Whereas the "sub_sync_count" value is calculated as (time clock frequency / desired time-sync frequency) - 1.

3.2 TSTDC Setup Register Writes Example

This register write example shows setting up a FOD as coarse clock source, measurement mode to continuous, selecting REF5 as one input and time sync clock as another, and enabling the TDC measurement.

```
# write TOP.TIME_SYNC_TOD.TIME_CLOCK_GEN_CNFG.time_clock_src: 0x0
write 0A 00, 13 00
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_MEAS_DIV_CNFG.time_ref_div: 0x13
write 0B 08, 00 00 00 13
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_MEAS_CNFG.tdc_meas_mode: 0x0
write 0B 04, 01
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_TDC_FANOUT_CNFG.sig1_mux_sel: 0x4
write 0B 00, 40 30 03 03
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_TDC_FANOUT_CNFG.sig2_mux_sel: 0x9
write 0B 00, 40 39 03 03
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_TDC_FANOUT_CNFG.time_clk_to_tdc_en: 0x1
```

```
write 0B 00, 42 39 03 03
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_TDC_FANOUT_CNFG.time_sync_to_tdc_en: 0x1
write 0B 00, 43 39 03 03
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_MEAS_CTRL.tdc_meas_en: 0x1
write 0B 10, 01
```

3.3 TS_DCO Register Writes Example

This example configures the TS_DCO for write phase mode and enable it. Then allows the TS_DCO to apply its combo bus information to the FOD that supplies the TOD reference. It is important that the internal 1Hz clock can track updates from the TS_DCO.

```
# write TOP.TIME_SYNC_LPF.LPF_MODE_CNFG.lpf_mode: 0x1
write 0A 80, 01
# write TOP.TIME_SYNC_LPF.LPF_CTRL.lpf_en: 0x1
write 0A 98, 31
# write TOP.TIME_SYNC_LPF.LPF_DIS_CTRL.lpf_filter_dis: 0x0
write  0A 99, 00
# write TOP.FOD[0].FOD_CNFG.fod_ts_delta_freq_op: 0x2
write 03 00, 54 00
```

4. Implementation

4.1 Initial Locking Procedure

The initial lock to a 1Hz input requires gradual phase and frequency adjustments. The adjustments are repeatedly applied to the outputs so they can match the 1Hz input in both phase and frequency. This occurs in three steps listed in order of execution:

1. Phase snap – Adjust the TOD to phase align the internal 1Hz with the external 1Hz CLK input.
2. Frequency correction – Measure the frequency offset between the internal 1Hz clock and external. Use the TS_DCO to apply a frequency correction to the outputs.
3. Phase correction – Use the TS_DCO to apply a timed frequency correction to the outputs.

The phase snap is completed first to set up future phase and frequency measurements. If the internal 1Hz clock is too far out of frequency from the external clock, then the phase snap is necessary. A frequency correction would not allow the two clocks to align properly.

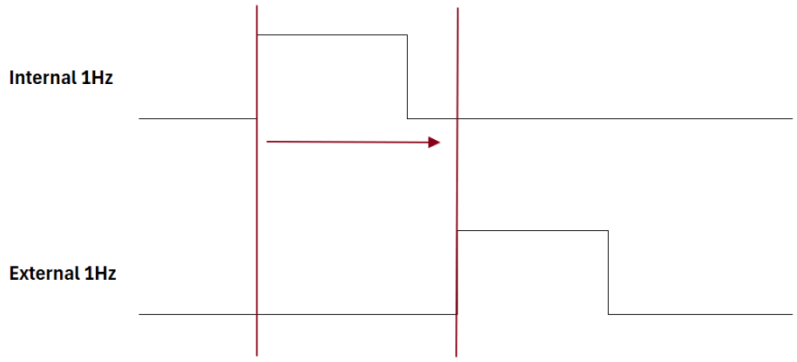

Figure 21. Phase Snap

A phase drift is expected because the two clocks are not frequency aligned. As the two clocks drift in phase from each other, the TSTDC can measure the phase offset at two separate points in time, then compare the two points to calculate the frequency offset between the two clocks. The TOD can be read for accurate time stamp information when calculating the frequency offset.

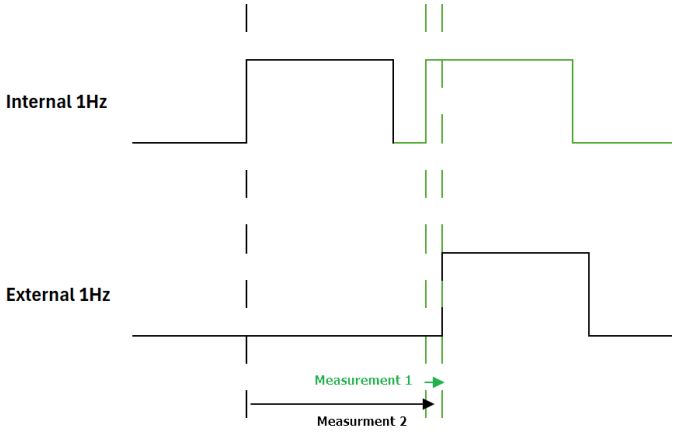

Figure 22. Frequency Measurement

A frequency correction is done to align the outputs to the frequency of the 1Hz input. Then the phase is corrected so the outputs can match the phase of the 1Hz input.

For the examples, a phase snap threshold of 5ms and frequency threshold of 10ppb are used.

4.1.1 Phase Snap

1. Enable the TSTDC measurement then read back the coarse and fine values.

```
# write TOP.TIME_SYNC_TDC.TIME_CLOCK_MEAS_CTRL.tdc_meas_start: 0x1
write 0B 10, 02
# write TOP.TIME_SYNC_TDC.TDC_FIFO_READ_REQ.fifo_read_req: 0x1
write 0B 2F, 01
# read TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_fine: 0x0000
# read TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_coarse: 0x0000000
read 8B 30, 00 00 00 00 00 00 00 00
```

2. Read the TOD count value. This will be used as a time stamp for the TSTDC measurement.

```
# read TOP.TIME_SYNC_TOD.TOD_COUNTER_STS.sync_counter_value: 0x0000000000000
# read TOP.TIME_SYNC_TOD.TOD_COUNTER_STS.sub_sync_counter_value: 0x00000000
read 8A 5F, 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

3. Check if the TSTDC measured phase offset is within the phase snap threshold. If the measured phase is within the threshold, then the next steps can be skipped. Go directly to the frequency correction phase.
4. Apply the TSTDC measured time to TOD measurement and program the TOD to the new value. This will adjust the internal 1Hz clock.

```
# write TOP.TIME_SYNC_TOD.TOD_SYNC_LOAD_EN_CTRL.sync_load_enable: 0x1
write 0A 20, 01
# write TOP.TIME_SYNC_TOD.TOD_SYNC_LOAD_VAL_CTRL.sub_sync_counter_load_val:
0x0000FFFF
write 0A 10, FF FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00
# write TOP.TIME_SYNC_TOD.TOD_SYNC_LOAD_REQ_CTRL.sync_load_req: 0x1
write 0A 21, 01
```

5. Wait 3 seconds for the TOD update then flush the TDC measurement.

```
# write TOP.TIME_SYNC_TDC.TDC_FIFO_CTRL.fifo_clear: 0x1
write 0B 12, 01
```

4.1.2 Frequency Correction

1. Get the TDC measurement and TOD time stamp (see steps 1 and 2 of “Phase Snap”).
2. If this is the first measurement, then wait 3 seconds and go back and collect the TSTDC and TOD information again.
3. Calculate the frequency offset.

   (second measurement - first measurement) / (second TOD time - first TOD time)
4. Apply calculated value to TS_DCO as a frequency control word.

```
# write TOP.TIME_SYNC_LPF.LPF_MODE_CNFG.lpf_mode: 0x3
write 0A 80, 03
# write TOP.TIME_SYNC_LPF.LPF_WR_FREQ_CTRL.lpf_wr_freq: 0x000000000
write 0A B0, 00 00 00 00 00 00 00 00
```

5. Check to see if the TSTDC measurement is within the phase snap threshold. If it is not, then go back to Phase Snap.
6. Check to see if the calculated frequency exceeds the frequency lock threshold. If yes, then repeat frequency correction. The Frequency was adjusted but it is still off. This will gradually adjust the frequency of the internal 1Hz to the external input.

4.1.3 Phase Correction

1. Get the TDC measurement and TOD time stamp (see steps 1 and 2 of “Phase Snap”).

   Check to see if the TSTDC measurement is within the phase snap threshold. If it i not, then go back to Phase Snap.
2. Apply phase timed phase correction using the TS_DCO.

```
# write TOP.TIME_SYNC_LPF.LPF_MODE_CNFG.lpf_mode: 0x1
write 0A 80, 01
# write TOP.TIME_SYNC_LPF.LPF_WR_FREQ_PHASE_TIMER_CNFG.lpf_write_timer_val: 0xFFFF
write 0A 88, FF FF 00 00
# write TOP.TIME_SYNC_LPF.LPF_WR_FREQ_PHASE_TIMER_CNFG.lpf_timer_en_write_freq: 0x1
write 0A 88, 00 00 02 00
```

3. Wait 3 seconds to complete phase correction.
4. Then flush the TDC measurement.

```
# write TOP.TIME_SYNC_TDC.TDC_FIFO_CTRL.fifo_clear: 0x1
write 0B 12, 01
```

5. Check to see if phase adjustment is greater than phase lock threshold.
   a. If yes, then repeat phase adjustment.
   b. If no, then the device is locked to the input.

4.2 Maintain Lock

Ensure that the phase control word is programmed to 0 before starting the Maintain Lock phase.

1. Get TDC measurement and TOD time stamp (see steps 1 and 2 of “Phase Snap”).
2. Check if TDC measurement exceeds the phase lock threshold. If yes, then go to holdover.
3. Apply phase offset to the TSTDC with write phase.

```
# write TOP.TIME_SYNC_LPF.LPF_MODE_CNFG.lpf_mode: 0x1
write 0A 80, 01
# write TOP.TIME_SYNC_LPF.LPF_WR_PHASE_CTRL.lpf_wr_phase: 0x000FFFF
write 0A A8, FF FF 00 00 00 00 00 00
```

4. Repeat from step 1 continuously.

4.3 Holdover

1. Get TDC measurement and TOD time stamp (see steps 1 and 2 of “Phase Snap”).

   Check if TDC measurement exceeds the phase lock threshold. If yes, then check to see if the device has been in holdover for too long. Compare the TOD measurement with the holdover time threshold.

   a. If yes, then go back to phase snap. Loss of lock has occurred.

   b. If no, then continue holdover.
2. Apply the measured phase offset to the TSTDC write phase (see step 3 of “Maintain Lock”).
3. The device is locked, go back to the Maintain Lock phase.

5. Revision History

Revision	Date	Description
1.00	Sep 27, 2024	Initial release.

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