How to Make 1.2V LVCMOS from 1.8V LVCMOS Output

1. Introduction

LVCMOS logic simply toggles the output of its driver between ground level and VDD rail level. This means that the output amplitude or swing is a function of the VDD rail voltage. The common method for setting the LVCMOS amplitude is to apply the corresponding VDD rail voltage.

Most LVCMOS driver circuits have a certain VDD rail voltage range where requirements are met like output impedance and rise / fall times. When an amplitude is required that is below the low limit of the LVCMOS driver, there will be issues when simply lowering the VDD rail to this low voltage. Fortunately there are alternative methods to control the LVCMOS amplitude that allow amplitudes below the VDD rail low limit for the LVCMOS driver.

1.1 Typical LVCMOS Application

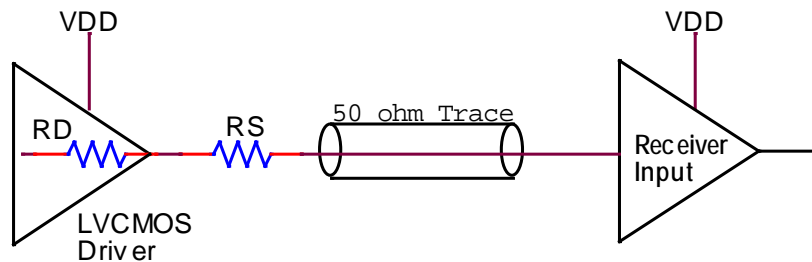The typical LVCMOS driver to LVCMOS receiver input is as displayed in the following figure.

Figure 1. LVCMOS Clock Trace

RS is used to match the LVCMOS driver output impedance (RD) to the 50Ω clock trace. Renesas LVCMOS drivers are typically designed with 17Ω output impedance and need RS = 33Ω to match to a 50Ω clock trace. Some fan-out buffers (and for example, the FemtoClock 2 LVCMOS drivers) have a 50Ω output impedance in the driver so RS is not needed. For the LVCMOS driver output impedance, please check the relevant device datasheet.

This method of terminating a clock trace is called "Source Termination" because the clock trace is terminated at the source (driver) side only. The destination (receiver) side is a high impedance and is not terminated. Using this method, the full ground to VDD swing will appear at the receiver input. The signal integrity of the waveform at the receiver is good while at other places on the clock trace and at the driver side a reflection can be visible.

Below waveforms are from a simulation with a 25MHz 1.8V LVCMOS clock and a 10 inch or 25cm 50Ω clock trace to a receiver input.
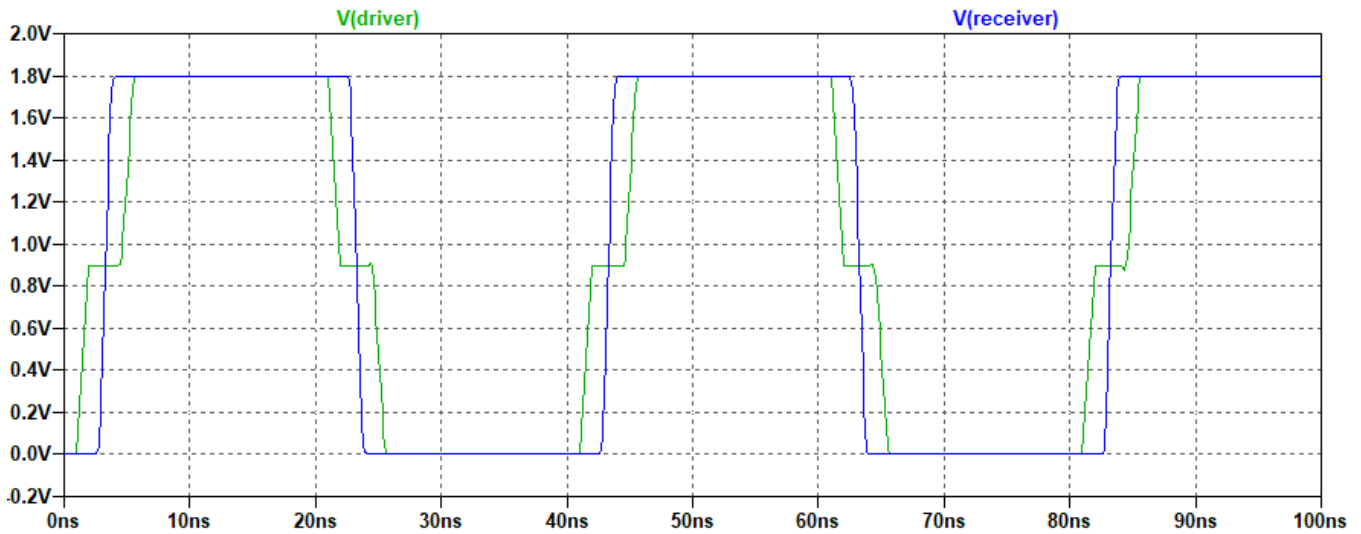

Figure 2. LVCMOS Waveform at Receiver and at Driver Side

Reflections are visible at the driver side but cannot do any harm at that location. What is important is that the waveform at the receiver input has good signal integrity.

1.2   Attenuating the LVCMOS Amplitude

When, for example, the LVCMOS driver cannot operate below 1.8V but the receiver needs a 1.2V amplitude, the LVCMOS waveform needs to be attenuated. The simplest method is a resistor parallel to the receiver input.
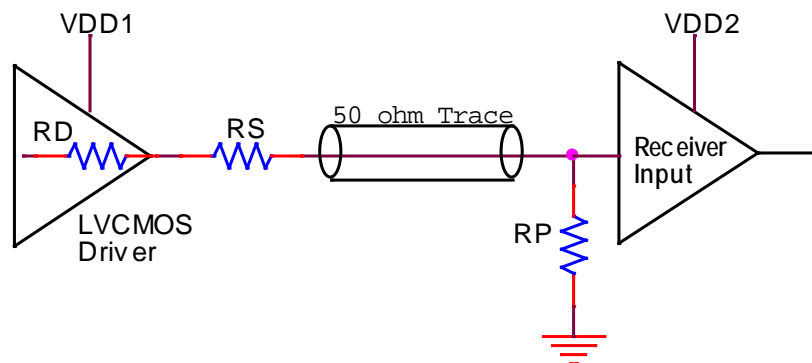

Figure 3. Attenuating LVCMOS

Assuming that the LVCMOS amplitude at the driver is equal to VDD1 and the LVCMOS amplitude needed at the receiver input is VDD2, the formula for finding the parallel resistor RP value is as follows:

(EQ) 1 $RP = 50 \times VDD2 / (VDD1-VDD2)$

Example: VDD1 = 1.8V and VDD2 = 1.2V → RP = 50 × 1.2 / (1.8-1.2) = 100Ω

This formula also assumes a 50Ω trace impedance and RD + RS = 50Ω for proper matching to the clock trace.

The method works for any receiver amplitude below the driver amplitude. In addition to 1.2V LVCMOS, you can also make 1.5V LVCMOS or 1.0V LVCMOS or anything below the 1.8V driver levels by adjusting the RP resistor value.

The following waveforms are from a simulation with a 25MHz 1.8V LVCMOS clock, a 10 inch or 25cm 50Ω clock trace to a receiver input and 100Ω parallel to the receiver input.
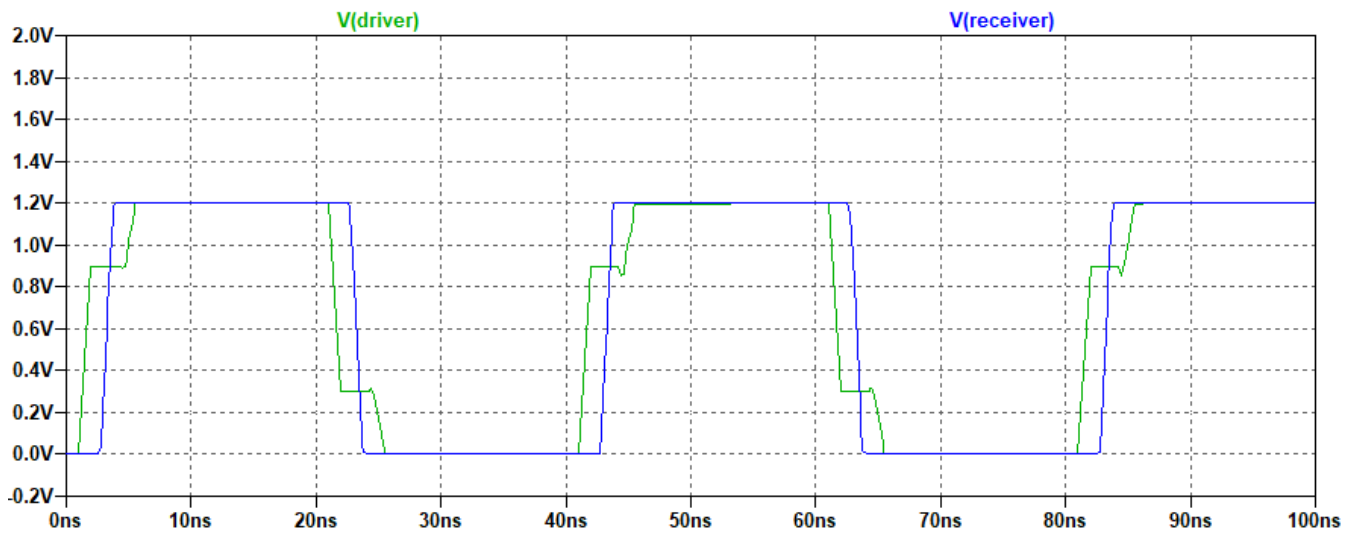

Figure 4. Attenuated LVCMOS Waveform at Receiver and at Driver Side

As predicted by the formula, the amplitude at the receiver input is now 1.2V and signal integrity is still good. The reflections that are visible at the driver side are no longer near the 50% level but can still not do any harm.

2. Measurements
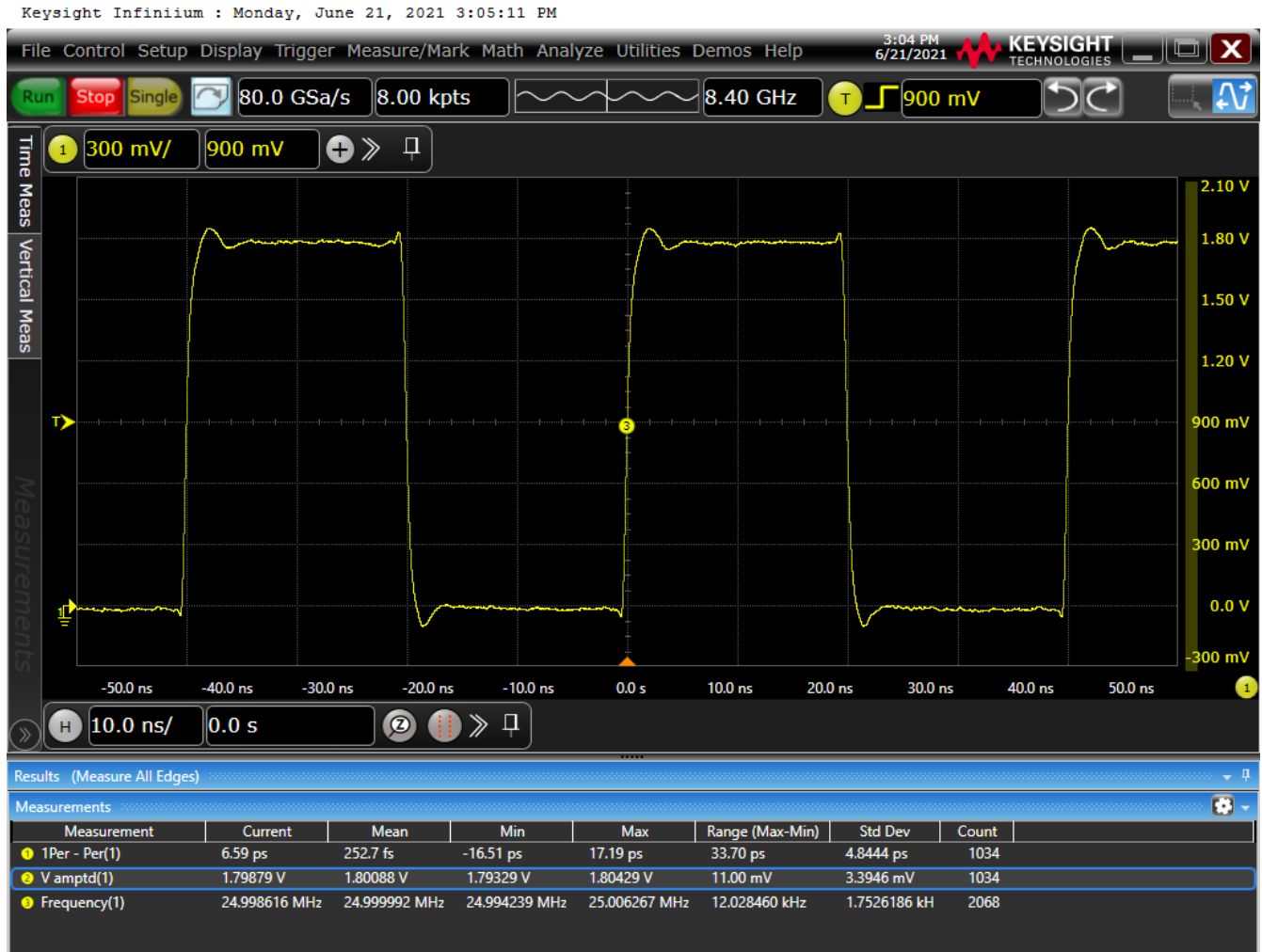
2.1 Typical 1.8V LVCMOS

Figure 5. Typical 1.8V LVCMOS 25MHz Waveform at Receiver Side

Measurements:

- Amplitude = 1.80V
- Frequency = 24.999992MHz
- Cycle-to-Cycle Jitter = 4.84ps RMS, 17.2ps peak

2.2 Adding 100Ω to 1.8V LVCMOS

Adding 100Ω parallel to the receiver input (in this case the Probe to the oscilloscope) to attenuate the waveform to 1.2V.

Figure 6. 1.8V LVCMOS 25MHz with 100Ω added at Receiver Side

The vertical scale for the measurement was adjusted to improve the jitter measurement.

Measurements:

- Amplitude = 1.23V
- Frequency = 25.000000MHz
- Cycle-to-Cycle Jitter = 5.96ps RMS, 20.5ps peak

The resistor parallel to the receiver input does a good job simply lowering the amplitude and not affect other properties of the clock with any significance.

The Cycle-to-Cycle Jitter ("1Per-Per" in the plot) looks a little bit higher because the smaller amplitude also makes the rising and falling edges slower in absolute volts per nanosecond, and as a result, this increases the noise floor of the oscilloscope. The jitter of the clock itself did not change: it is the noise contribution of the oscilloscope that changed. Besides that, the small LVCMOS amplitudes are mostly needed for micro-processor or "compute" applications where this jitter level is well within the requirements.

The frequency changed very little, only 0.3ppm in this case. This is also mostly due to the frequency measurement precision of an oscilloscope. This test was done with a Renesas Frequency Generator IC where

the isolation from the outputs to the crystal is very good. Clock oscillators with one output use much smaller chips where that isolation may be less good. When using this attenuation method with a clock oscillator, some frequency change can be expected.

3.   Conclusion

Adding a single resistor parallel to the LVCMOS receiver input is an effective method to attenuate the LVCMOS amplitude when the VDD on the LVCMOS driver cannot be lowered enough to achieve the desired amplitude.

4.   Revision History

Revision	Date	Description
1.0	Jul 5, 2021	Initial release.

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