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H8S/2200 Series

Using an External Interrupt to Start Counter Incrementation

Introduction

In this application note, the watchdog timer (WDT) is used in interval timer mode and its operation is started by an edge signal input from an external input (IRQ) pin. An 8-bit software counter is incremented each time the watchdog timer overflows.

Target Device

H8S/2215

Contents

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1. Specifications

1. As shown in figure 1, watchdog timer operation (as an interval timer) is triggered by an edge signal input to the $\overline{\text{IRQ0}}$ pin (pin 39).
2. When the watchdog timer overflows, an interrupt is generated and an 8-bit counter in RAM, cnt, is incremented.
3. When cnt reaches H'FF, it is cleared to H'00 and the watchdog timer and cnt are restarted; the timer/counter operation is thus repeated.

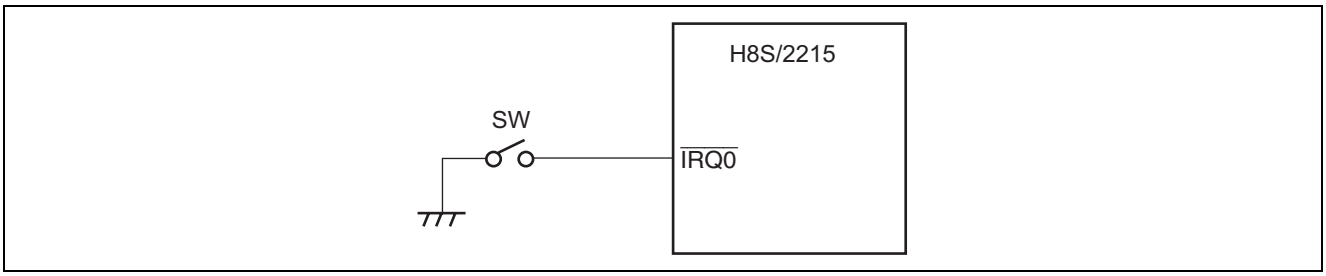


Figure 1 Example of Edge Signal Input to $\overline{\text{IRQ0}}$ Pin

2. Description of Functions

1. Figure 2 shows a block diagram of the interrupt controller, and the following is the description of the interrupt controller registers used in the sample task:
   - The system control register (SYSCR) selects the interrupt control mode, sets the NMI detection edge, enables/disables the $\overline{\text{MRES}}$ pin input and enables/disables the internal RAM.
   - The interrupt priority register x (IPRx; x represents A to G, I to K, and M) sets the priority levels (7 to 0) of interrupts other than NMI. For details on IPR and corresponding interrupt sources, refer to the hardware manual. By setting a value from H'0 to H'7 to bits 6 to 4 and 2 to 0, the priority of the corresponding interrupt is decided.
   - The IRQ enable register (IER) enables IRQ7 to IRQ0 interrupt requests.
   - The IRQ sense control registers H and L (ISCRH and ISCRL) select the conditions for generation of interrupt requests by the $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ pins.
   - The IRQ status register (ISR) consists of IRQ7 to IRQ0 interrupt request flags.

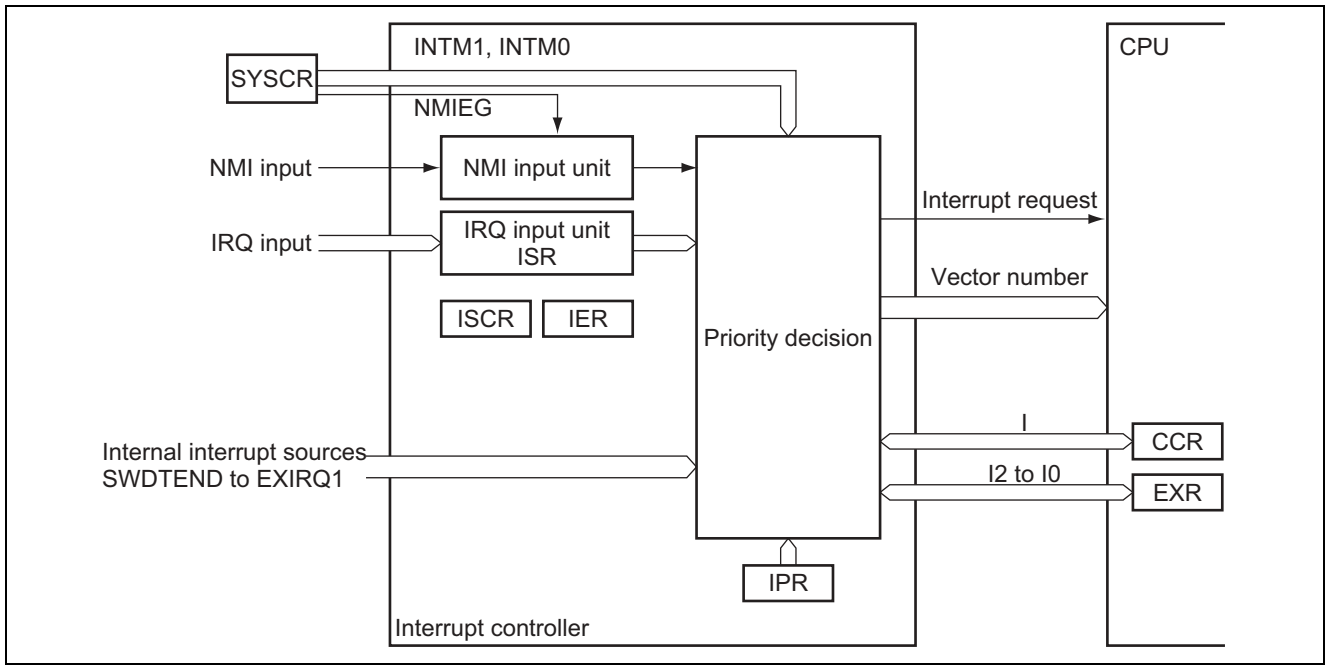


Figure 2 Block Diagram of Interrupt Controller

2. Table 1 shows the assignment of interrupt-related functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
SYSCR	Enables the on-chip RAM and manual resets.
IPRx	Sets the interrupt priority in the range from 7 to 0. The initial setting is 7 for the highest priority level.
IER	Enables IRQ0 interrupts.
ISCRH and ISCRL	Sets to generate interrupts at both edges of the IRQ0 input.
ISR	When an interrupt is generated by an external input signal from the $\overline{\text{IRQ0}}$ pin, the corresponding flag in this register is set.

3. Principles of Operation

Figure 3 shows the principles of operation. This sample task performs count operations through the hardware and software processing shown in the figure.

1. Immediately after a reset, registers are set to configure an interval timer, etc., and the system enters a state waiting for SWONF = 1.
2. When an edge signal (rising or falling) is input to the $\overline{\text{IRQ0}}$ pin (pin 39), the SWONF is set to 1.
3. TCNT of the watchdog timer, which has been set up as an interval timer, starts counting. When TCNT overflows, the 8-bit counter cnt is incremented.
4. After cnt reaches H'FF, it is cleared to H'00, and then TCNT and cnt start counting again.

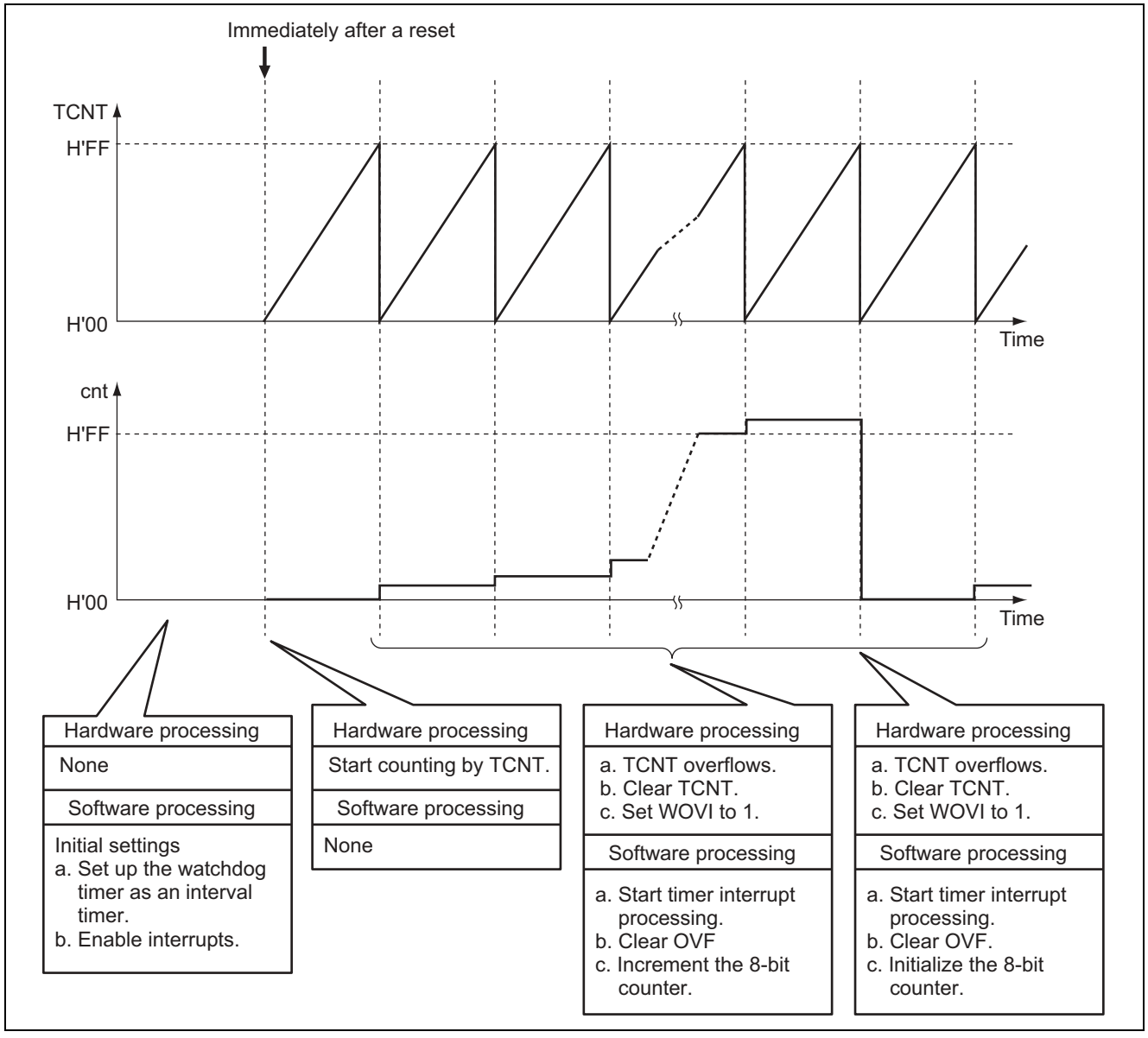


Figure 3 Count Operation Triggered by External Interrupt

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Enables interrupts generated by IRQ0 inputs. After setting up the watchdog timer, enters a state waiting for IRQ0 input.
Count up	intval	Increments or initializes the 8-bit counter (cnt) on an interval timer interrupt of the watchdog timer.
Switch on	Irq0int	IRQ0 interrupt processing routine that sets SWONF to 1.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The interrupt-related internal registers used in this sample task are described in table 3.

Table 3 Description of Internal Registers

Register		Function	Address	Setting
SYSCR	INTM1 INTM0	System Control Register Selects interrupt control mode for the interrupt controller. When INTM1 and INTM0 = 00, interrupt control mode 0 is selected. When INTM1 and INTM0 = 10, interrupt control mode 2 is selected. Note: Setting of 01 or 11 is prohibited.	H'FFFDE5 Bit 5 Bit 4	0, 0
	NMIEG	System Control Register (NMI Edge Select) When NMIEG = 0, an interrupt request is generated at the falling edge of NMI input. When NMIEG = 1, an interrupt request is generated at the rising edge of NMI input.	H'FFFDE5 Bit 3	0
	MRESE	System Control Register (Manual Reset Select) When MRESE = 0, manual reset is disabled. When MRESE = 1, manual reset is enabled.	H'FFFDE5 Bit 2	1
	RAME	System Control Register (RAM Enable) When RAME = 0, the on-chip RAM is disabled. When RAME = 1, the on-chip RAM is enabled.	H'FFFDE5 Bit 0	1
IPRA		Interrupt Priority Register A Bits IPR6 to IPR4 = 111 to 000: Sets priority of the IRQ0 interrupt source. 111 sets the highest priority level (7) and 000 sets the lowest (0).	H'FFFEC0 Bits 6 to 4	1, 1, 1 (Initial value)*

Register	Function	Address	Setting
IER	IRQ Enable Register When IRQnE = 0, interrupt requests are disabled. When IRQnE = 1, interrupt requests are enabled. (n: 7 to 0)	H'FFFE14	H'04
ISCRL	IRQ Sense Control Registers L When bits IRQ0SCB and IRQ0SCA = 11, interrupt requests are generated at both of the falling and rising edges of the $\overline{\text{IRQ0}}$ input.	H'FFFE13	H'03
ISR	IRQ Status Register When IRQnF = 0, the interrupt source has not been detected. When IRQnF = 1, the interrupt source selected with ISCR has been detected. (n: 7 to 0)	H'FFFE15 Bits 7 to 0	0 for each bit

Note: * "Initial value" indicates the value before setting is made by this program.

4.4 RAM Usage

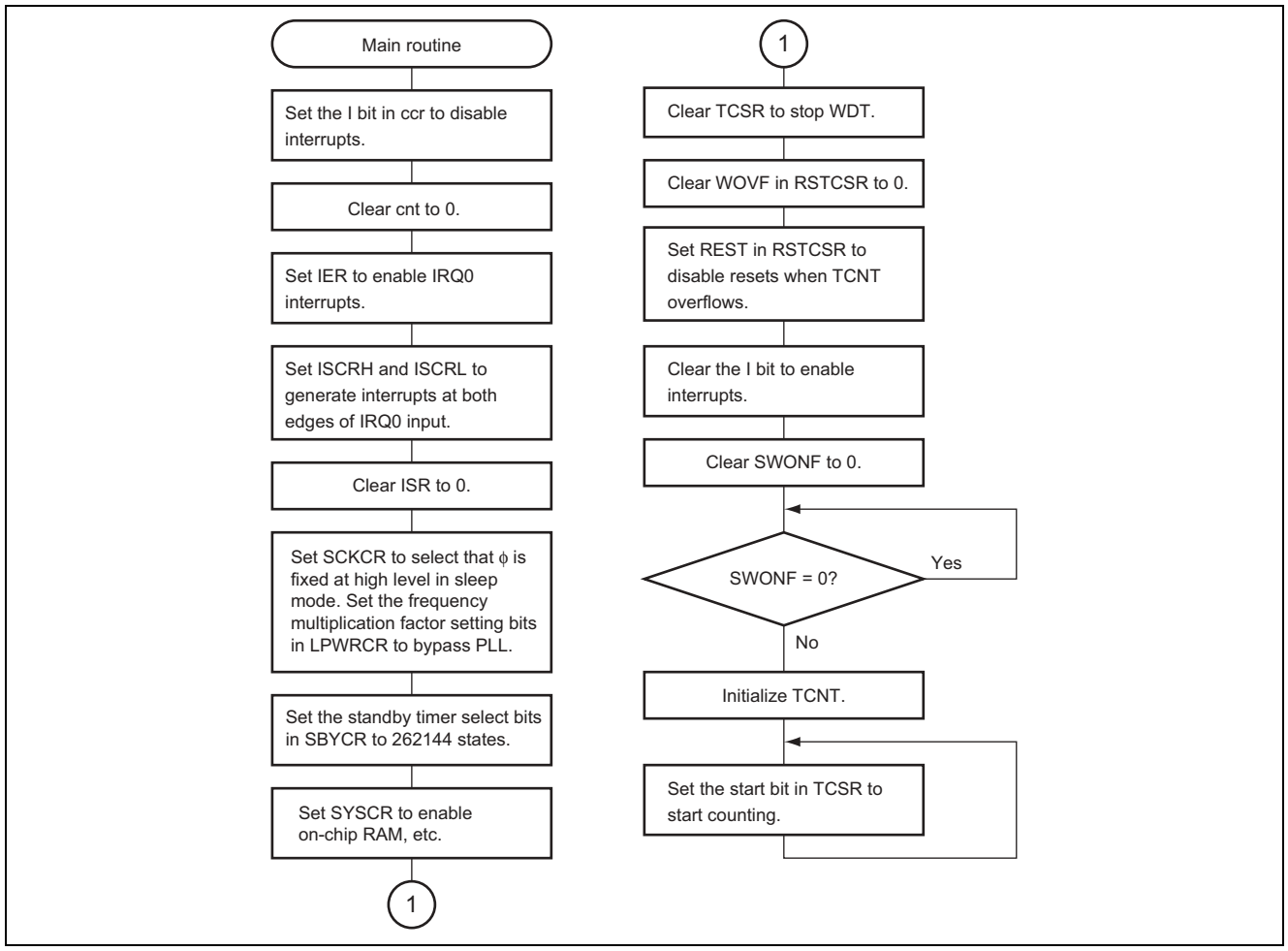
Table 4 describes the RAM usage in this sample task.

Table 4 Description of RAM

Label		Function	Address	Used in
cnt		8-bit counter for counting the number of interrupts	H'FFB000	Main routine, Count up
USRF	SWONF	Flag for determining whether the switch input is on or off	H'FFB001 Bit 0	Main routine, Switch on

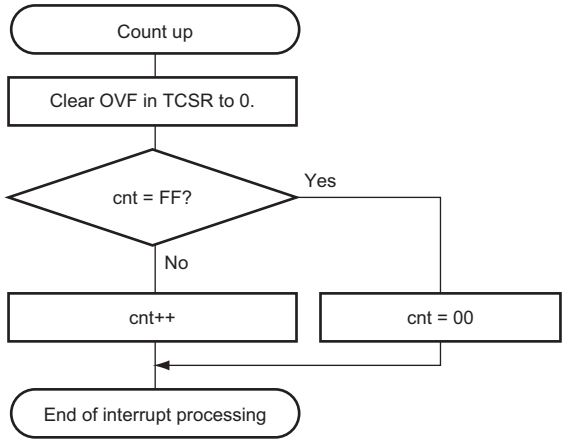
5. Flowchart

1. Main routine

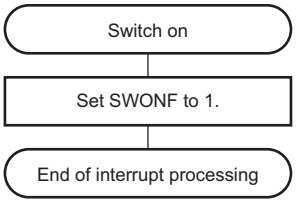


2. Interrupt routines

(a) Interval Timer Interrupt Processing Routine



(b) IRQ0 Interrupt Processing Routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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