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Renesas Electronics Corporation

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## H8S/2200 Series

### Simultaneous Startup of DTC, DMAC, and CPU

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#### Introduction

Starts up DTC, DMAC, and CPU each time a compare match occurs. DTC transfers data from the ROM to the I/O port and outputs pulses. The DMAC transfers data stored in RAM1 to RAM2. The CPU monitors the state of the port and stops DTC and DMAC when the port output goes low.

#### Target Device

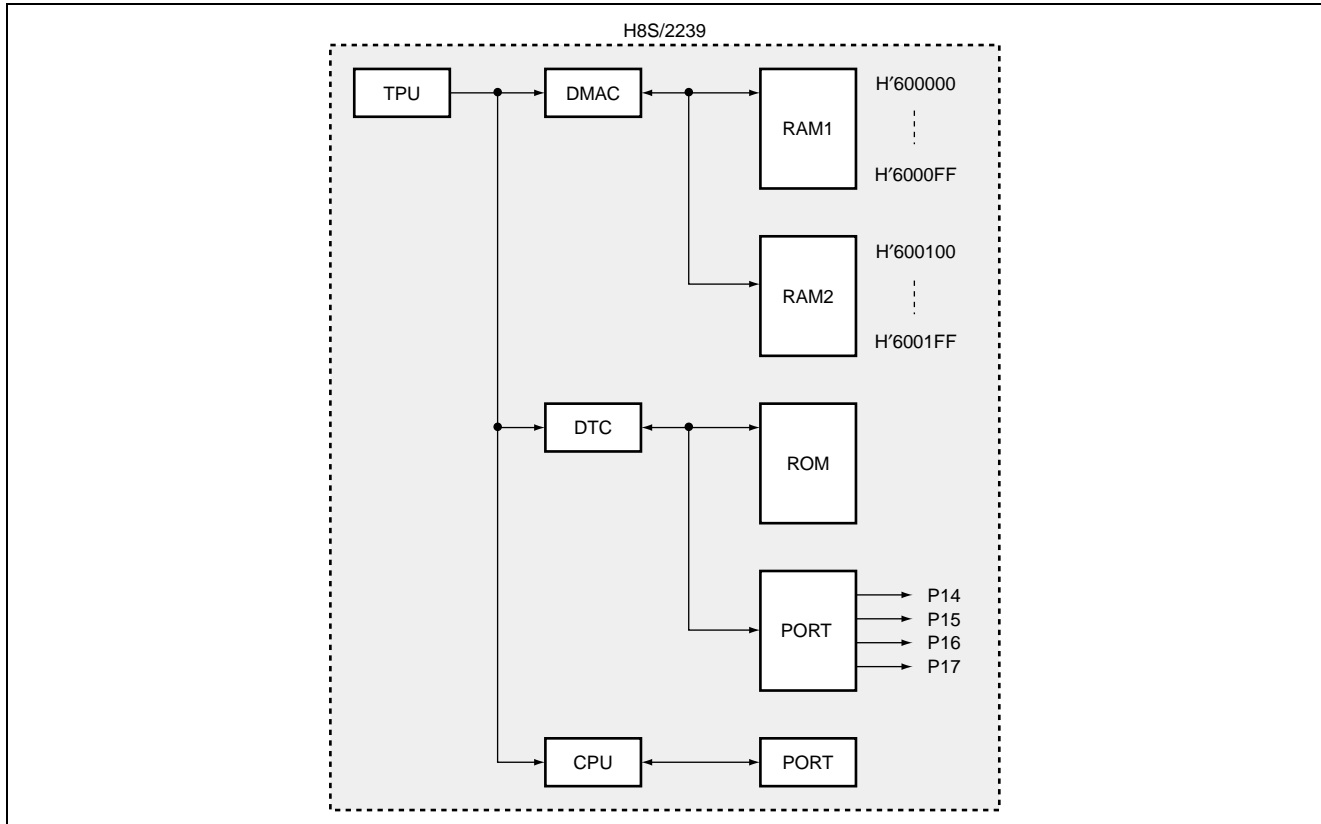
H8S/2239

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### 1. Specifications

1. As shown in figure 1, this sample task starts up DTC, DMAC, and CPU each time a timer compare match occurs. DTC transfers data to I/O Port from the data table (ROM) to output the pulses. The DMAC transfers 512-byte data stored in RAM1 to RAM2. The CPU monitors the state of the port. When the port goes low, the CPU stops DTC and DMAC transfer. An interrupt to the CPU continues to be enabled.
2. Data to be transferred by the DMAC is stored in addresses H'600000 to H'6001FF.
3. The H8S/2215 runs at 16-MHz internal operating frequency.



**Figure 1 Block Diagram of Simultaneous Startup of DTC, DMAC, and CPU**

### 2. Description of Functions

1. This sample task starts up the DMAC, DTC, and CPU each time a TPU compare match occurs.

A. The block diagram of H8S/2215 internal functions that this sample task uses is shown in figure 2.

This sample task uses the following functions to start up DTC, DMAC, and CPU simultaneously to transfer data and monitor the port.

[TPU]

Generates a compare match to generate a transfer request to DTC and DMAC and a CPU interrupt request.

[DMAC]

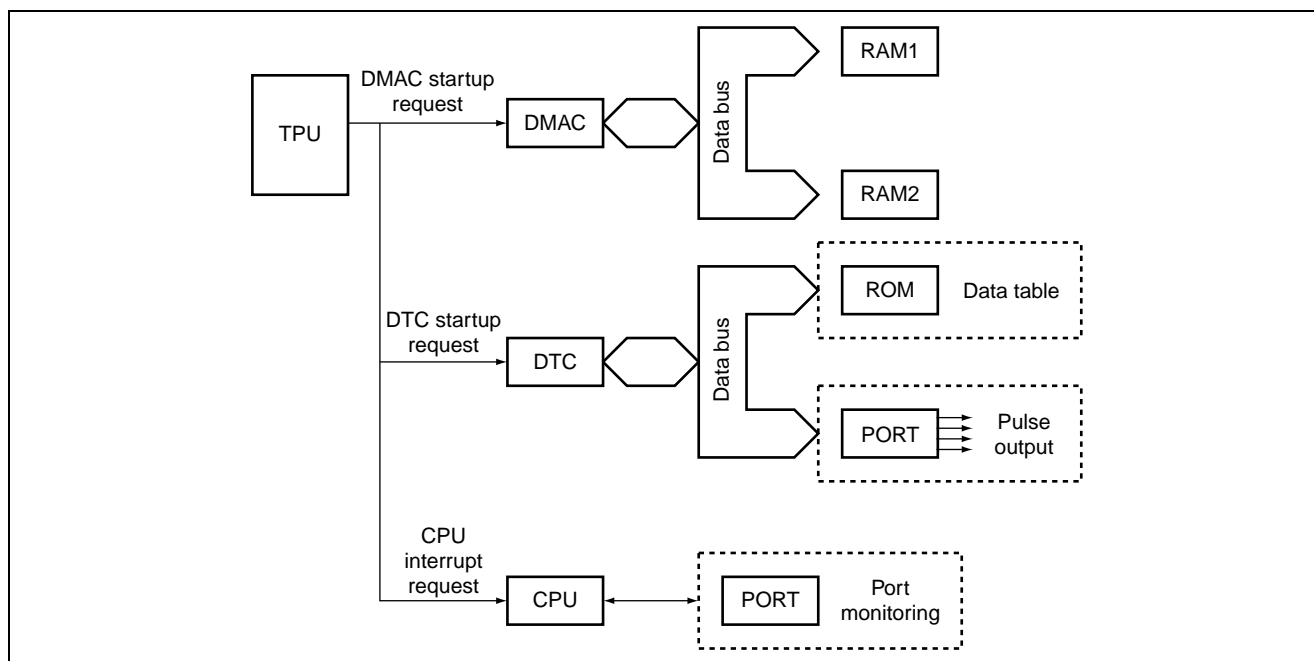
Starts up by a TPU compare match to transfer 512-byte data to RAM2 from RAM1.

[DTC], [PORT]

Start up by a TPU compare match to transfer 4-byte data to I/O Port from the data table.

[CPU]

Executes interrupt processing by a TPU compare match. During interrupt processing, monitors the port state and controls DMAC and DTC transfer.



**Figure 2 Block Diagram of Simultaneous Startup of DTC, DMAC, and CPU**

2. Function allocation of this sample task is shown in table 1. This sample task allocates H8S/2215 functions as shown in table 1 to transfer data.

**Table 1 Assignment of Functions**

<b>Elements</b>		<b>Description</b>
DMAC	DMABCR	Sets the DMAC0A as follows: <ul style="list-style-type: none"> <li>• Sets the full-address mode as the transfer mode.</li> <li>• Inhibits clear of internal interrupt source during DMA transfer.</li> <li>• Enables data transfer and a transfer end interrupt.</li> </ul>
	DMACR0A	Sets the DMAC0A as follows: <ul style="list-style-type: none"> <li>• Sets the data size to the byte size.</li> <li>• Sets MAR increment.</li> <li>• Sets data transfer in the block transfer mode.</li> <li>• Sets the data transfer direction (DMAC0A: MAR to OAR)</li> <li>• Sets the startup source to TPU0A.</li> </ul>
	MAR0A	Sets the start address of RAM1 (transfer source).
	MAR0B	Sets the start address of RAM2 (transfer destination).
	ETCR0A	Sets the transfer count.
TPU	TCR0	Clears the TCNT by a compare match.
	TIOR0	Inhibits compare match output.
	TIER0	Enables a compare match interrupt.
	TSR0	Sets the TGRA compare match interrupt request flag.
DTC	DTCER	Enables DTC startup by a TGIA interrupt.

### 3. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs hardware and software processing at the timing shown in figure 3 to request simultaneous startup of DTC, DMAC, and CPU interrupt.

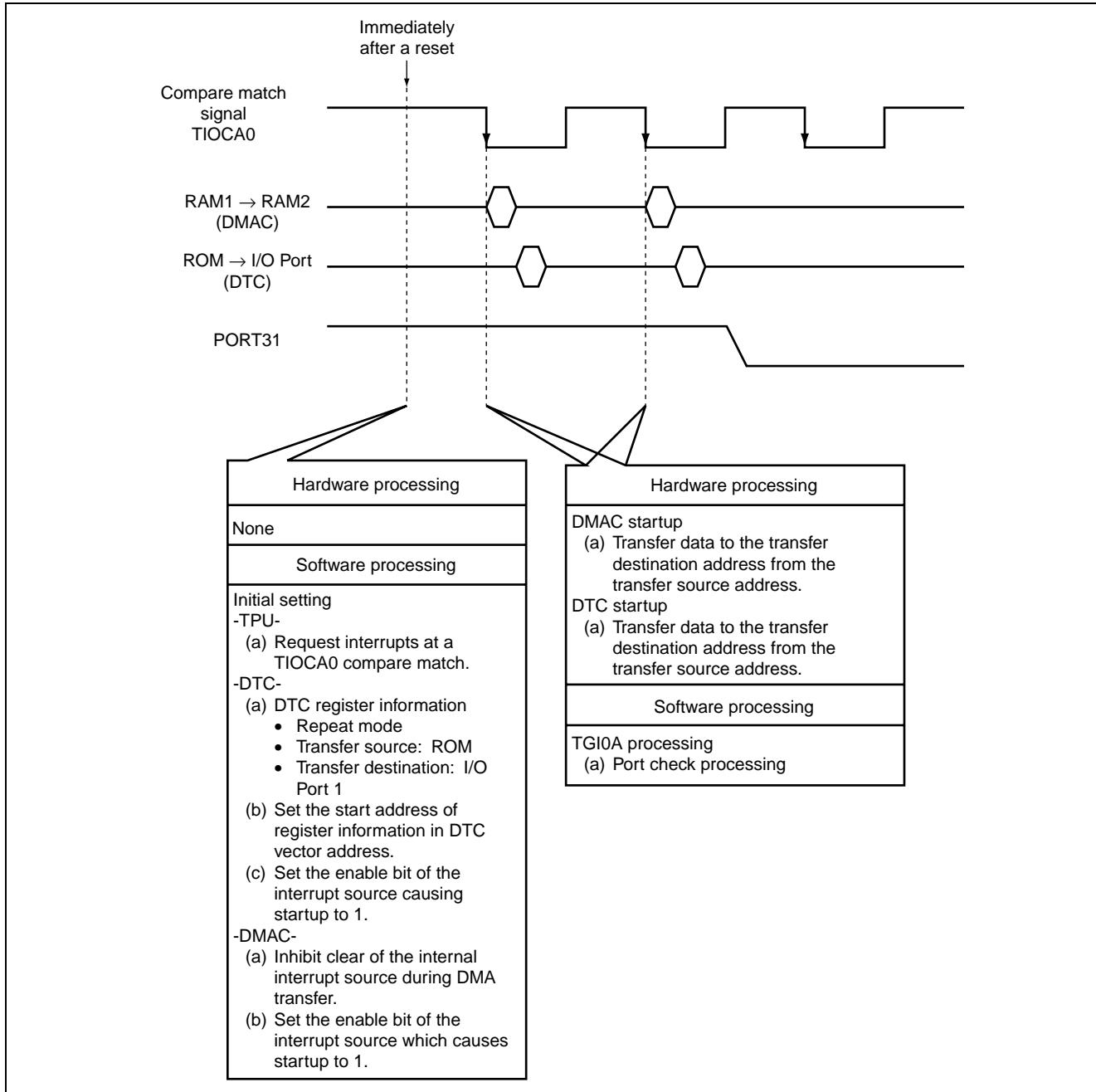


Figure 3 Principles of Operations Used of Simultaneous Startup of DTC, DMAC, and CPU

## 4. Description of Software

### 1. Description of Modules

Module Name	Label Name	Function
Main routine	simbsrnm	Performs initial setting of the TPU, DTC, DMAC, I/O Port and interrupt processing.
Port check	portchk	Checks the port and performs transfer inhibition processing.
Data transfer end	trsend	Sets the data transfer end flag.

### 2. Description of Arguments

Elements	Function	Data Length	Used in	I/O
status	Indicates the state of port 31. 0: Transfer enabled    1: Data transfer disabled	unsigned char	Port check	Output
trs_end	Flag indicating the end of 512-byte transfer 0: Transfer enabled    1: Data transfer disabled	unsigned char	Data transfer end	Output



### 3. Description of Internal Registers Used

Implemented Function	Register Name	Function
DMAC	DMABCR	Sets the DMAC0A as follows: <ul style="list-style-type: none"> <li>• Full-address mode as the transfer mode</li> <li>• Inhibiting clear of the internal interrupt source during DMA transfer</li> <li>• Enabling data transfer and a transfer end interrupt</li> </ul>
	DMACR0A	Sets the DMAC0A as follows: <ul style="list-style-type: none"> <li>• Byte size as the data size</li> <li>• MAR increment</li> <li>• Block transfer mode for data transfer</li> <li>• Data transfer direction (ch0A: MAR to IOAR)</li> <li>• Setting the startup source to TPU0A</li> </ul>
	MAR0A	Sets the start address (trs) of RAM1.
	MAR0B	Sets the start address (rev) of RAM2.
	ETCR0A, OB	Sets the transfer count.
	TPU	TCR0
TIOR0		Inhibits compare match output.
TIER0		Enables a compare match interrupt.
TSR0		Sets the TGRA capture interrupt request flag.
DTC		DTCER
MSTPCR		Controls module stop mode of DTC, TPU and DMAC.

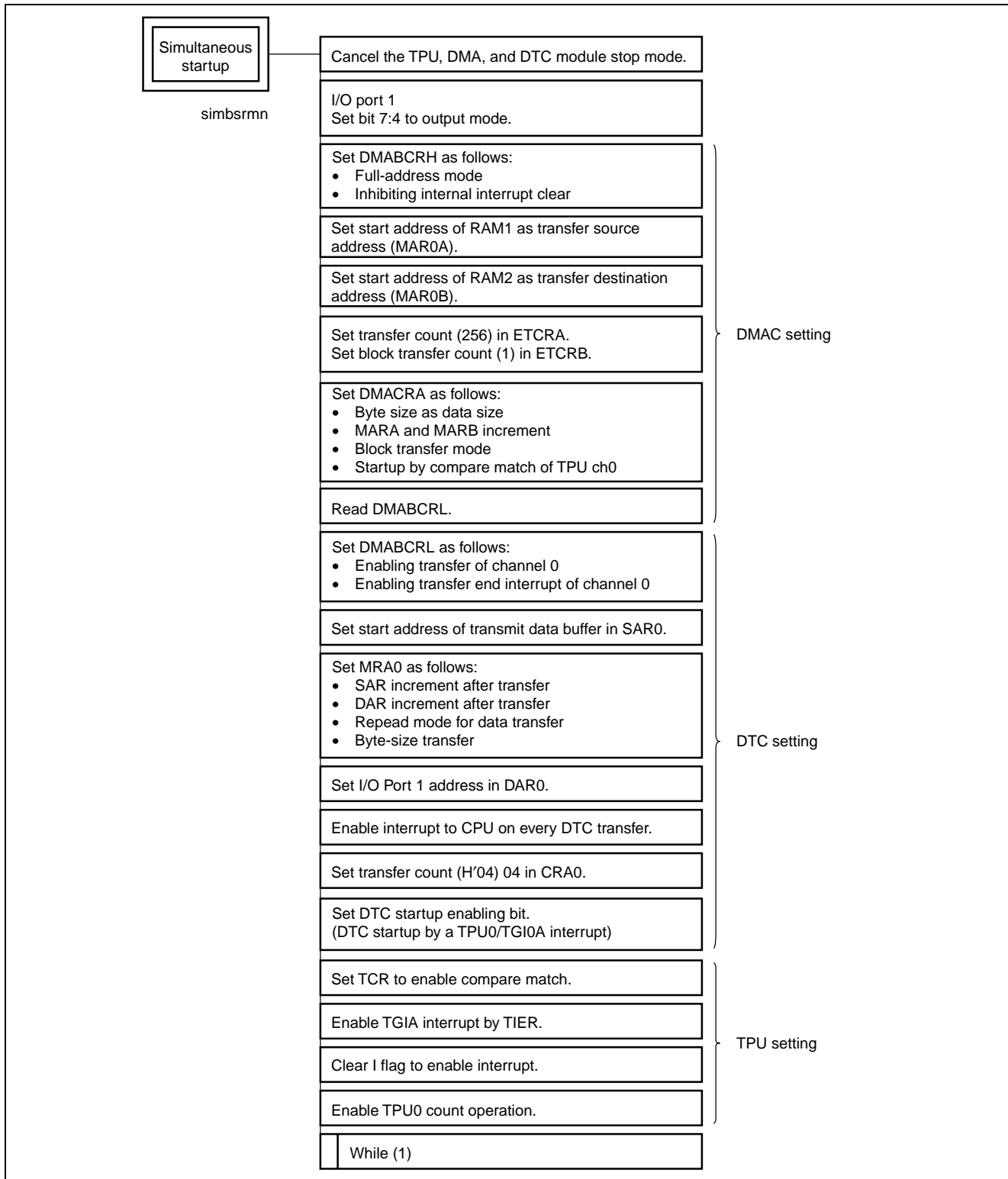
### 4. RAM Usage

Table below describes RAM usage in this sample task.

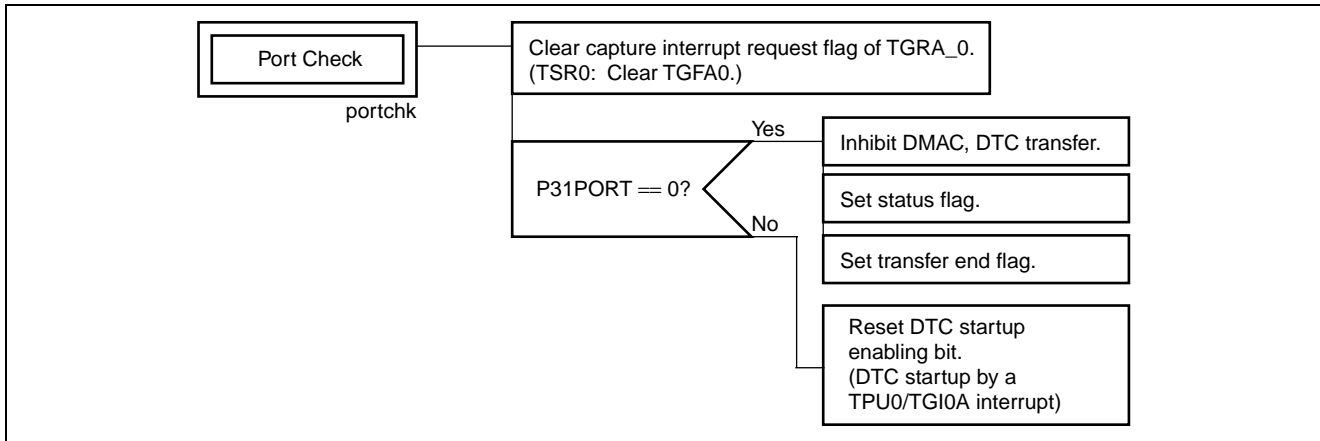
Elements	Function	Data Length	Used in
MAR0	Sets the DTC0 in the repeat mode.	unsigned char	Main routine
MRB0	Enables an interrupt to the CPU.	unsigned char	
SAR0	Sets the transfer source address (PATTBL1).	unsigned long	
DAR0	Sets the transfer destination address (P1DR).	unsigned long	
CRA0	Sets the transfer count.	unsigned short	
trs	Stores transmit data.	256 bytes	
rev	Stores received data.	256 bytes	
PATTBL1	Stores pulse output data.	4 bytes	

### 5. PAD

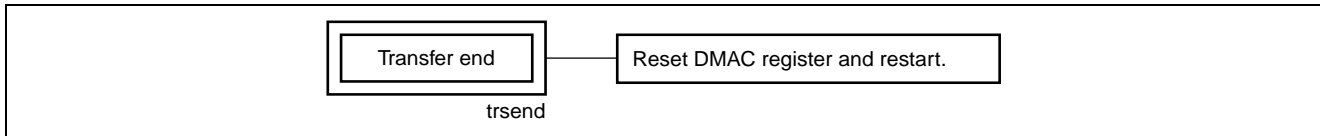
#### 1. Main Routine



### 2. Port Check



### 3. Data Transfer End



### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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