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H8S Family

Serial Communications Interface (Smart Card) Control

Introduction

The H8S/2339 serial communication interface supports the smart card (IC card) interface based on the ISO/IEC 7816-3 (Identification Card) as an extension function. This interface allows data communication between the H8S/2339 and a smart card. H8S/2377R is used instead of a smart card in this application note.

Target Device

H8S/2339

Contents

1. Overview

The H8S/2339 serial communication interface supports the smart card (IC card) interface based on the ISO/IEC 7816-3 (Identification Card) as an extension function. This interface allows data communication between the H8S/2339 and a smart card. H8S/2377R is used instead of a smart card in this application note.

2. Configuration

Table 1 shows the configuration of this sample task. Table 2 shows the smart card interface specifications.

The internal operation of a smart card includes manufacturer's confidential information that cannot be described in this application note. Accordingly, H8S/2377R is used instead of a smart card in this application note.

Table 1 Configuration of this Sample Task

Part	Specification
H8S/2339 CPU board Product code: HSB8S2339EF (Manufactured by Hokuto Denshi Co., Ltd.)	Board power supply input: 3.3 V DC Operating frequency: 19.6608 MHz MCU operating mode: 7
H8S/2377 CPU board Product code: HSB8S2377F (Manufactured by Hokuto Denshi Co., Ltd.)	Board power supply input: 3.3 V DC Operating frequency: 19.6608 MHz MCU operating mode: 7

Table 2 Interface Specifications

Item	Specification
Microcomputer port used	SCI_2
Transfer rate	38400 bps
Data type	Direct convention type (even parity)
Block transfer mode	Not used
GSM mode (clock output)	Not used

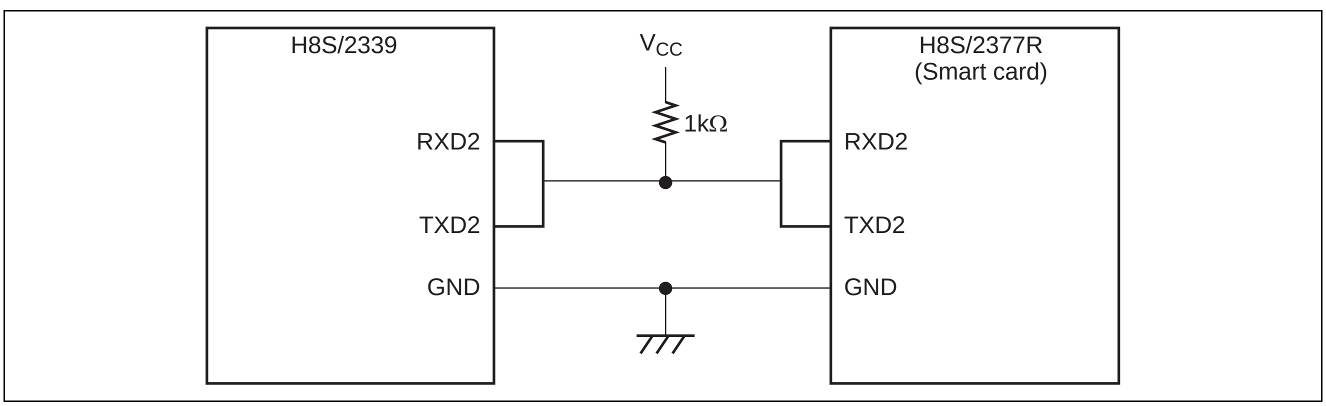


Figure 1 Connections between H8S/2339 and H8S/2377R (Smart Card)

3. Description of Functions

After the H8S/2339 transmits the contents (1 byte) of send_data in the on-chip RAM, the H8S/2339 enters receive mode. The receiver (H8S/2377R) returns response data (0x67: fixed value) after it has received the data.

The H8S/2339 receives the response data and stores it in read_data of on-chip RAM.

In this case, data transmission and reception status is set in the following flags.

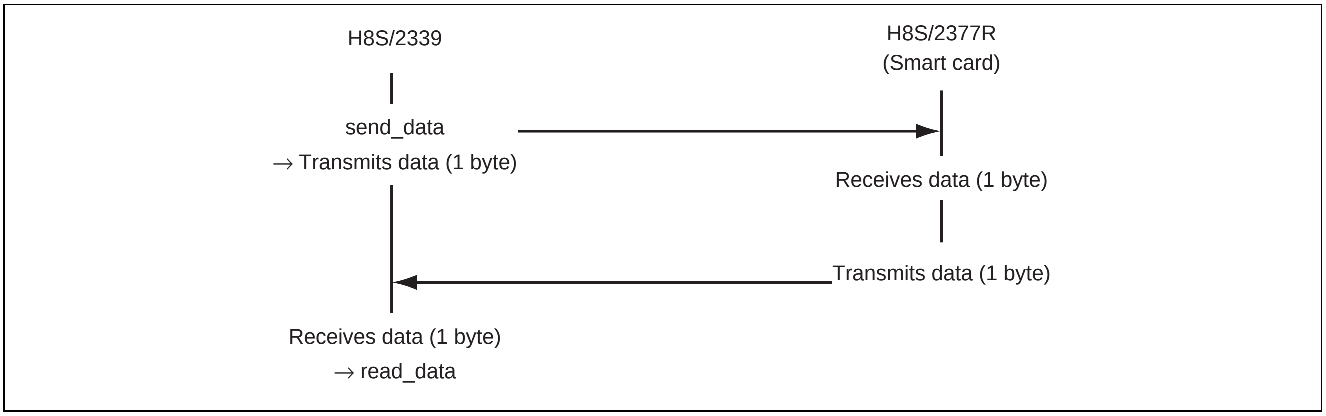


Figure 2 Data transmission and reception status

On-Chip RAM Area Name	Data Size	Function
send_data	unsigned char	Sets transmit data
read_data	unsigned char	Stores receive data
rxi_flg	unsigned char	1: Normal data reception
eri_flg	unsigned char	1: Receive error
status_code	unsigned char	Indicates data transmission and reception status.

Bit	Description
7	1: Data transmission end
6	1: An error signal for transmit data is sent from receiver*[1].
5, 4	Reserved
3	1: Normal data reception
2	1: An overrun error is detected during data reception.
1	1: A parity error is detected during data reception*[2].
0	Reserved

Notes: 1. The transmitter that receives an error signal re-transmits the same data automatically.
2. When a parity error is received, an error signal is returned.

4. Description of Operation

4.1 Basic Operation

The smart card interface performs data transmission and reception in asynchronous mode with parity and re-transmits data automatically by hardware when a parity error has occurred.

The smart card interface has the following functions

1. One frame consists of 8-bit data and a parity bit.
2. During transmission, a guard timer of 2 etu (1 etu during block transfer mode) (etu: elementary time unit <one bit transfer period>) or more is necessary from the parity bit transmission to the next frame start.
3. When the receiver detects a parity error, the receiver outputs a low level of an error signal for 1 etu period after 10.5 etu or more has passed from the start of bit transmission (other than block transfer mode).
4. When the transmitter samples an error signal, the transmitter re-transmits the same data automatically after 2 etu or more has passed (other than block transfer mode).
5. The smart card interface only supports the asynchronous communication function and does not support clock synchronous communication function.

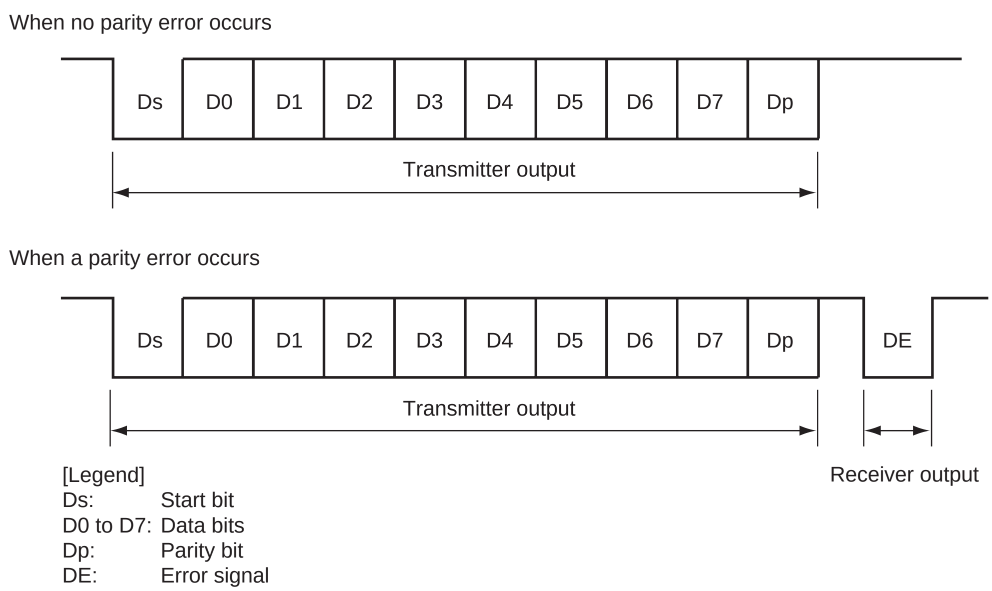


Figure 3 Data Format of Normal Smart Card Interface

4.2 Initialization Processing

When data transmission or reception is performed by the smart card interface initially or when transmission or reception operation is switched, the following initialization processing is performed. During initialization processing, subroutine **smartcard_if_init (void)** is called.

4.2.1 Initial Values

reg name	bit	name	value	Description	Reference Section
MSTPCR	7	_SCI2	0	Operates SCI_2	—
SCR	5	TE	0	Disables transmission	—
SCR	4	RE	0	Disables reception	—
SSR	7:0	—	0x00	Reads and reset the status register	—
SMR	7	GM	0	Does not use GSM mode	4.2.2
	6	BLK	0	Does not use block transfer mode	4.2.3
	5	PE	1	Enables a parity	4.2.4
	4	O/E	0	Uses an even parity	
	3:2	BCP[1:0]	00	Sets the number of basic clocks in a bit period as 32 clocks	4.2.5
	1:0	CKS[1:0]	00	Sets the clock source of internal baud rate generator as ϕ/clock	
SCMR	7:4	—	0000	Reserved	—
	3	SDIR	0	Sets LSB first	4.2.4
	2	SINV	0	Does not invert data	
	1	—	0	Reserved	—
	0	SMIF	1	Sets smart card interface mode	—
BRR	7:0	—	7	Sets transfer rate as 38400 bps (operating frequency: 19.6608 MHz)	4.2.5
SCR	1:0	CKE[1:0]	00	Disables SCK clock output	4.2.2

Note: After setting the above initial values, wait for at least 1-bit time.

4.2.2 GSM Mode

When the GM mode of SMR is set to 1, the SCK clock specified by the CKE[1:0] bits in the SCR can be output.

If CKE in the SCR = 0, a low level is output. If CKE in the SCR = 1 or 3, a clock is output. If CKE in the SCR = 2, a high level is output.

The clock output period with a duty cycle of 50% is obtained by:

Transfer rate $\times$ the number of clocks specified by SMR (BCP)

In this sample task, the transfer rate is 38400 bps and the number of clocks specified by SMR (BCP) = 0 is 32. Accordingly, the clock period is calculated as follows:

38400 bps $\times$ 32 = 1.23 Mbps $\rightarrow$ 813 ns.

In this sample task, GSM mode is not used.

4.2.3 Block Transfer Mode

When the BLK mode in the SMR is set to 1, the block transfer mode is selected. The block transfer mode differs from normal smart card interface in the following points.

- Though a parity check is performed during reception, no error signal is output even if an error is detected. When an error is detected during the parity check, the PER bit in SSR is set to 1 and the PER bit must be cleared before the parity bit of the next frame is received.
- During transmission, the guard time from the end of the parity bit to the start of the next frame is 1 etu or more. Because re-transmission of the same data is not performed during transmission, the TEND flag is set 11.5 etu after the start of transmission.
- Though the ERS flag indicates the error signal status in the same way as the normal smart card interface, the ERS flag is always cleared to 0 because the error signal transmission and reception are not performed.

In this sample task, block transfer mode is not used.

4.2.4 Data Type Selection

The smart card interface supports direct convention and inverse convention types according to the smart card to be connected.

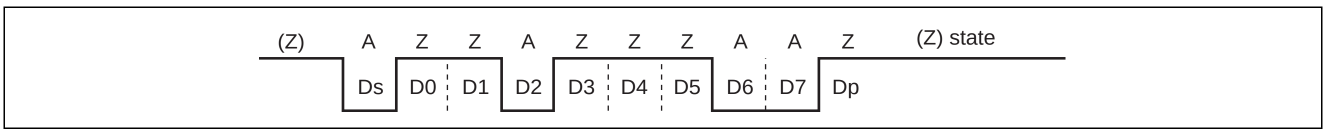


Figure 4 Direct Convention (SDIR = SINV = $O/\overline{E}$=0)

In the direct convention type, as shown in the start character above, logic levels 1 and 0 correspond to states Z and A, respectively, and data is received or transmitted in LSB first. In the above start character, data is H'3B. In the direct convention type, both the SDIR and SINV bits in SCMR must be cleared to 0. In addition, to satisfy the smart card standard, the $O/\overline{E}$ bits in SMR must be cleared to 0 to select an even parity.

In this sample task, the direct convention type is used.

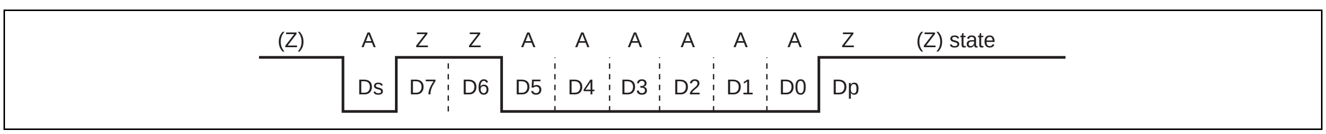


Figure 5 Inverse Convention (SDIR = SINV = $O/\overline{E}$=1)

In the inverse convention type, as shown in the start character above, logic levels 1 and 0 correspond to states A and Z, respectively, and data is received or transmitted in MSB first. In the above start character, data is H'3F. In the inverse convention type, both the SDIR and SINV bits in SCMR must be set to 1. According to the smart card standard, logic level 0 corresponds to state Z in even parity. In this LSI, the SINV bit inverts only data bits D7 to D0. Accordingly, the $O/\overline{E}$ bit in SMR must be set to 1 to inverse a parity bit during transmission and reception.

4.2.5 Transfer Rate Setting

Only the internal clock generated by the internal baud rate generator can be used as a transmission or reception clock for the smart card interface. In this case, the BRR register is set by transfer rate (bps) and the CKS [1:0] and BCP [1:0] bits in SMR using the following formula.

$$N = \frac{\phi}{S \times 2^{2n+1} \times B} \times 10^6 - 1$$

N= BRR setting value ($0 \leq N \leq 255$)
B = transfer rate (bps)
ϕ = operating frequency (MHz)
n = Refer to the following table.
S = Number of internal clocks in one-bit period specified by BCP1 and BCP0

Table 3 Correspondence among n, CKS1, and CKS0

n	CKS1	CKS0
0	0	0
1		1
2	1	0
3		1

The deviation is calculated using the following formula. A transfer rate with a deviation as small as possible must be selected.

$$\text{Deviation (\%)} = \left(\frac{\phi}{S \times 2^{2n+1} \times B \times (N+1)} \times 10^6 - 1\right) \times 100$$

In this sample task, since B = 38400 bps, ϕ = operating frequency = 19.6608 MHz, n = 0 and S = 32, N = BRR setting value = 7 and deviation (%) = 0.

4.3 Data Transmission

After the initialization processing described in section 4.2 is performed before data transmission, 1-byte data is transmitted by subroutine **smartcard_send_data**.

The subroutine specification is shown below.

- **void** smartcard_send_data (**unsigned char*** p)
  Transmits 1-byte data.

Argument		
Type	**Name**	**Description**
Unsigned char*	p	Write data address

4.4 Data Reception

After the initialization processing described in section 4.2 is performed and before data reception, the RE and RIE bits in the SCR register are set to 1 to wait for a receive interrupt. In the receive interrupt wait state, 1-byte data is read by subroutine **smartcard_receive_data**.

The subroutine specification is shown below.

- **Unsigned char** smartcard_receive_data (**unsigned char*** p)
  Receives 1-byte data.

Argument		
Type	**Name**	**Description**
Unsigned char*	p	Address to store read data

Return Value Type: unsigned char	Description
0	Normal completion
Other than 0	Abnormal completion Bit 5 = 1: Overrun error Bit 3 = 1: Parity error

5. Description of Sample Program

5.1 File Configuration

The sample program is provided as a project of the HEW (High-performance Embedded Workshop)*.

By executing **H8S_2339_1.hws**, the **HEW** startup source program can be referenced or updated. If the user has no **HEW**, please refer to the following source files directly using editors.

File Name	Specification
resetprg.c	Executed from reset vector address 0 if the MCU is reset.
intprg.c	Executed if an interrupt other than a reset occurs.
dbsct.c	Sets start and end addresses of the section used by _INITSCT function in resetprg.c to section initialization table. For details, refer to the H8S, H8/300H Series C/C++ Compiler, Assembler, and Optimization Linkage Editor User's Manual.
H8S_2339_1.c	Main routine and interrupt routine of this sample task.
iodefine.h	Configuration definition file of internal registers.
stacksct.h	Defines stack size.

Note: * http://documentation.renesas.com/eng/products/tool/rej10b0058_h8scompiler.pdf

5.2 Linkage

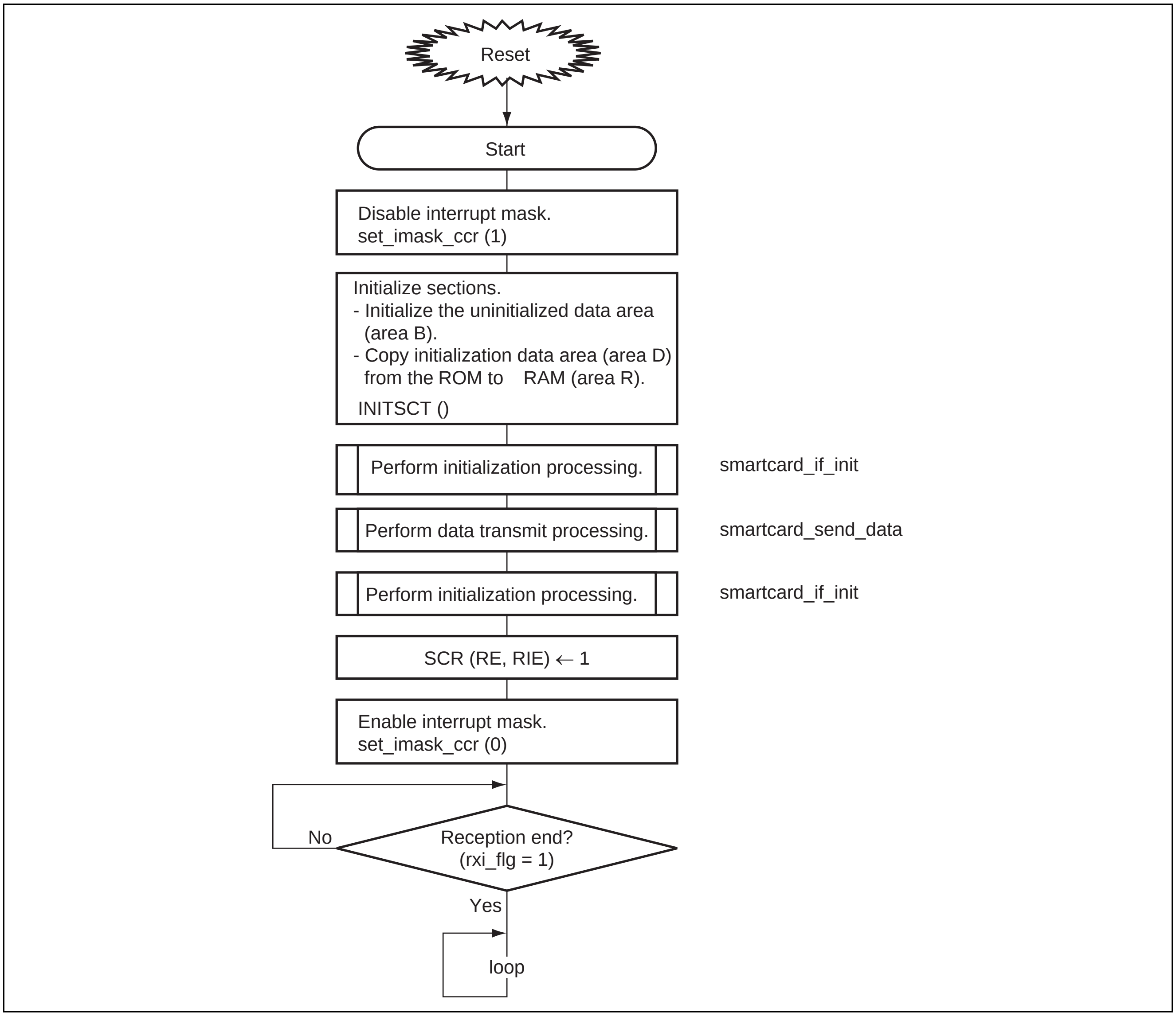
The linkage addresses of each section are as follows.

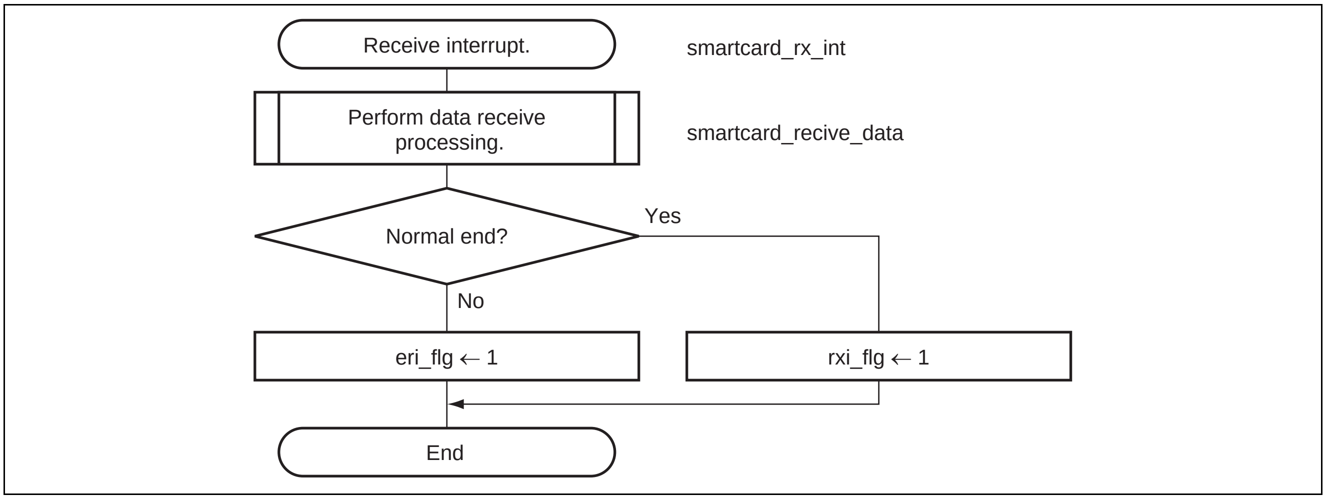
In the HEW project files, the linkage addresses can be referenced and set by Category: section of Link/librarq tab in option – Standard Toolchain.

Section	Start Address
PResetPRG	0x000400
PIntPRG	
P	0x000800
C$DSEC	
C$BSEC	
D	
B	0xFFDC00
R	
S	0xFFF9F0

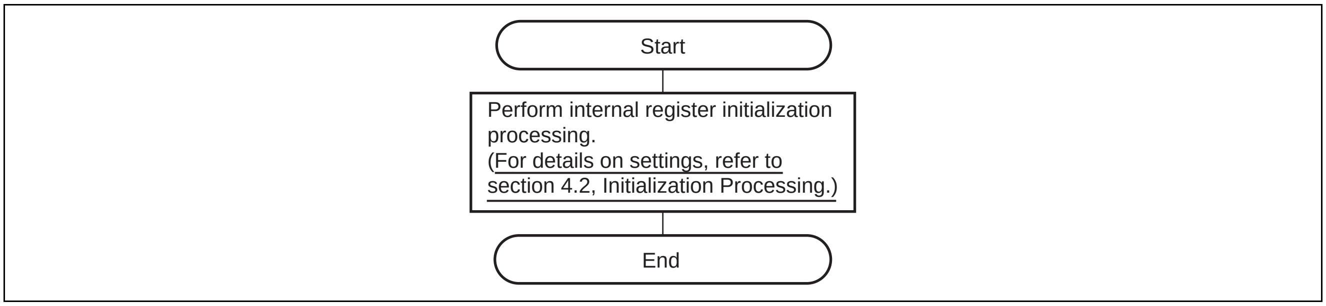
6. Flowchart

6.1 Whole Flow

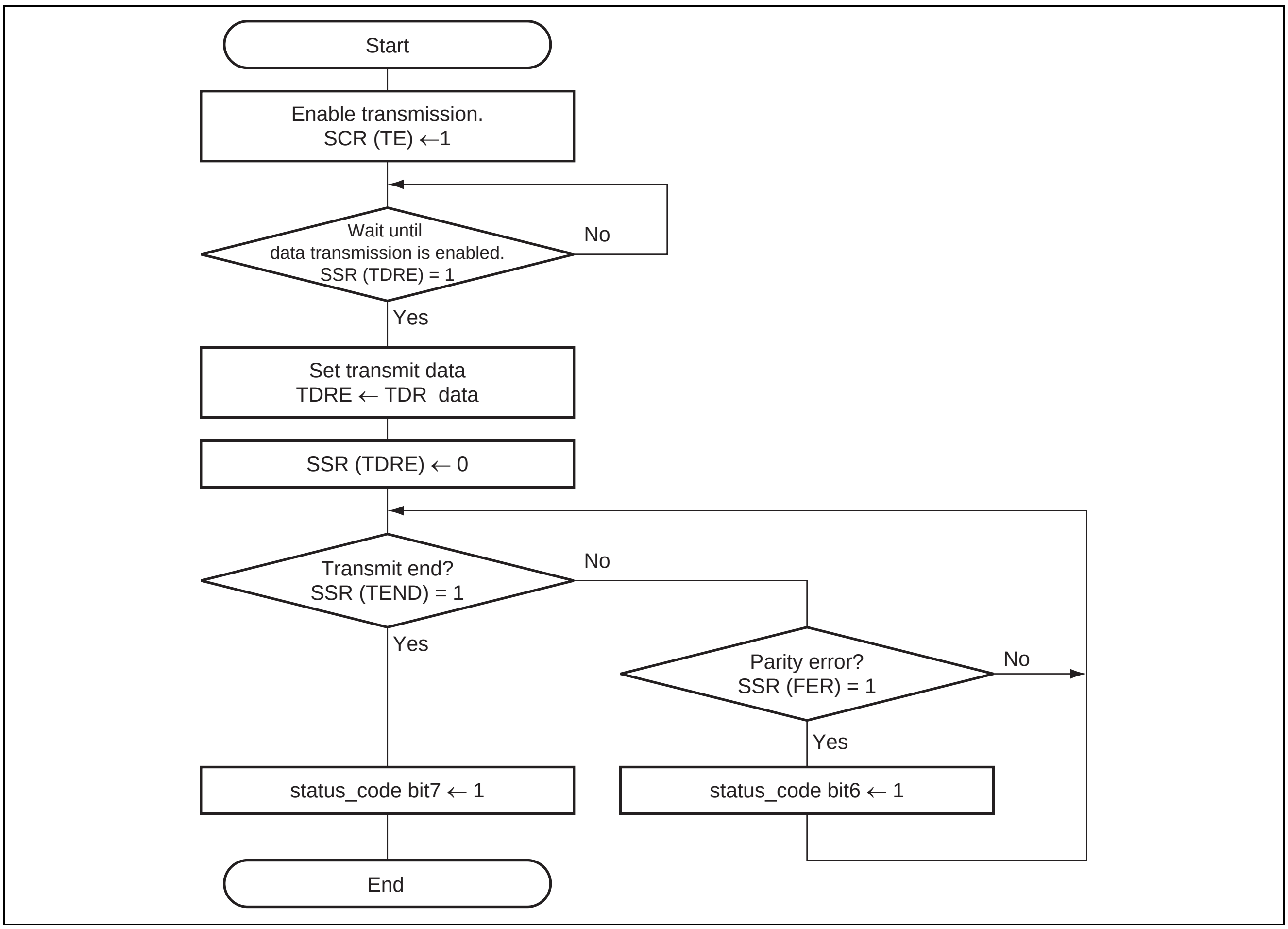



Receive interrupt.
smartcard_rx_int
Perform data receive processing.
smartcard_recive_data
Normal end?
Yes
No
eri_flg ← 1
rxi_flg ← 1
End

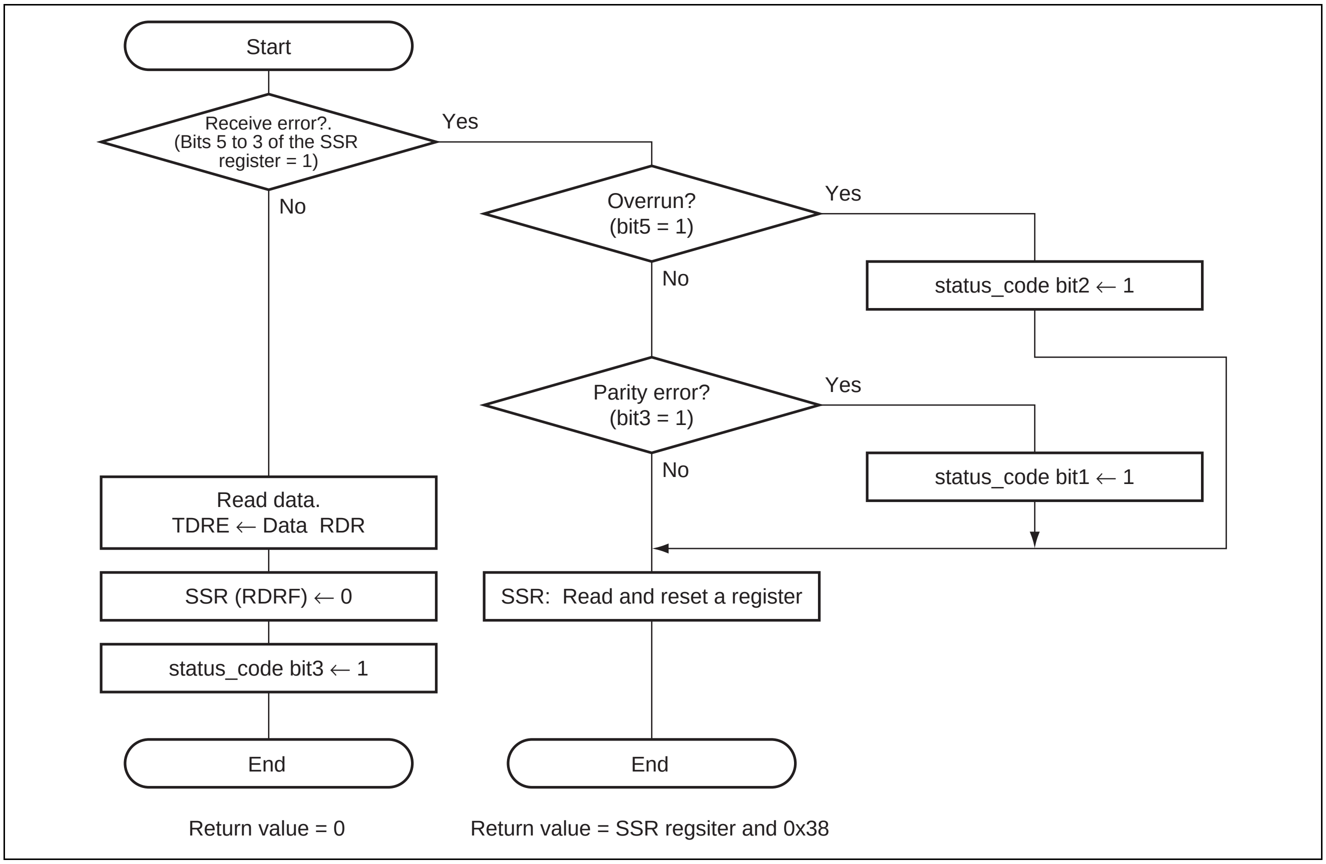
- smartcard_if_init
  Smart Card Interface Initialization



- smartcard_send_data (unsigned char* p)
  1-byte data transmission



- smartcard_receive_data (unsigned char* p)
  1-byte data reception



References

Document Name	How to Get the Document
H8S/2339 Series, H8S/2338 Series, H8S/2329 Series, H8S/2328 Series, H8S/2319 Series, and H8S/2318 Series Hardware Manual	Download from the website of Renesas Technology Corp.

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Rev.	Date	Description	
		Page	Summary
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