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H8/38602R Group

Subclock Operation Using the On-Chip Oscillator

Introduction

This application note discusses the subclock operation using the on-chip oscillator of the H8/38602R. After a reset, the on-chip oscillator is selected as the subclock source, after which a direct transition is made to subactive mode. In addition, ϕw is output from the TMOW pin by means of the clock output function of the Realtime Clock (RTC).

Target Device

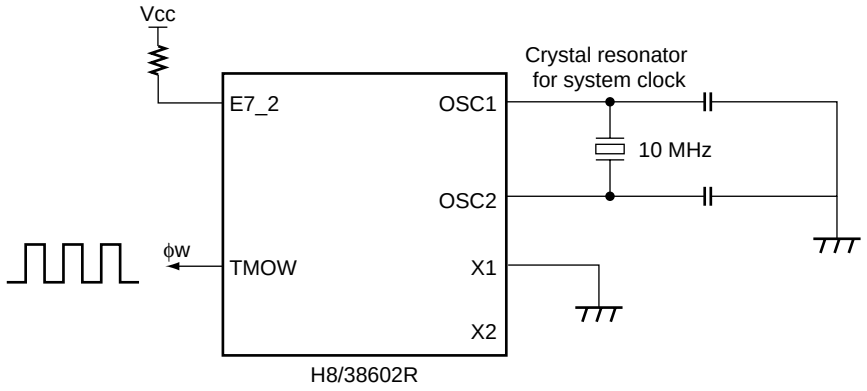
H8/38602R

Contents

1. Specifications

The subclock operation is performed using the on-chip oscillator of the H8/38602R. After a reset, the on-chip oscillator is selected as the subclock source, after which a direct transition is made to subactive mode, and ϕw is output from the TMOW pin by means of the RTC's clock output function. The system clock is generated by the system clock oscillator for which a 10-MHz crystal resonator is used.

Figure 1 shows a block diagram of the subclock operation using the on-chip oscillator.



System clock is generated by the system clock oscillator circuit, for which a 10-MHz crystal resonator is used.
Subclock is generated using the on-chip oscillator.

Figure 1 Subclock Operation Using On-chip Oscillator

2. Description of Functions

2.1 Functions

In this sample task, the subclock operation is carried out using the on-chip oscillator. After a reset, the on-chip oscillator is selected as the subclock source, after which a direct transition is made to subactive mode, and ϕw is output from the TMOW pin by means of the RTC's clock output function. The following describes the functions used in this sample task.

2.1.1 Clock Pulse Generator Function

The clock pulse generator includes both a system clock pulse generator and a subclock pulse generator. The system clock pulse generator consists of a system clock oscillator, system clock divider, and on-chip oscillator. The subclock pulse generator consists of a subclock oscillator, on-chip oscillator clock divider, and subclock divider.

A subclock can be provided in three ways: by connecting a crystal resonator, inputting an external clock, or selecting the on-chip oscillator. To select the on-chip oscillator as the subclock source, the SUBSEL bit in the Oscillator Control Register (OSCCR) should be set to 1.

Figure 2 shows a block diagram of the clock pulse generators.

- Oscillator Control Register (OSCCR)
  OSCCR controls the subclock oscillator, built-in feedback resistance, and on-chip oscillator.

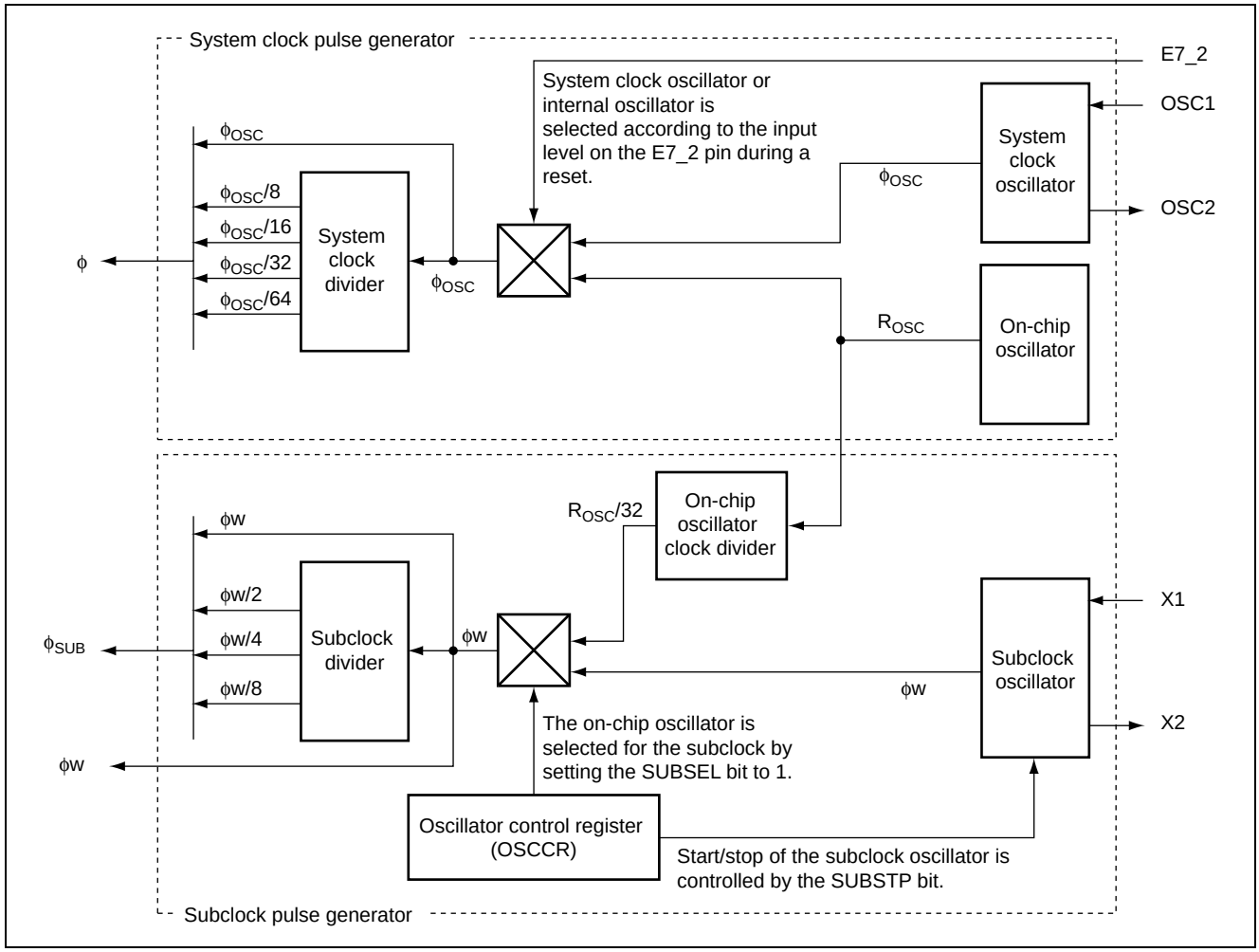


Figure 2 Block Diagram of Clock Pulse Generators

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer, which is active after a reset. The timer counter WD (TCWD) counts up, and the H8/38602R is internally reset if the TCWD overflows. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. The setting value cannot be changed by bit manipulation instructions.

2.1.3 Power-Down Mode (Subactive Mode) Function

In subactive mode, the system clock oscillator stops but on-chip peripheral modules except for the IIC2 operate. As long as a required voltage is applied, the contents of registers of certain on-chip peripheral modules are retained.

Subactive mode is exited by executing a SLEEP instruction. When subactive mode is exited, a transition to subsleep mode, active mode, or watch mode is made, according to the combination of bits SSBY, LSON, and TMA3 in SYSCR1 and bits MSON and DTON in SYSCR2. Subactive mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable register.

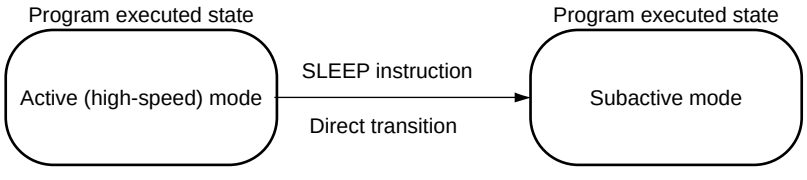
The operating frequency of subactive mode is selected from ϕw (watch clock), ϕw/2, ϕw/4, and ϕw/8 by the SA1 and SA0 bits in SYSCR2. After a SLEEP instruction is executed, the operating frequency returns to the frequency that was set before the execution.

In this sample task, a direct transition is made from active (high-speed) mode to subactive mode. There are two modes in which the CPU executes programs: active and subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition can be made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition is also helpful in changing the operating frequency between active mode and subactive mode. After the mode transition, direct transition interrupt exception handling starts. It must be noted that if a direct transition is attempted while the I bit in CCR is set to 1, sleep or watch mode will be entered but the resulting mode cannot be exited by means of an interrupt.

When a SLEEP instruction is executed in active (high-speed) mode while the SSBY, TMA3, and LSON bits in SYSCR1 are set to 1 and the DTON bit in SYSCR2 is set to 1, a transition is made to subactive mode via watch mode.

Figure 3 shows a block diagram of a direct transition from active (high-speed) mode to subactive mode.

- System Control Register 1 (SYSCR1)
  SYSCR1 controls the power-down modes, in combination with SYSCR2.
- System Control Register 2 (SYSCR2)
  SYSCR2 controls the power-down modes, in combination with SYSCR1.



Mode transition conditions

LSON	MSON	SSBY	TMA3	DTON
1	X	1	1	1

[Legend] X: Don't care

Figure 3 Direct Transition from Active (High-Speed) Mode to Subactive Mode

2.1.4 RTC Clock Output Function

In this sample task, ϕw is output from the TMOW pin by means of the RTC's clock output function. By clearing the CLKOUT bit to 0 and setting the TMOW bit to 1 in the port mode register 1 (PMR1), the function of the P10/AEVH/FTIOA/TMOW/CLKOUT pin is set to TMOW. ϕw is output from the TMOW pin by setting the SUB32K bit in the clock source select register (RTCCSR) to 1.

- Port Mode Register 1 (PMR1)
  PMR1 controls the selection of functions for port 1 pins.
- Clock Source Select Register (RTCCSR)
  RTCCSR selects the clock source.

2.2 Function Assignment

Table 1 shows the assignment of functions used in this sample task. Subclock operation using the on-chip oscillator is carried out by assigning the functions as shown in table 1.

Table 1 Functions Assignment

Function	Description
OSCCR	Controls start/stop of the subclock oscillator and selects the oscillator used for operation of the subclock pulse generator.
TCSRWD1	Stops the watchdog timer.
SYSCR1	Controls direct transition to subactive mode, in combination with SYSCR2.
SYSCR2	Controls direct transition to subactive mode, in combination with SYSCR1.
PMR1	Sets so that the P10/AEVH/FTIOA/TMOW/CLKOUT pin functions as the TMOW pin.
RTCCSR	Selects ϕw as the clock output from the TMOW pin.

3. Description of Operation

In this sample task, the subclock operation is carried out using the on-chip oscillator. After a reset, the on-chip oscillator is selected as the subclock source, after which a direct transition is made to subactive mode, and ϕw is output from the TMOW pin by means of the RTC's clock output function. Figure 4 illustrates the subclock operation using the on-chip oscillator.

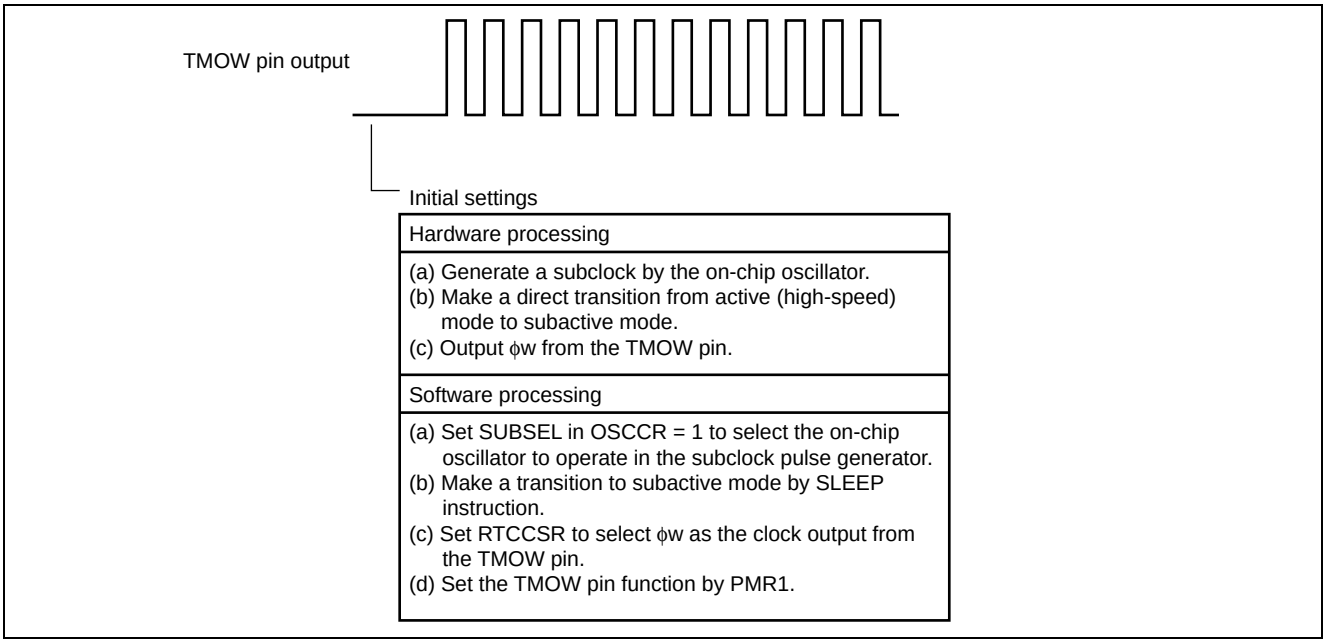


Figure 4 Subclock Operation by On-chip Oscillator

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Function Name	Description
main	Stops the watchdog timer, selects a subclock oscillator, controls interrupts, makes a transition to subactive mode, initializes the RTC and sets the TMOW pin function.
int_sleep	Direct transition interrupt processing

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers

The following describes internal registers used in this sample task.

- Oscillator Control Register (OSCCR) Address H'FFF5

Bit	Bit Name	Setting	R/W	Function
7	SUBSTP	1	R/W	Subclock Oscillator Control Controls start/stop of the subclock oscillator. This bit should be set to 1 when the subclock is not used. 0: Subclock oscillator operates. 1: Subclock oscillator stops.
5	SUBSEL	0	R/W	Subclock Select Selects the oscillator used for operation of the subclock pulse generator. 0: Subclock oscillator is used. 1: On-chip oscillator is used. Note: The SUBSEL bit setting can be changed only when the subclock is not being used.

- Timer Control/Status Register WD1 (TCSRWD1) Address H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

- System Control Register 1 (SYSCR1) Address H'FFF0

Bit	Bit Name	Setting	R/W	Function
7	SSBY	1	R/W	Software Standby Selects the mode to which the transition is made after a SLEEP instruction is executed. 0: Transition is made to sleep mode or subsleep mode. 1: Transition is made to standby mode or watch mode.
3	LSON	1	R/W	Low Speed ON Flag Selects the system clock (ϕ) or subclock (ϕSUB) as the operating clock of the CPU when watch mode is exited. 0: The CPU operates on the system clock (ϕ) 1: The CPU operates on the subclock (ϕSUB)
2	TMA3	1	R/W	In combination with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2, selects the mode to which transition is made after a SLEEP instruction is executed.

- System Control Register 2 (SYSCR2) Address H'FFF1

Bit	Bit Name	Setting	R/W	Function
3	DTON	1	R/W	Direct Transfer ON Flag In combination with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2, selects the mode to which transition is made after a SLEEP instruction is executed.
2	MSON	0	R/W	Medium Speed ON Flag Selects whether the MCU operates in active (high-speed) or active (medium-speed) mode after exiting from standby, watch, or sleep mode. 0: Active (high-speed) mode 1: Active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	These bits select the operating clock frequency in subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: ϕw/8 01: ϕw/4 10: ϕw/2 11: ϕw

- Port Mode Register 1(PMR1) Address H'FFC0

Bit	Bit Name	Setting	R/W	Function
2	CLKOUT	0	R/W	P10/AEVH/FTIOA/TMOW/CLKOUT Pin Function Switching
1	TMOW	1	R/W	000: P10 I/O pin and FTIOA I/O pin
0	AEVH	0	R/W	001: AEVH input pin
				01x: TMOW pin
				100: CLKOUT output pin (ϕ_{OSC})
				101: CLKOUT output pin (ϕ_{OSC}/2)
				110: CLKOUT output pin (ϕ_{OSC}/4)
				111: Setting prohibited

[Legend] x: Don't care.

- Clock Source Select Register (RTCCSR) Address H'F06F

Bit	Bit Name	Setting	R/W	Function
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	These bits select the clock output from the TMOW pin when TMOW
4	SUB32K	1	R/W	output is enabled by PMR1.
				000: ϕ/4
				010: ϕ/8
				100: ϕ/16
				110: ϕ/32
				xx1: ϕW

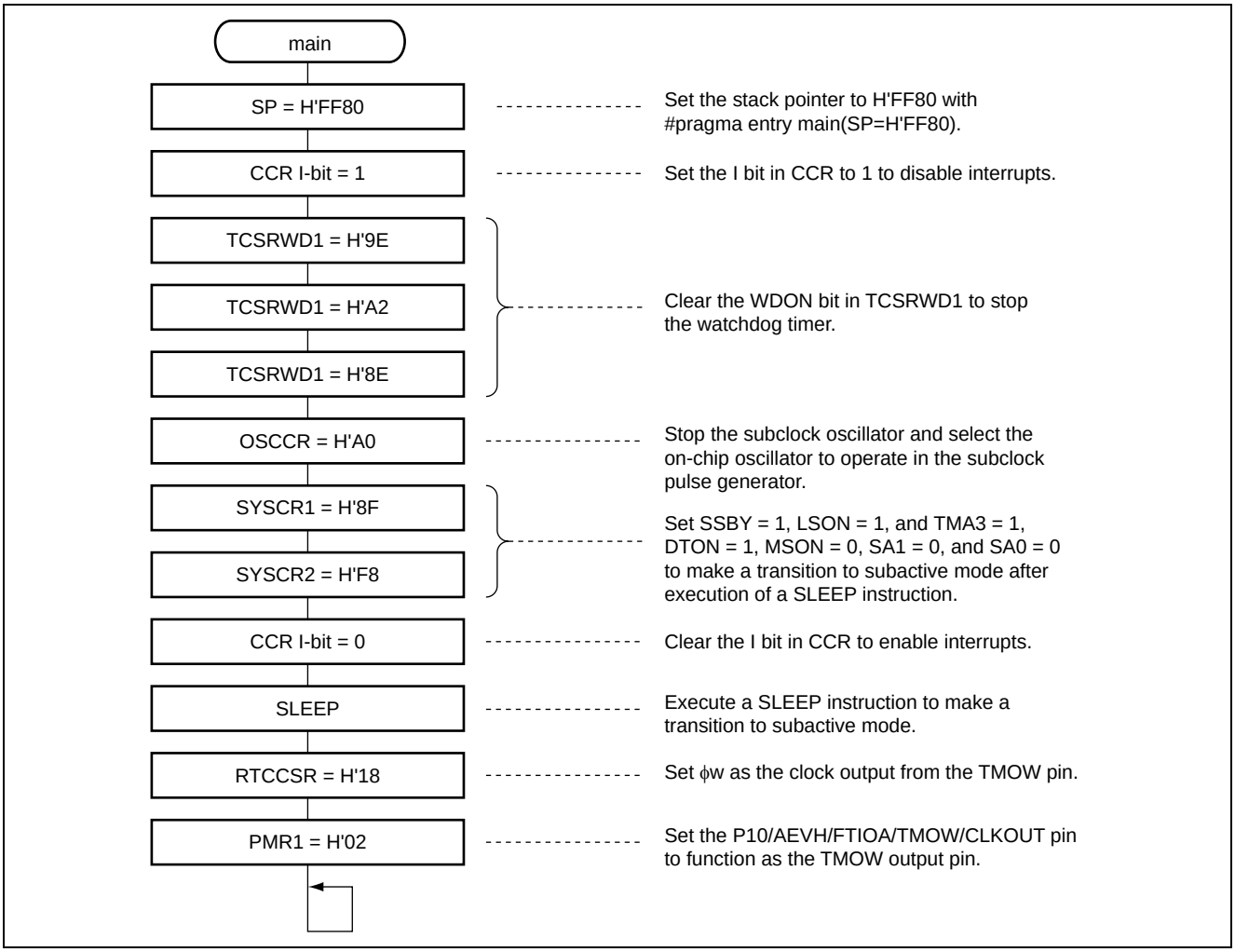
[Legend] x: Don't care.

4.4 RAM Usage

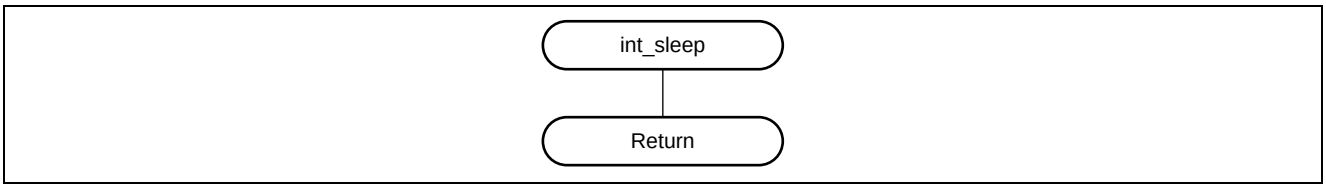
This sample program does not use on-chip RAM.

5. Flowchart

5.1 main



5.2 int_sleep



5.3 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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