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H8/38076R

PWM Output Using Timer F Output Compare Function

Introduction

The output compare function of timer F is used to output a PWM waveform from the TMOFH pin.
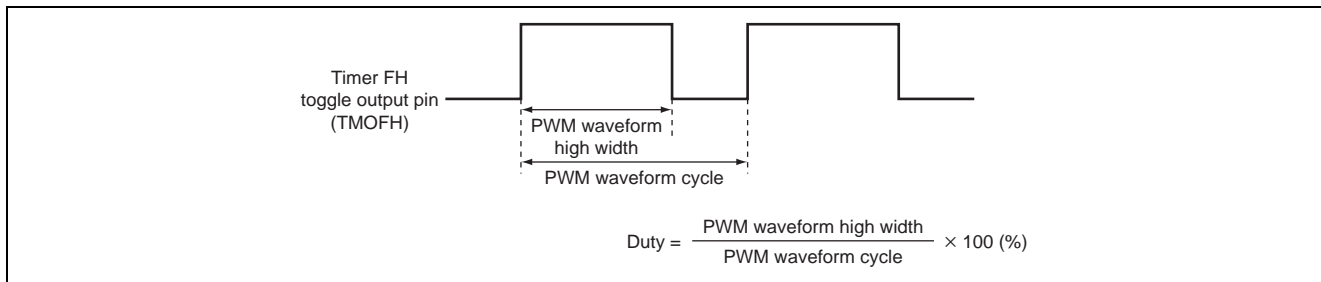
Target Device

H8/38076R

Contents

1. Specifications

Figure 1 shows the PWM out put.

- The period of the output PWM waveform is set by the overflow period of 8-bit timer counter FH (TCFH).
- The high width of the output PWM waveform is set by 8-bit output compare register FH (OCRFH).
- In this sample task a PWM waveform with a period of 819.2 µs and a duty cycle that changes 6.25% per period, within a range of 6.25% to 93.75%, is output.

Timer FH toggle output pin (TMOFH)

PWM waveform high width

PWM waveform cycle

$$\text{Duty} = \frac{\text{PWM waveform high width}}{\text{PWM waveform cycle}} \times 100 \ (\%)$$

Figure 1 PWM Output

2. Description of Functions

2.1 Functions

In this sample task the output compare function of timer F is used to output a PWM waveform from the TMOFH pin. A block diagram of the output compare function of timer F is shown in figure 2. The block diagram of the output compare function of timer F is described below.

1. System Clock (ϕ)
   This 10-MHz clock is the reference clock for operation of the CPU and peripheral functions.

2. Prescaler S (PSS)
   PSS is a 13-bit counter that takes ϕ as input and counts up once per period.

3. Timer F Functions
   This 16-bit timer has an output compare function. It can be used for external event counting or as a multifunction timer for a variety of applications, including counter resetting, interrupt request, and toggle output using compare match signals. It can also be used as two independent 8-bit timers (timer FH and timer FL).

- Timer counter FH (TCFH)
  TCFH is an 8-bit readable/writeable up-counter that is incremented by input of an internal or an external clock. Four input clock options are available: the system clock divided by 4, 16, or 32, or the subclock divided by 4.
- Timer control register F (TCRF)
  TCRF switches between 16-bit mode and 8-bit mode, selects the input clock, and selects the output level of the TMOFH and TMOFL pins.
- Timer control/status register F (TCSRF)
  TCSRF performs counter clear selection, overflow flag and compare match flag settings and controls enabling of overflow interrupt requests.
- Output compare register FH (OCRFH)
  OCRFH is an 8-bit readable/writeable register whose contents are constantly compared with TCFH. When the values match, a compare match FH is generated and toggle output occurs from the TMOFH pin. The contents of TCFH are constantly compared with OCRFH. When the values match, compare match flag H (CMFH) in TCSRF is set to 1. At this point an interrupt request is sent to the CPU. In this way a PWM waveform is output from the timer FH output pin (TMOFH).

4. Interrupt Controller Functions
   The following registers are used to control interrupts.

- Interrupt enable register 2 (IENR2)
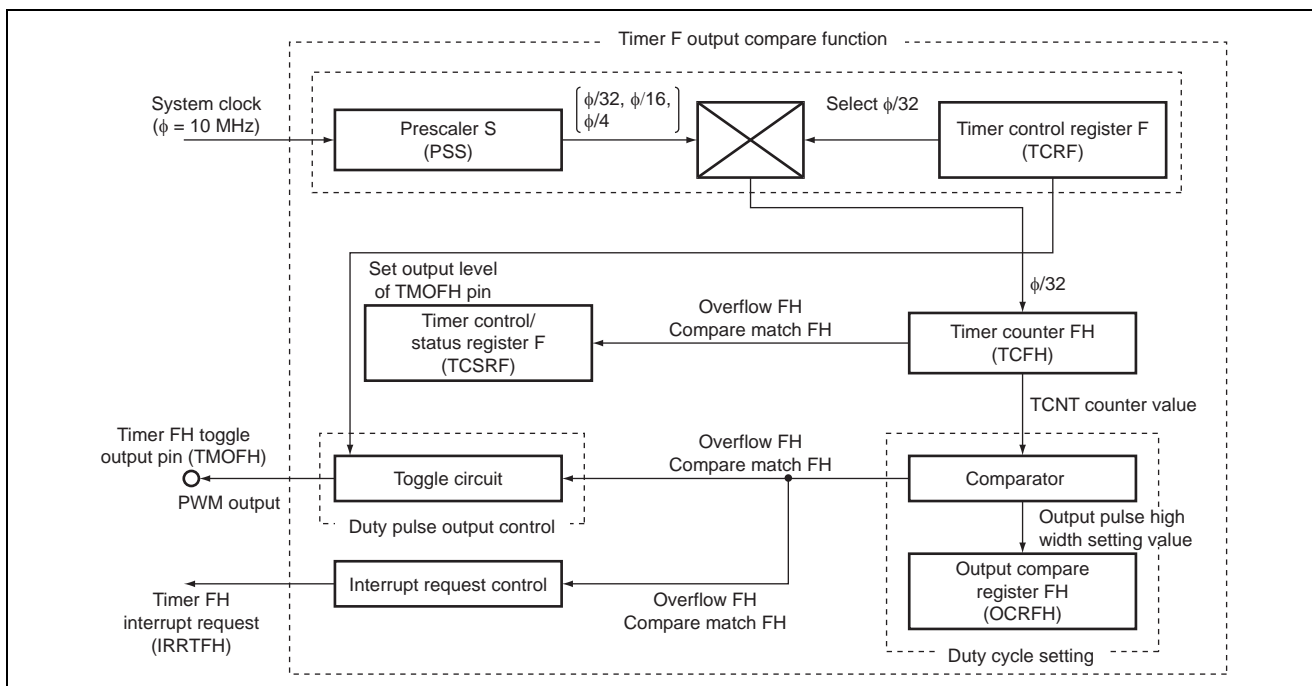 IENR2 controls timer F interrupts.
- Interrupt request register 2 (IRR2)
  IRR2 is the interrupt request status register for timer F interrupts.

5. I/O Port Functions
   The following register is used to set pin functions.

- Port mode register 4 (PMR4)
  PMR4 is used to set the P42/TXD31/IrTXD/TMOFH pin as a TMOFH output pin.

Figure 2 Block Diagram of Output Compare Function of Timer F

2.2   Assignment of Functions

Table 1 shows the assignment of functions in this sample task. The output compare function of timer F is used to output a PWM waveform using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Classification	Description
TMOFH	Pin	Timer FH toggle output pin
TCFH	Timer F	Timer counter FH
OCRFH	Timer F	Sets PWM high width to output from TMOFH pin
TCRF	Timer F	Sets TCFH as 8-bit counter, selects φ/32 as internal clock, and sets output level of TMOFH pin to high
TCSRF	Timer F	Enables TCFH overflow interrupts, timer F status register, disables clearing TCFH by compare match
IENTFH	Interrupt controller	Enables/disables timer FH interrupt requests
IRR2	Interrupt controller	Timer FH interrupt request status register

2.3 PWM Settings

The method of setting the period and duty cycle of the PWM output waveform used in this sample task is shown in figure 3.
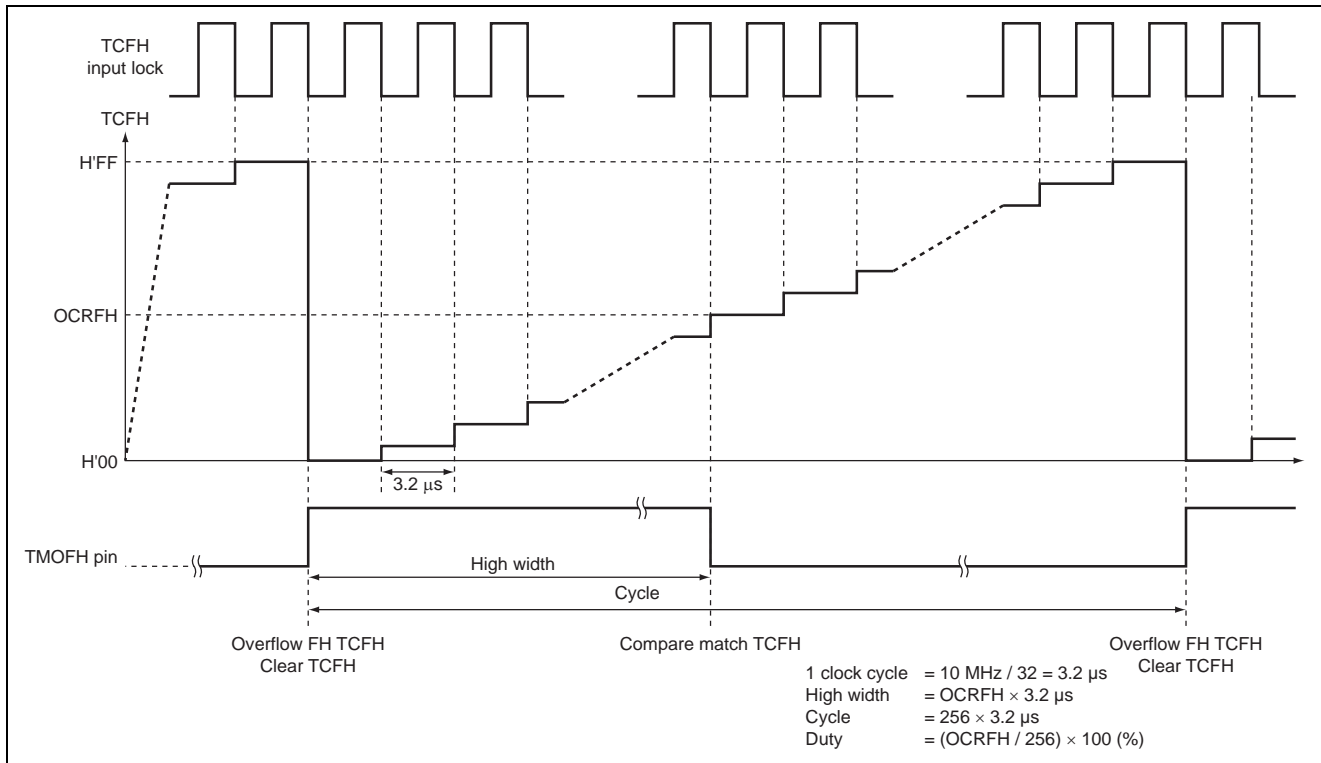
Figure 3 Method for Setting Period and Duty Cycle of PWM Output Waveform

2.4 Increasing the PWM Duty Cycle

The duty cycle is increased by rewriting OCRFH using the timing shown in figure 4. The contents of OCRFH are updated simultaneously with the write to OCRFH. If the duty cycle is increased by rewriting OCRFH during interval a in figure 4, compare match FH will not be generated successively before the overflow interrupt occurs and the PWM waveform output will be abnormal. It is therefore necessary to rewrite OCRFH during interval b in figure 4. In this sample task OCRFH is rewritten during overflow FH interrupt handling.
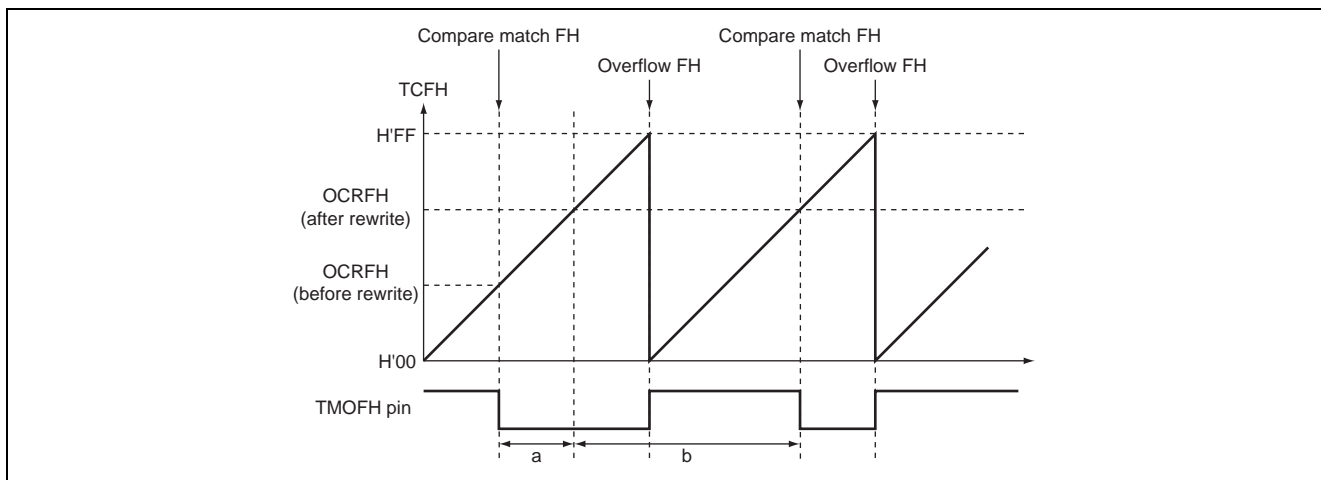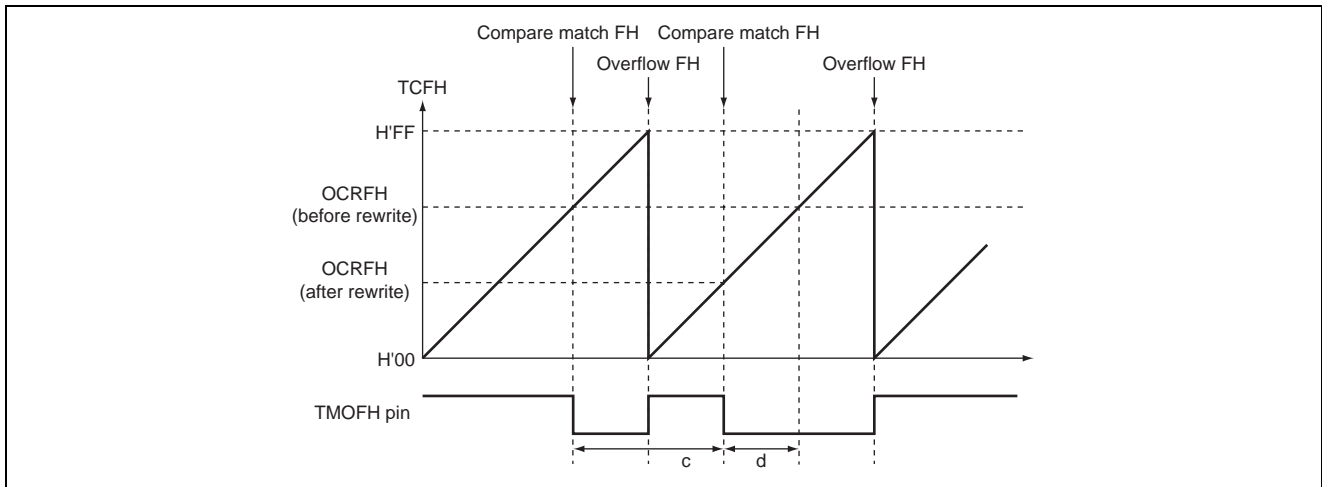

Figure 4 OCRFH Rewrite Timing When Increasing Duty Cycle

2.5 Decreasing the PWM Duty Cycle

The duty cycle is decreased by rewriting OCRFH using the timing shown in figure 5. The contents of OCRFH are updated simultaneously with the write to OCRFH. If the duty cycle is decreased by rewriting OCRFH during interval d in figure 5, the next compare match FH will not be generated and the PWM waveform output will be abnormal. It is therefore necessary to rewrite OCRFH during interval c in figure 5. In this sample task OCRFH is rewritten during compare match FH interrupt handling.

Figure 5 OCRFH Rewrite Timing When Decreasing Duty Cycle

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 6. Using the hardware and software processing shown in figure 6 the output compare function of timer F is used to output a PWM waveform.
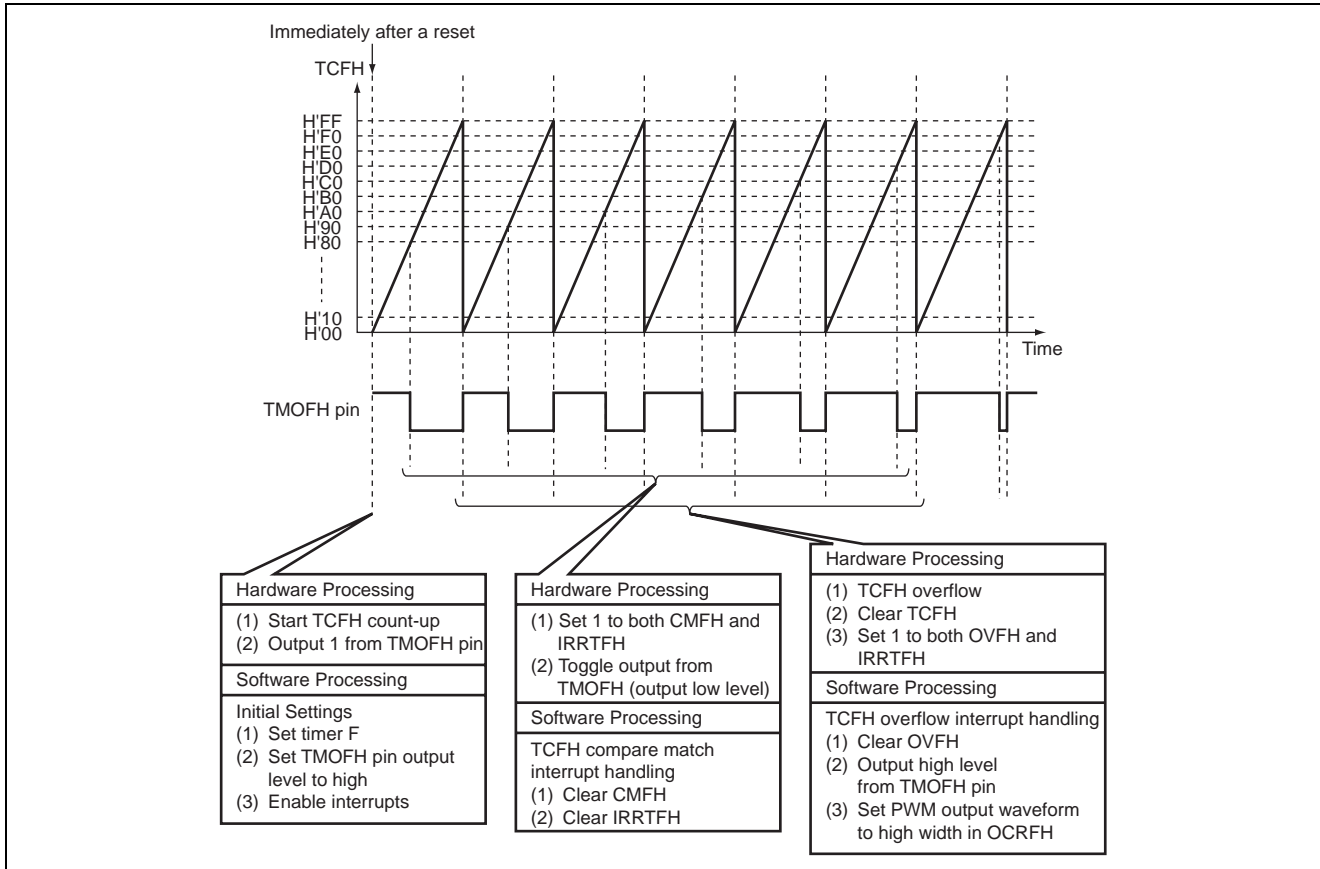
Figure 6 Principles of Operation for Using Output Compare Function of Timer F to Output PWM Waveform

4. Description of Software

4.1 Description of Modules

Table 2 shows the functions used in this sample task.

Table 2 List of Functions

Function Name	Description
main	Settings for timer F output compare function
	Sets TCFH as an 8-bit timer, selects φ/32 as the clock source, enables TCFH overflow interrupts, disables clearing TCFH by compare match, selects the TMOFH pin settings, and enables interrupts
tfhint	Timer F interrupt handling
	For overflow interrupts, clears OVFH and IRRTFH and rewrites OCRFH
	For compare match interrupts, clears CMFH and IRRTFH

4.2 Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

The internal registers used in this sample task are shown below.

- TCRF   Timer Control Register F   Address: H'FFB6

Bit	Bit Name	Set Value	R/W	Description
7	TOLH	1	W	Toggle Output Level H
				Sets the TMOFH pin output level.
				0: Low level
				1: High level
6	CKSH2	1	W	Clock Select H
5	CKSH1	0	W	Selects the clock input to TCFH from among internal clock sources
4	CKSH0	0	W	or TCFL overflow.
				100: 8-bit mode, counting on internal clock φ/32
2	CKSL2	0	W	Clock Select L
1	CKSL1	1	W	Select the clock input to TCFL from among internal clock sources
0	CKSL0	1	W	or external event input.
				011: Use disabled

- TCSRF   Timer Control/Status Register F   Address: H'FFB7

Bit	Bit Name	Set Value	R/W	Description
7	OVFH	Undefined	R/W*	Timer Overflow Flag H [Setting condition] • When TCFH overflows from H'FF to H'00 [Clearing condition] • When 0 is written to this bit after reading it as 1
6	CMFH	Undefined	R/W*	Compare Match Flag H This is a status flag that indicates a match between TCFH and OCRFH. [Setting condition] • When the TCFH value matches the OCRFH value [Clearing condition] • When 0 is written to this bit after reading it as 1
5	OVIEH	1	R/W	Timer Overflow Interrupt Enable H Enables or disables interrupt generation when TCFH overflows. 1: TCFH overflow interrupt requests enabled
4	CCLRH	0	R/W	Counter Clear H In 8-bit mode, this bit selects whether TCFH is cleared when TCFH and OCRFH match. In 8-bit mode: 0: TCFH clearing by compare match disabled

Note: * Only 0 can be written to clear the flag.

- TCFH   Timer Counter FH   Address: H'FFB8

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	1	R/W	Count-up Compare Register FH
6	Bit 6	0	R/W	When CKSH2 in TCRF is set to 1, TCFH and TCFL operate as two
5	Bit 5	0	R/W	independent 8-bit counters. The TCFH (TCFL) input clock is
4	Bit 4	0	R/W	selected by bits CKSH2 to CKSH0 (CKSL2 to CKSL0) in TCRF.
3	Bit 3	0	R/W	TCFH (TCFL) can be cleared in the event of a compare match by
2	Bit 2	0	R/W	CCLRH (CCLRL) in TCSRF.
1	Bit 1	0	R/W	When TCFH (TCFL) overflows from H'FF to H'00, OVFH (OVFL) in
0	Bit 0	0	R/W	TCSRF is set to 1. If the value of OVIEH (OVIEL) in TCSRF is 1 at this time, IRRTFH (IRRTFL) in IRR2 is set to 1, and if in addition the value of IENTFH (IENTFL) in IENR2 is 1, an interrupt request is sent to the CPU.

- OCRFH   Output Compare Register FH   Address: H'FFBA

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	1	R/W	Output Compare Register FH
6	Bit 6	0	R/W	When CKSH2 in TCRF is set to 1, OCRF operates as two
5	Bit 5	0	R/W	independent 8-bit registers. The contents of OCRFH are compared
4	Bit 4	0	R/W	with TCFH and the contents of OCRFL with TCFL.
3	Bit 3	0	R/W	If the OCRFH (OCRFL) and TCFH (TCFL) values match, CMFH
2	Bit 2	0	R/W	(CMFL) in TCSRF is set to 1. At the same time, IRRTFH (IRRTFL)
1	Bit 1	0	R/W	in IRR2 is set to 1. If the value of IENTFH (IENTFL) in IENR2 is 1
0	Bit 0	0	R/W	at this time an interrupt request is sent to the CPU.
				Toggle output can be provided from the TMOFH pin (TMOFL pin) using the compare match function, and the output level can be set by the TOLH (TOLL) bit in TCRF.

- PMR4   Port Mode Register 4   Address: H'FFC3

Bit	Bit Name	Set Value	R/W	Description
2	TMOFH	1	R/W	P42/TXD31/IrTXD/TMOFH Pin Function Switch
				Selects whether pin P42/TXD31/IrTXD/TMOFH is used as P42, TXD31/IrTXD, or as TMOFH.
				1: Functions as TMOFH output pin

- IENR2   Interrupt Enable Register 2   Address: H'FFF4

Bit	Bit Name	Set Value	R/W	Description
3	IENTFH	1	R/W	Timer FH Interrupt Enable
				Timer FH interrupt requests are enabled when this bit is set to 1.
				1: Timer FH interrupt requests enabled

- IRR2   Interrupt Request Register 2   Address: H'FFF7

Bit	Bit Name	Set Value	R/W	Description
3	IRRTFH	Undefined	R/W	Timer FH Interrupt Request Flag
				[Setting condition]
				• When timer FH compare match or overflow occurs
				[Clearing condition]
				• When 0 is written to this bit

4.4   RAM Usage

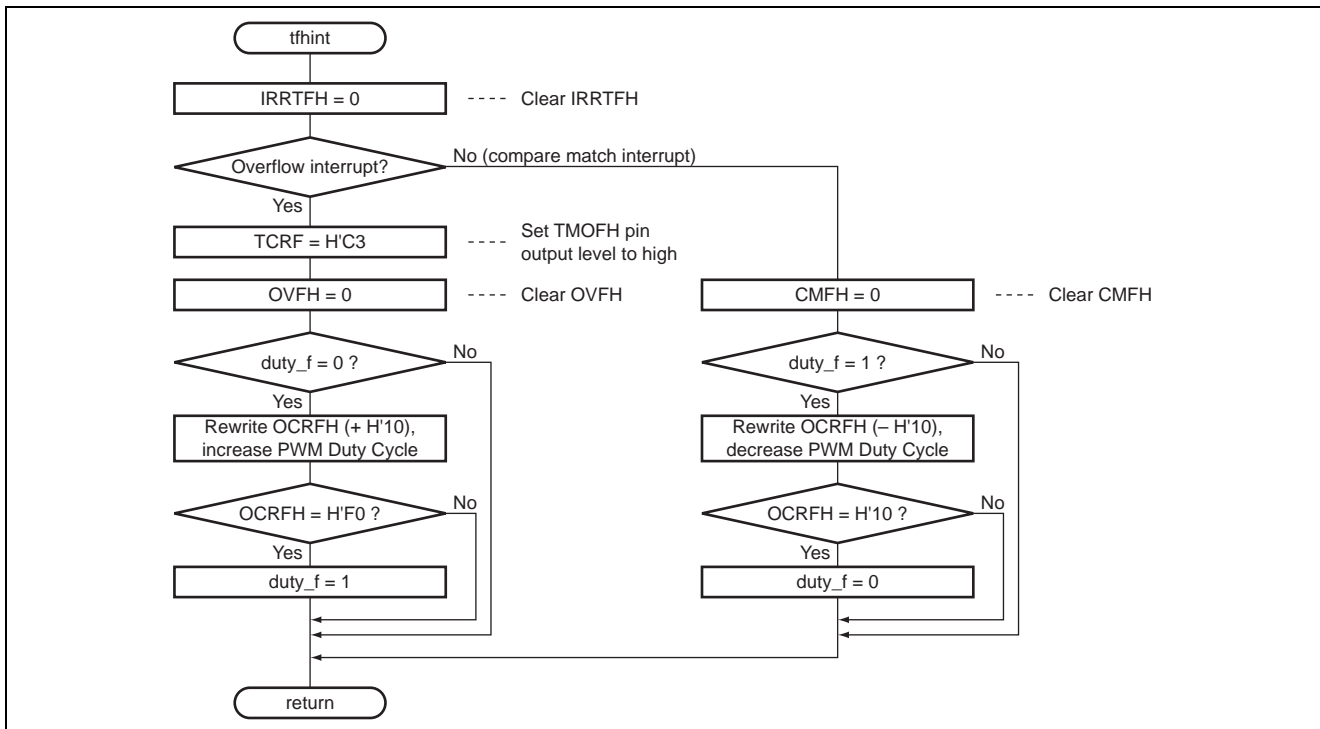The RAM usage in this sample task is shown in table 3.

Table 3 RAM Usage

Label	Description	Amount of Memory Used	Used in
duty_f	Indicates whether the duty cycle of the PWM output from the TMOFH toggle output pin increases or decreases 0: Increase PWM duty cycle 1: Decrease PWM duty cycle	1 byte	main tfhint

5. Flowchart

5.1 main

main	
SP = H'FF80	- - - - Initialize stack pointer
CCR I-bit = 1	- - - - Set I bit in CCR to 1, disable interrupts
duty_f = 0	- - - - Initialize RAM area to be used
TCRF = H'C3	- - - - Select 8-bit mode, count TCFH at φ/32 of internal clock, set output level of TMOFH pin to high
OCRFH = H'80	- - - - Select 50% duty cycle for high width of PWM output from TMOFH pin
TCFH = H'00	- - - - Initialize TCFH
tmp = TCSRF TCSRF = H'20	- - - - Enable interrupt requests at TCFH overflow, clear OVFH and CMFH at compare match of TCFH and OCRFH, disable clearing of TCFH
TMOFH = 1	- - - - Select TMOFH pin function
IRRTFH = 0	- - - - Clear IRRTFH
IENTFH = 1	- - - - Enable TCFH interrupt requests (compare match, overflow)
CCR I-bit = 0	- - - - Set I bit in CCR to 1 to enable interrupts

5.2 tfhint

tfhint

IRRTFH = 0 - - - - Clear IRRTFH

Overflow interrupt? — No (compare match interrupt) →

Yes:
TCRF = H'C3 - - - - Set TMOFH pin output level to high
OVFH = 0 - - - - Clear OVFH
duty_f = 0 ? — No
Yes: Rewrite OCRFH (+ H'10), increase PWM Duty Cycle
OCRFH = H'F0 ? — No
Yes: duty_f = 1

No (compare match):
CMFH = 0 - - - - Clear CMFH
duty_f = 1 ? — No
Yes: Rewrite OCRFH (– H'10), decrease PWM Duty Cycle
OCRFH = H'10 ? — No
Yes: duty_f = 0

return

5.3　Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued