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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# H8/38076R

## Module Standby Mode

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### Introduction

This application note describes the module standby mode of the H8/38076R.

### Target Device

H8/38076R

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## 1. Description of Functions

### 1.1 Functions Used

The functions used in this sample are described below.

#### 1. Module Standby Mode

The module standby function can be used to reduce power consumption by halting the operation of unused internal modules on an individual basis. The module standby function has settings for all of the device's internal modules. No clock is supplied to modules that have been set to module standby mode, thereby reducing power consumption. Clearing a bit in clock halt register 1 (CKSTPR1) or clock halt register 2 (CKSTPR2) to 0 puts the corresponding module into module standby mode. Setting a bit to 1 clears module standby mode for the corresponding module. These two registers are described below.

- CKSTPR1      Clock halt register 1      Address: H'FFFA

Bit	Bit Name	Initial Value	R/W	Description
7	S4CKSTP <sup>*1</sup>	1	R/W <sup>*1</sup>	SCI4 module standby 0: Sets SCI4 to module standby mode 1: Clears SCI4 from module standby mode
6	S31CKSTP	1	R/W	SCI3 module standby <sup>*2</sup> 0: Sets SCI3 to module standby mode 1: Clears SCI3 from module standby mode
5	S32CKSTP	1	R/W	SCI3 module standby <sup>*2</sup> 0: Sets SCI3 to module standby mode 1: Clears SCI3 from module standby mode
4	ADCKSTP	1	R/W	A/D converter module standby 0: Sets A/D converter to module standby mode 1: Clears A/D converter from module standby mode
3	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
2	TFCKSTP	1	R/W	Timer F module standby 0: Sets timer F to module standby mode 1: Clears timer F from module standby mode
1	FROMCKSTP	1	R/W	Flash memory module standby 0: Sets flash memory to module standby mode 1: Clears flash memory from module standby mode
0	RTCKSTP	1	R/W	RTC module standby 0: Sets RTC to module standby mode 1: Clears RTC from module standby mode

Notes: 1. In the mask ROM version this is a reserved bit that is not readable or writable.

2. When the SCI3 is set to module standby, all registers in the SCI3 enter the reset state.

- CKSTPR2                      Clock halt register 2                      Address: H'FFFB

Bit	Bit Name	Initial Value	R/W	Description
7	ADBCKSTP	1	R/W	Address break module standby 0: Sets address break to module standby mode 1: Clears address break from module standby mode
6	TPUCKSTP	1	R/W	TPU module standby 0: Sets TPU to module standby mode 1: Clears TPU from module standby mode
5	IICCKSTP	1	R/W	IIC2 module standby 0: Sets IIC2 to module standby mode 1: Clears IIC2 from module standby mode
4	PW2CKSTP	1	R/W	PWM2 module standby 0: Sets PWM2 to module standby mode 1: Clears PWM2 from module standby mode
3	AECCKSTP	1	R/W	Asynchronous event counter module standby 0: Sets asynchronous event counter to module standby mode 1: Clears asynchronous event counter from module standby mode
2	WDCKSTP*	1	R/W	Watchdog timer module standby 0: Sets watchdog timer to module standby mode 1: Clears watchdog timer from module standby mode
1	PW1CKSTP	1	R/W	PWM1 module standby 0: Sets PWM1 to module standby mode 1: Clears PWM1 from module standby mode
0	LDCKSTP	1	R/W	LCD module standby 0: Sets LCD to module standby mode 1: Clears LCD from module standby mode

Note: \* WDCKSTP is valid when the WDON bit in timer control/status register WD1 (TCSRWD1) is 0. If this bit is cleared to 0 while the WDON bit is set to 1 (while the watchdog timer is operating), this bit is cleared to 0. However, the watchdog timer does not enter module standby mode and continues operating. When the watchdog timer stops operating and the WDON bit is cleared to 0 by software, WDCKSTP becomes valid and the watchdog timer enters module standby mode.

### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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