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H8/38076R

Master-Slave Communication Using I²C Bus Interface 2

Introduction

In this example the I²C2 (Inter IC Bus Interface 2) module of the H8/38076R is used to implement master-slave communication in I²C bus format.

Target Device

H8/38076R

Contents

1. Specifications

- The I²C bus interface 2 of the H8/38076R is used for communication between microcomputers as shown in figure 1.
- In this sample task 4 bytes of data are transmitted from an H8/38076R operating in the master mode and received by an H8/38076R operating in the slave mode.
- The slave H8/38076R then transmits the receive data to the master H8/38076R.
- The data transfer clock frequency is 250 kHz.

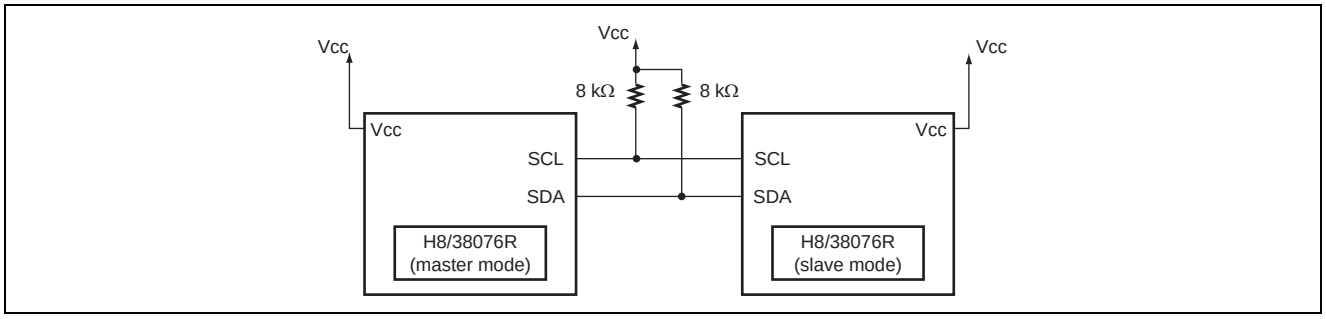


Figure 1 Connection Diagram for Master-Slave Communication Using I²C Bus Interface 2

2. Description of Functions

2.1 Functions Used

In this sample task the I²C bus interface 2 is used for master-slave communication. A block diagram of the I²C bus interface 2 is shown in figure 2, and its functions are described below.

1. I²C Bus Interface 2 Functions
   The I²C bus interface 2 conforms to and provides a subset of the Philips I²C bus (Inter IC Bus) interface functions.

- I²C bus control register 1 (ICCR1)
  ICCR1 enables or disables the I²C bus interface 2, controls transmission and reception, and selects the master mode or the slave mode, transmission or reception, and the transfer clock frequency in the master mode. In this sample task the transfer clock frequency is set to 250 kHz.

- I²C bus control register 2 (ICCR2)
  ICCR2 issues start/stop conditions, manipulates the SDA pin, monitors the SCL pin state, and controls resets of the control block of the I²C bus interface 2.

- I²C bus mode register (ICMR)
  ICMR selects whether the MSB or LSB is transferred first, performs master mode wait control, and selects the transfer bit count.

- I²C bus status register (ICSR)
  ICSR confirms interrupt request flags and status.

- I²C bus interrupt enable register (ICIER)
  ICIER enables interrupt sources, enables or disables acknowledge bits, sets acknowledge bits to be transferred, and confirms acknowledge bits to be received.

- I²C bus transmit data register (ICDRT)
  ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the shift register (ICDRS), it transfers the transmit data which was written to ICDRT to ICDRS and starts transferring data. Continuous transfer is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. If the MLS bit of ICMR is set to 1, MSB/LSB inverted data is read after the data is written to ICDRT.

- I²C bus receive data register (ICDRR)
  ICDRR is an 8-bit register that stores receive data. After one byte of data is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, so the CPU cannot write to it.

- I²C bus shift register (ICDRS)
  ICDRS is a register that is used to transmit and receive data. In transmission, data is transferred from ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred from ICDRS to ICDRR after one byte of data is received. This register cannot be read directly from the CPU.

- Slave address register (SAR)
  SAR selects the communication format and sets the slave address. When the device is in the slave mode with the I²C bus format, it operates as the slave device if the upper 7 bits of SAR match the upper 7 bits of the first frame received after a start condition.

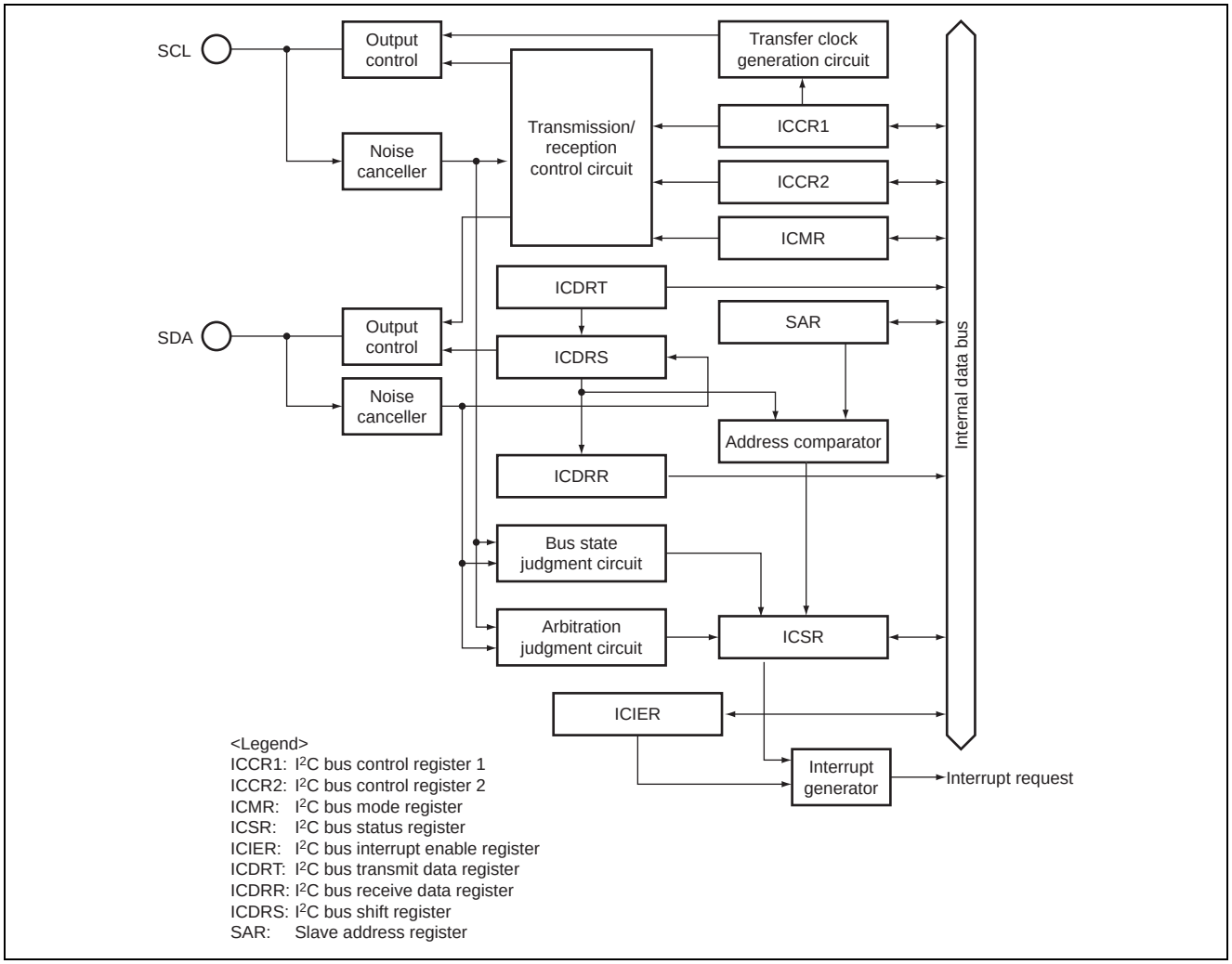


Figure 2 Block Diagram of I²C Bus Interface 2

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task.
Master-slave communication using the I²C bus interface 2 is implemented using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Classification	Description
SCL	Pin	I²C serial clock I/O pin
SDA	Pin	I²C serial data I/O pin
ICRR1	I²C2	Starts and stops operation of I²C bus interface 2, controls transmission and reception, selects the master mode or the slave mode, selects master mode transfer clock frequency
ICRR2	I²C2	Issues start and stop conditions, manipulates SDA pin
ICMR	I²C2	Selects MSB or LSB first, performs master mode wait control, selects the number of bits to be transferred
ICSR	I²C2	Status flag indicating the I²C operation state
ICIER	I²C2	Enables or disables acknowledge bits, sets acknowledge bits to be transferred, and confirms acknowledge bits to be received
ICDRT	I²C2	Register for storing transmit data
ICDRR	I²C2	Register for storing receive data
ICDRS	I²C2	Register for transmitting and receiving data
SAR	I²C2	Selects format, sets slave address

3. Sequence Diagrams

3.1 Master Transmit and Slave Receive Operations

Figure 3 is a sequence diagram of the master transmit and slave receive operation used in this sample task.

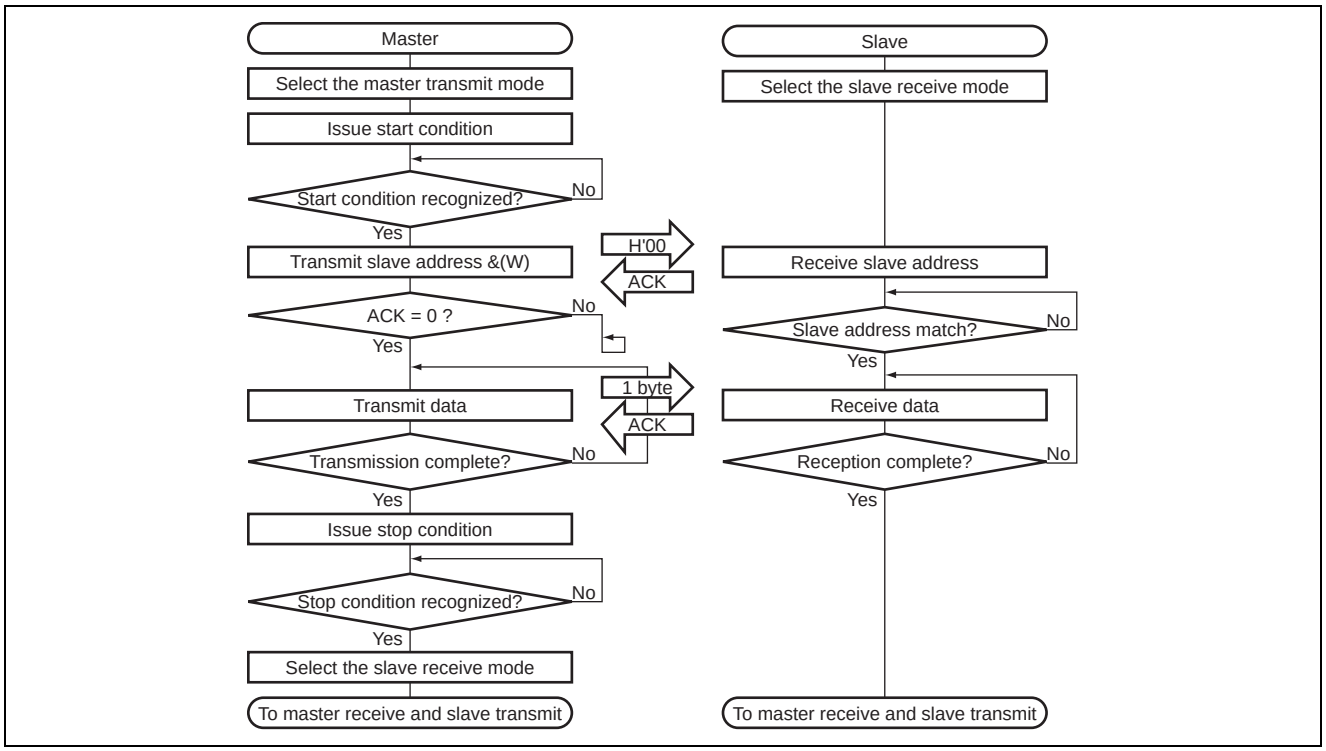


Figure 3 Master Transmit and Slave Receive Sequence Diagram

3.2 Master Receive and Slave Transmit Operations

Figure 4 is a sequence diagram of the master receive and slave transmit operation used in this sample task.

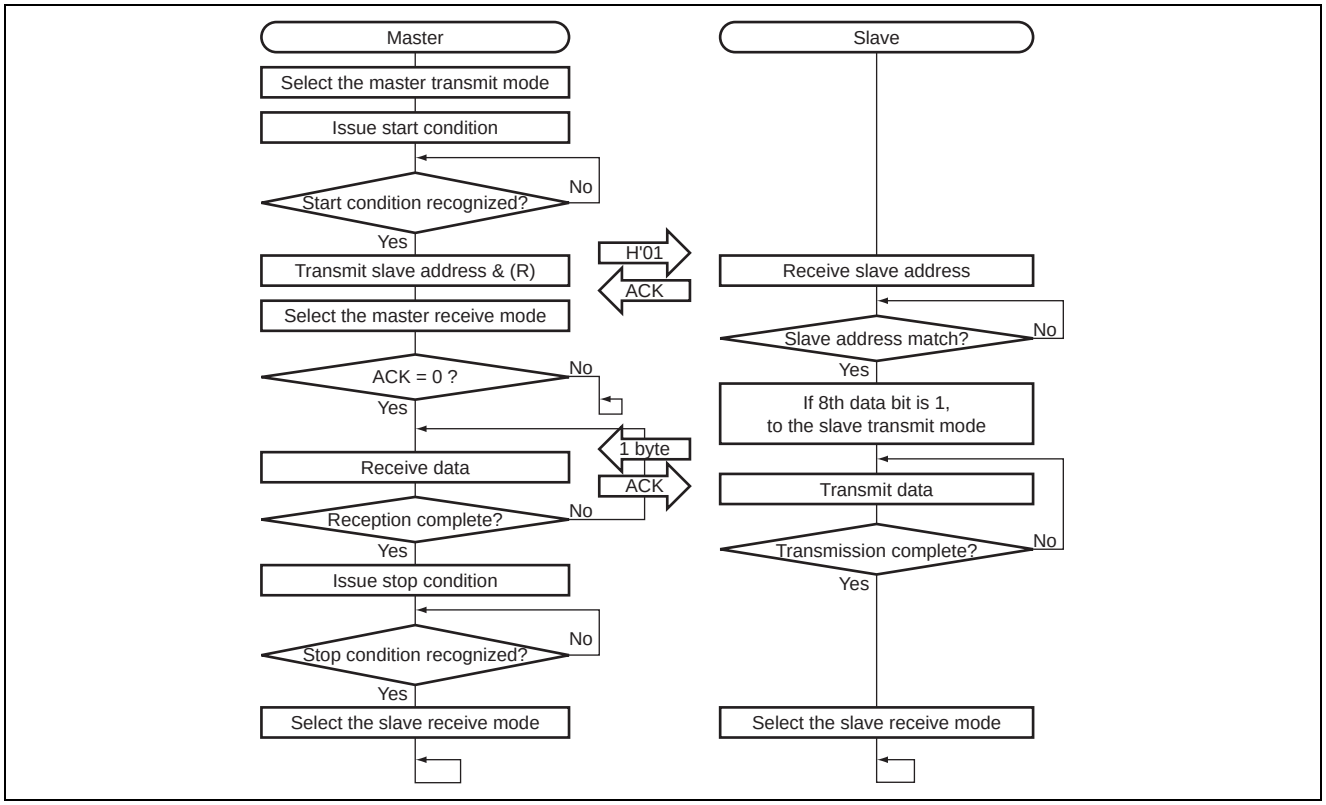


Figure 4 Master Receive and Slave Transmit Sequence Diagram

4. Principles of Operation

4.1 Master Transmit Mode

The operation timing in the master transmit mode for this sample task is illustrated in figures 5 and 6. Furthermore, details of the hardware and software processings are shown.

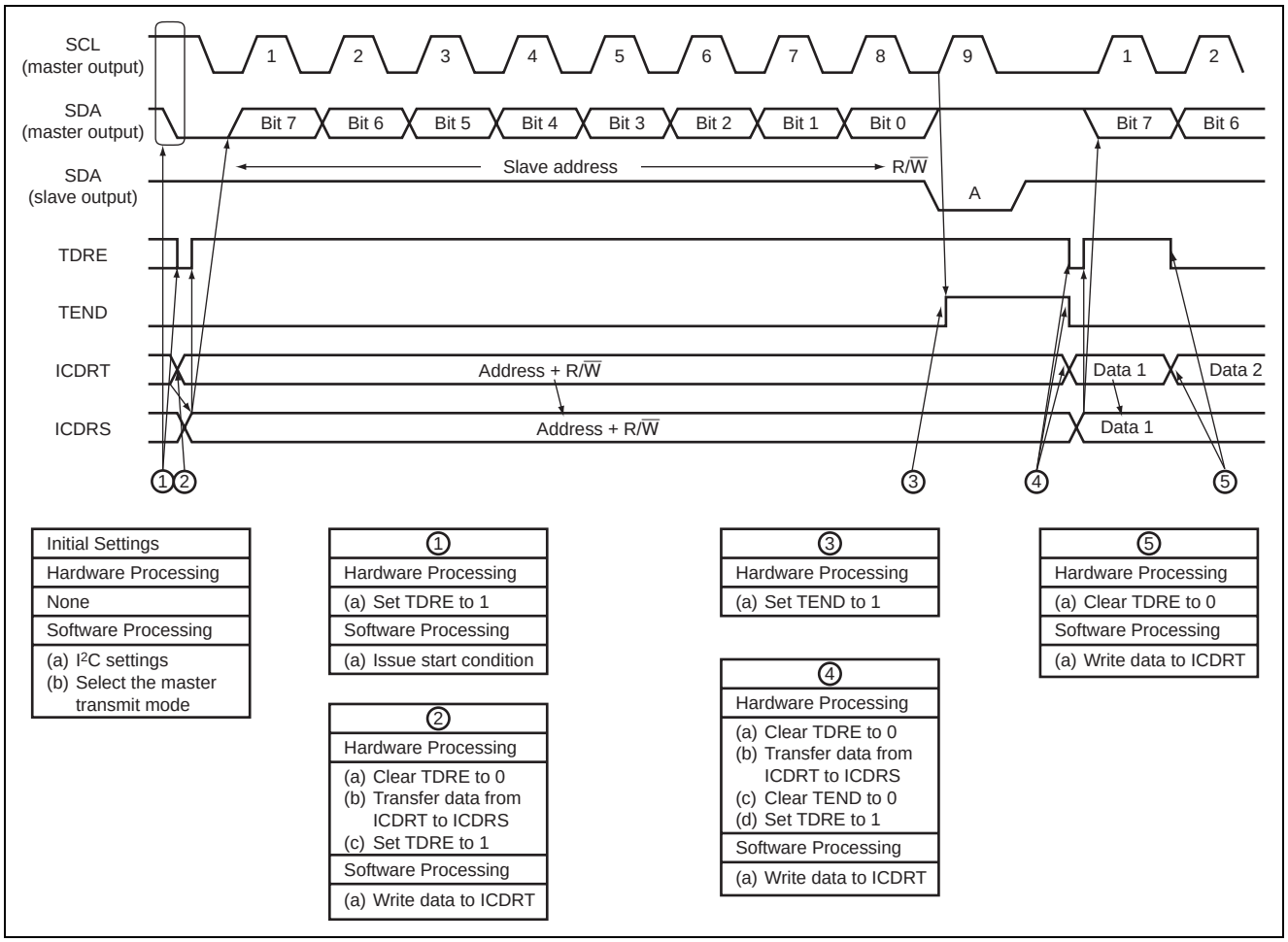


Figure 5 Master Transmit Mode Operation Timing 1

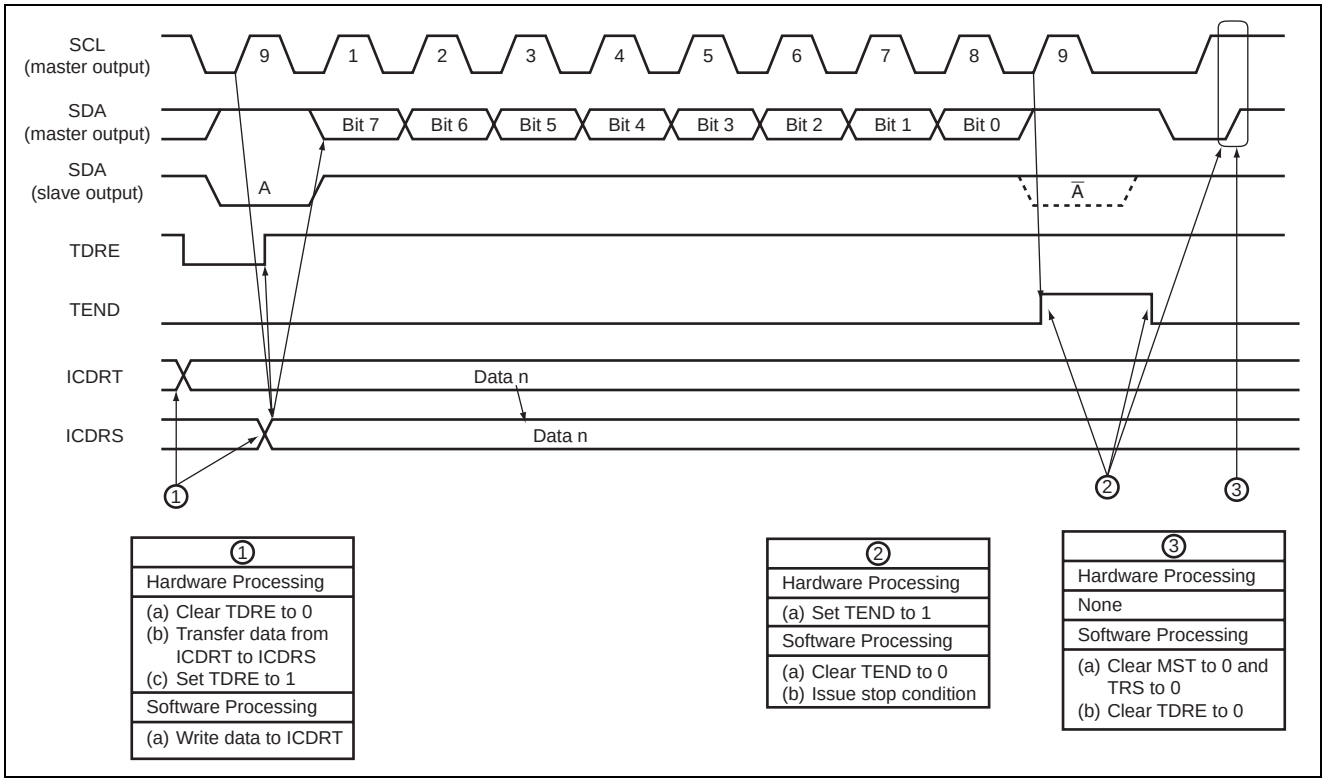


Figure 6 Master Transmit Mode Operation Timing 2

4.2 Master Receive Mode

The operation timing in the master receive mode for this sample task is illustrated in figures 7 and 8. Furthermore, details of the hardware and software processings are shown.

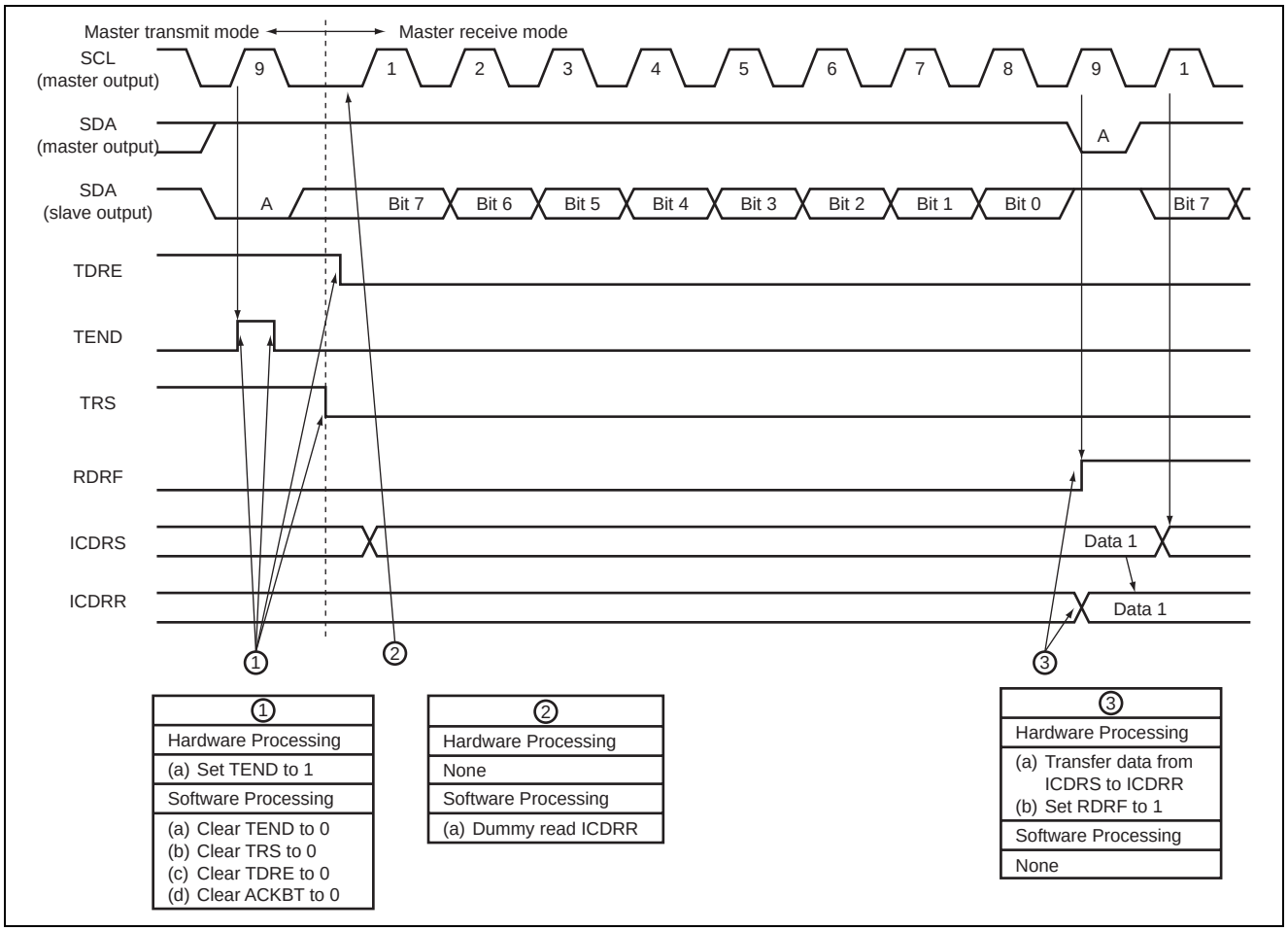


Figure 7 Master Receive Mode Operation Timing 1

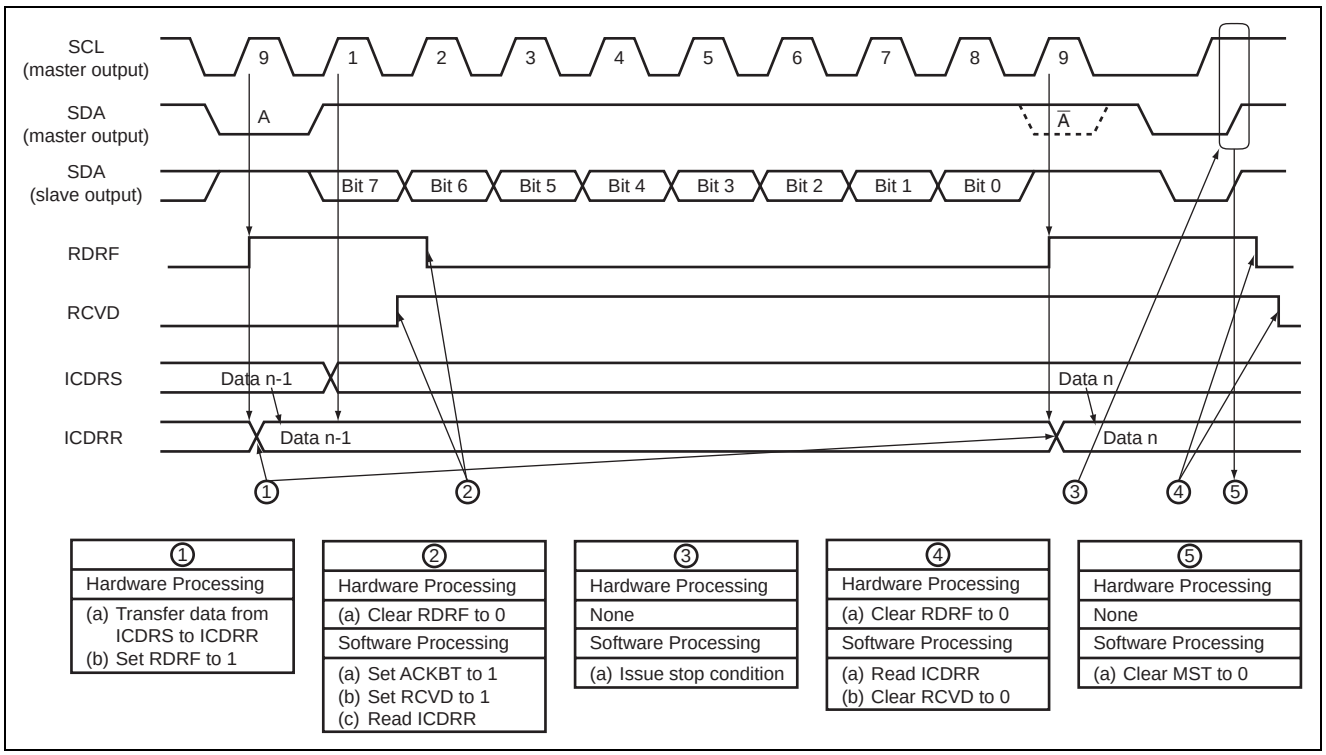


Figure 8 Master Receive Mode Operation Timing 2

4.3 Slave Transmit Mode

The operation timing in the slave transmit mode for this sample task is illustrated in figures 9 and 10. Furthermore, details of the hardware and software processings are shown.

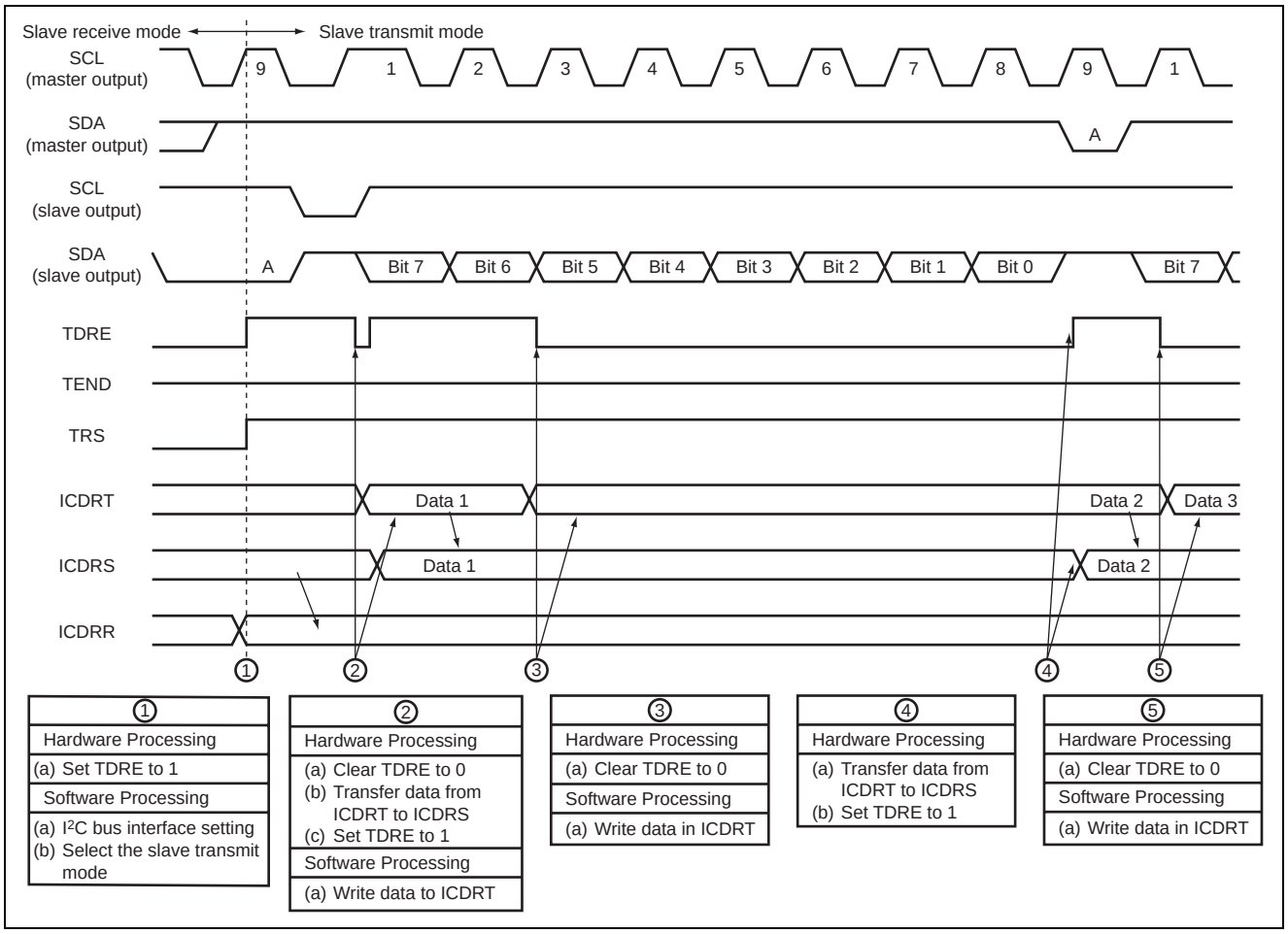


Figure 9 Slave Transmit Mode Operation Timing 1

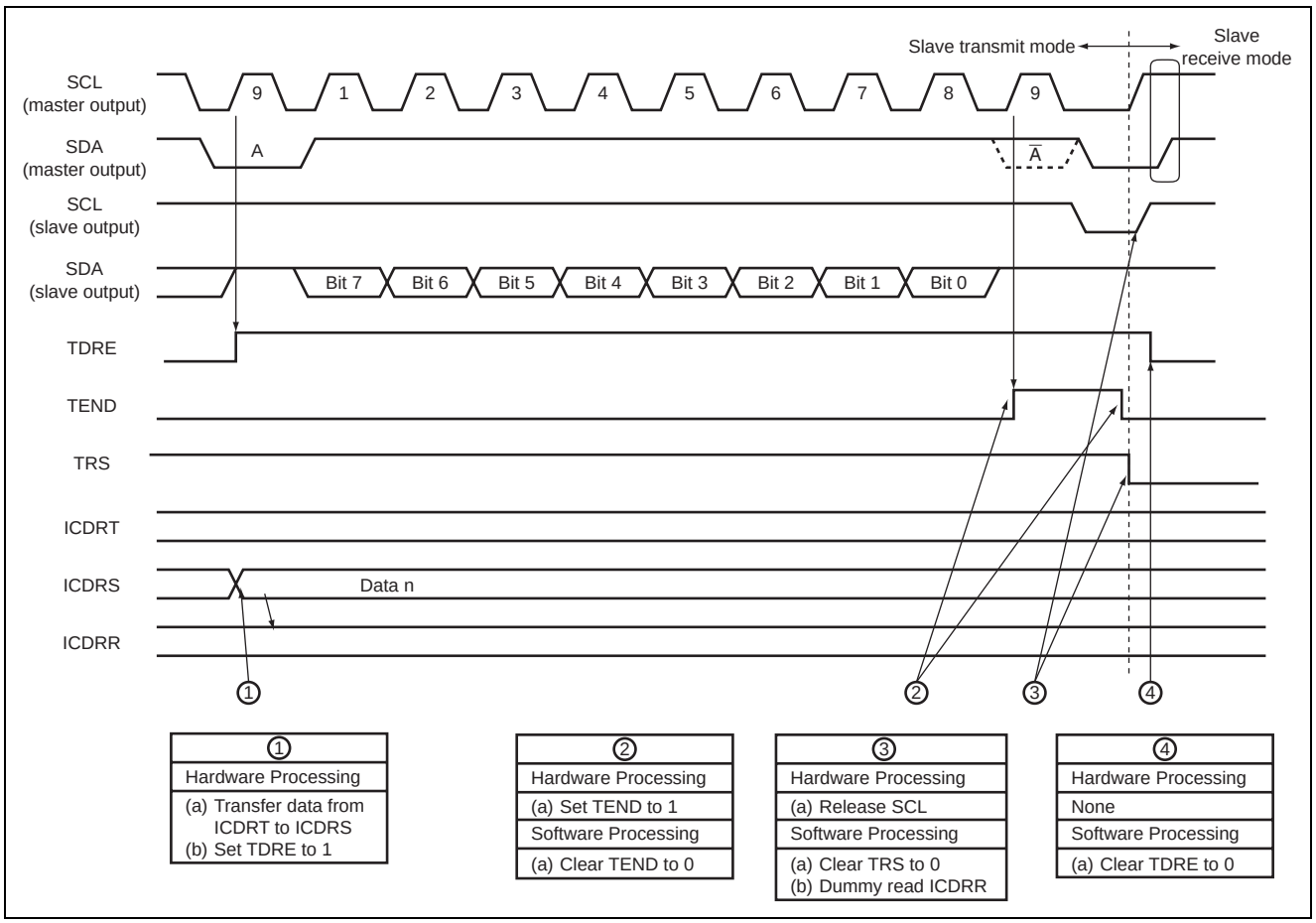


Figure 10 Slave Transmit Mode Operation Timing 2

4.4 Slave Receive Mode

The operation timing in the slave receive mode for this sample task is illustrated in figures 11 and 12. Furthermore, details of the hardware and software processings are shown.

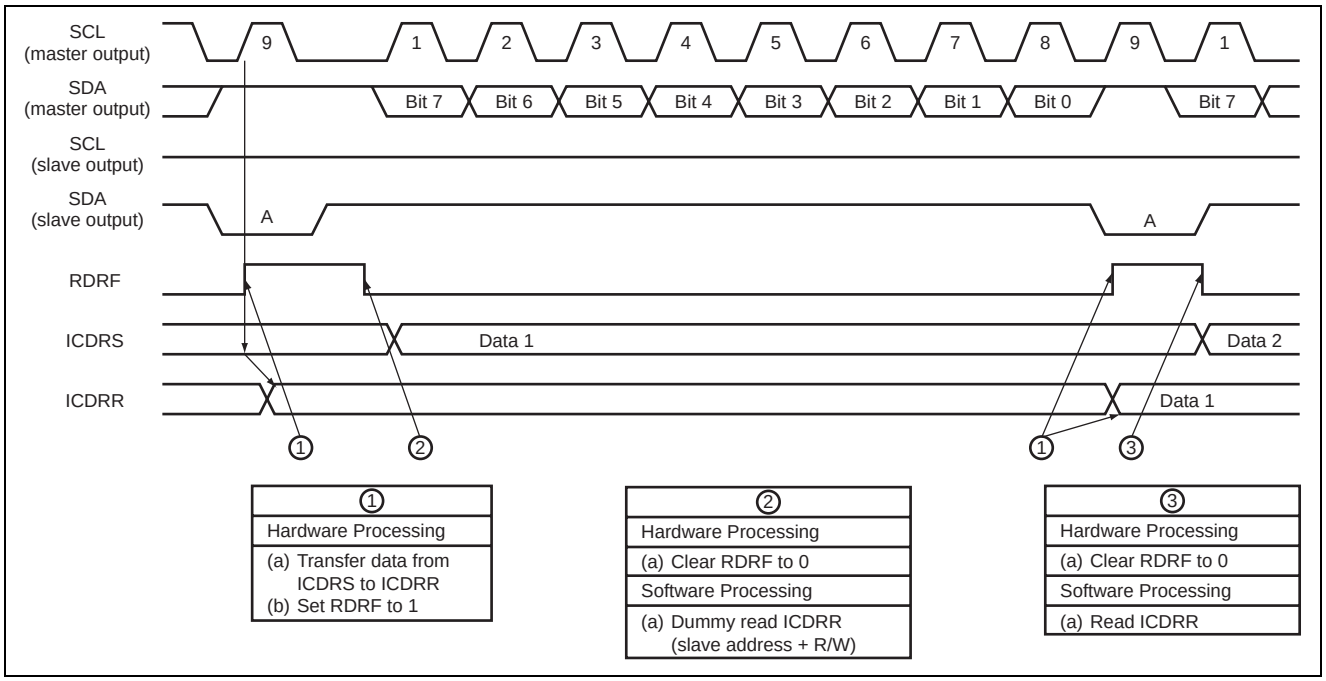


Figure 11 Slave Receive Mode Operation Timing 1

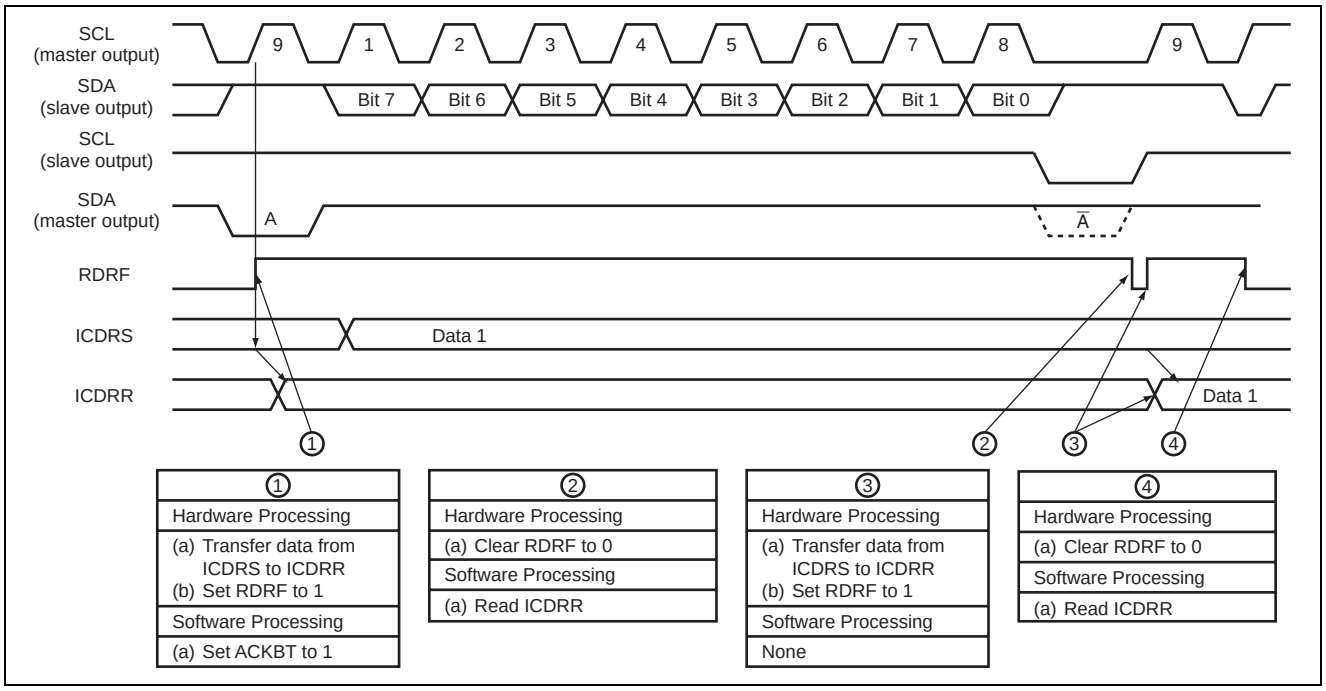


Figure 12 Slave Receive Mode Operation Timing 2

5. Description of Software (Master)

In this sample task I²C bus interface 2 module initialization, slave device and R/W setting, master transmit, and master receive operations are performed. The functions used by the master programs are described below.

5.1 Functions

Table 2 List of Master Program Functions

Function Name	Description
main	Controls master communication
IIC2_init	Initializes I²C2
set_slave_adrs	Selects slave device, selects R/W
master_trs	Master transmission
master_rcv	Master reception

5.2 Constants

Table 3 shows the constants used in this sample task.

Table 3 Constants

Label Name	Constant Value	Description	Used in
SLAVE_ADRS	H'00	Slave address	main
IIC_DATA_WRITE	H'00	Selects write as R/W option	main
IIC_DATA_READ	H'01	Selects read as R/W option	main
SIZE	4	Transmit/receive data size	master_trs master_rcv

5.3 RAM Usage

Table 4 shows the RAM used in this sample task.

Table 4 RAM Usage

Label Name	Description	Memory Consumption	Used in
m_trs[SIZE]	Buffer for storing transmit data	4 bytes	master_trs
m_rcv[SIZE]	Buffer for storing receive data	4 bytes	master_rcv

5.4 Modules

5.4.1 main() Function

1. Module Specifications

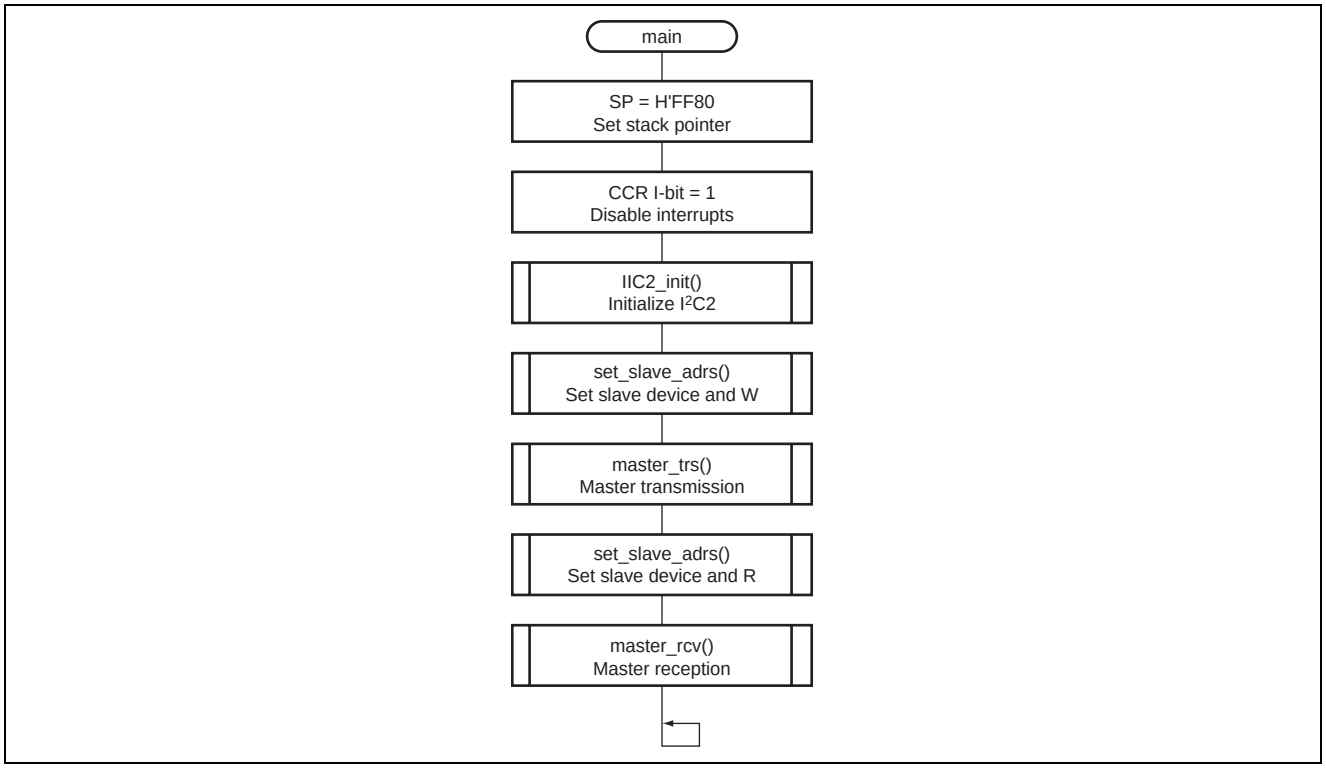
- Controls master communication

Table 5 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   None

3. Flowchart



5.4.2 IIC2_init() Function

1. Module Specifications

- Initializes I²C bus interface 2 module

Table 6 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
7	ICE	1	R/W	I²C bus interface 2 enable 0: The module is halted. (SCL and SDA pins are set to the port/serial function.) 1: The module is enabled for transfer operations. (SCL and SDA pins are bus-driven state.)
6	RCVD	0	R/W	Reception disable This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	0	R/W	Master/slave selection
4	TRS	0	R/W	Transmit/receive selection In the master mode with the I²C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode
3	CKS3	0	R/W	Transfer clock select 3 to 0 These bits are valid only in the master mode and should be set according to the necessary transfer clock frequency. In this sample task the operating frequency ϕ is 10 MHz. For details on the transfer clock frequency see table 7.
2	CKS2	0	R/W	
1	CKS1	0	R/W	
0	CKS0	1	R/W	

Table 7 Transfer Clock Frequency

Bit 3	Bit 2	Bit 1	Bit 0		Transfer Clock Frequency
CKS3	CKS2	CKS1	CKS0	Clock	ϕ = 10 MHz
0	0	0	1	ϕ/40	250 kHz

- ICCR2 I²C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
7	BBSY	0	R/W	Bus busy This bit functions both as a flag indicating whether the I²C bus is occupied or released and to issue start/stop conditions in the master mode. This bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. It is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Also follow this procedure when re-transmitting a start condition. Write 0 to BBSY and 0 to SCP to issue a stop condition. Use the MOV instruction to issue start/stop conditions.
6	SCP	1	R/W	Start/stop issue condition disable bit The SCP bit controls the issue of start/stop conditions in the master mode. This bit is always read as 1. If 1 is written to it, the value is not stored.
5	SDAO	1	R/W	SDA output value control This bit is used with SDAOP (bit 4) for modifying the output level of SDA. This bit should not be manipulated when a transfer is in progress. • When 0 is read, SDA pin outputs a low level • When 0 is written, SDA pin changes to low level output • When 1 is read, SDA pin outputs a high level • When 1 is written, SDA pin changes to Hi-Z output (high output by external pull-up resistor)
4	SDAOP	0	R/W	SDAO write protection This bit controls changes in the output level of the SDA pin by changing the SDAO bit value. To change the output level, use the MOV instruction to clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0. This bit is always read as 1.

- ICMR I²C bus mode register Address: H'F07A

Bit	Bit Name	Set Value	R/W	Description
7	MLS	0	R/W	MSB-first/LSB-first selection 0: MSB-first 1: LSB-first Clear this bit to 0 when the I²C bus format is used.
6	WAIT	0	R/W	Wait insertion bit In the master mode with the I²C bus format, the WAIT bit selects whether or not to insert a wait cycle after transferring data other than the acknowledge bit. 1: Low period extended for two transfer clock cycles after the falling edge of the clock for the final data bit 0: Data and acknowledge bits transferred consecutively with no wait cycles inserted
3	BCWP	1	R/W	BC write protection This bit controls writes to bits BC2 to BC0. To modify BC2 to BC0 clear this bit to 0 and use the MOV instruction. • When 0 is written, values of BC2 to BC0 are set • When read, 1 is always read • When 1 is written, settings of BC2 to BC0 are invalid
2	BC2	0	R/W	Bit counter 2 to 0 These bits specify the number of data bits to be transferred next. When read, the remaining number of transfer bits is indicated. In the I²C bus format an acknowledge bit is added to the data transferred. Bits BC2 to BC0 should be set during an interval between transfer frames. Furthermore, if bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL signal is low. The value of bits BC2 to BC0 returns to 000 at the end of a data transfer including the acknowledge bit. 000: 9 bits 001: 2 bits 010: 3 bits 011: 4 bits 100: 5 bits 101: 6 bits 110: 7 bits 111: 8 bits
1	BC1	0	R/W	
0	BC0	0	R/W	

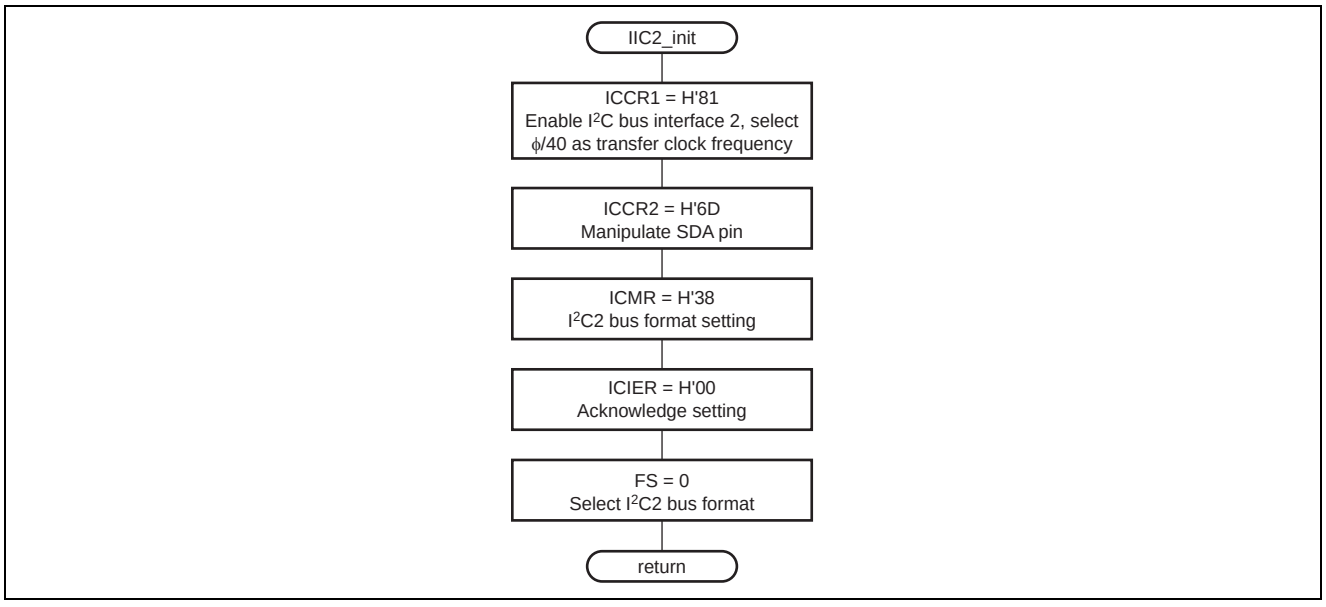
- ICIER I²C bus interrupt enable register Address: H'F07B

Bit	Bit Name	Set Value	R/W	Description
2	ACKE	0	R/W	Acknowledge bit judgment selection 0: The value of the receive acknowledge bit is ignored, and transfer continues. 1: If the receive acknowledge bit is 1, transfer is halted.
0	ACKBT	0	R/W	Transmit acknowledge In the receive mode, this bit specifies the bit to be sent at the acknowledge timing. 0: 0 sent at acknowledge timing 1: 1 sent at acknowledge timing

- SAR Slave address register Address: H'F07D

Bit	Bit Name	Set Value	R/W	Description
0	FS	0	R/W	Format selection 0: I²C bus format selected 1: Clock-synchronous serial format selected

3. Flowchart



5.4.3 set_slave_adrs() Function

1. Module Specifications

- Selects slave device
- Selects R/W

Table 8 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char	slv_adrs	Slave address
Arguments	unsigned char	write_read	Read or write setting

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
5	MST	1	R/W	Master/slave selection
4	TRS	1	R/W	Transmit/receive selection In the master mode with the I²C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

- ICCR2 I²C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
7	BBSY	1	R/W	Bus busy This bit functions both as a flag indicating whether the I²C bus is occupied or released and to issue start/stop conditions in the master mode. This bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. It is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Also follow this procedure when re-transmitting a start condition. Write 0 to BBSY and 0 to SCP to issue a stop condition. Use the MOV instruction to issue start/stop conditions.
6	SCP	0	R/W	Start/stop issue condition disable bit The SCP bit controls the issue of start/stop conditions in the master mode. This bit is always read as 1. If 1 is written to it, the value is not stored.

- ICIER I²C bus interrupt enable register Address: H'F07B

Bit	Bit Name	Set Value	R/W	Description
1	ACKBR	0	R	Receive acknowledge In the transmit mode, this bit stores the contents of the acknowledge bit received from the receive device. This bit cannot be written to. 0: Receive acknowledge = 0 1: Receive acknowledge = 1

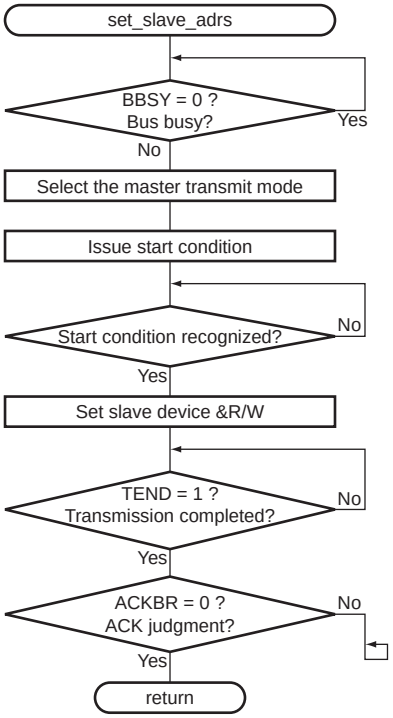
- ICSR I²C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 • When a start condition (including re-transfer) has been issued [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
6	TEND	Undefined	R/W	Transmit end [Setting condition] • When the rising edge of the ninth clock cycle of SCL is detected while the value of TDRE is 1 [Clearing conditions] • When 0 is written to TEND after it was read as 1 • When data is written to ICDRT with an instruction

- ICDRT I²C bus transmit data register Address: H'F07E

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R/W	I²C bus transmit data register ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the I²C bus shift register (ICDRS) it transfers the transmit data which has been written to ICDRT to ICDRS and starts transferring data. Continuous transfer is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. The initial value of ICDRT is H'FF.
6	Bit 6	Undefined	R/W	
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

3. Flowchart


set_slave_adrs
BBSY = 0 ?
Bus busy?
Yes
No
Select the master transmit mode
Issue start condition
Start condition recognized?
No
Yes
Set slave device &R/W
TEND = 1 ?
Transmission completed?
No
Yes
ACKBR = 0 ?
ACK judgment?
No
Yes
return

5.4.4 master_trs() Function

1. Module Specifications

- Master transmit

Table 9 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
5	MST	1	R/W	Master/slave selection
4	TRS	1	R/W	Transmit/receive selection In the master mode with the I²C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

- ICCR2 I²C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
7	BBSY	1	R/W	Bus busy This bit functions both as a flag indicating whether the I²C bus is occupied or released and to issue start/stop conditions in the master mode. This bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. It is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Also follow this procedure when re-transmitting a start condition. Write 0 to BBSY and 0 to SCP to issue a stop condition. Use the MOV instruction to issue start/stop conditions.
6	SCP	0	R/W	Start/stop issue condition disable bit The SCP bit controls the issue of start/stop conditions in the master mode. This bit is always read as 1. If 1 is written to it, the value is not stored.

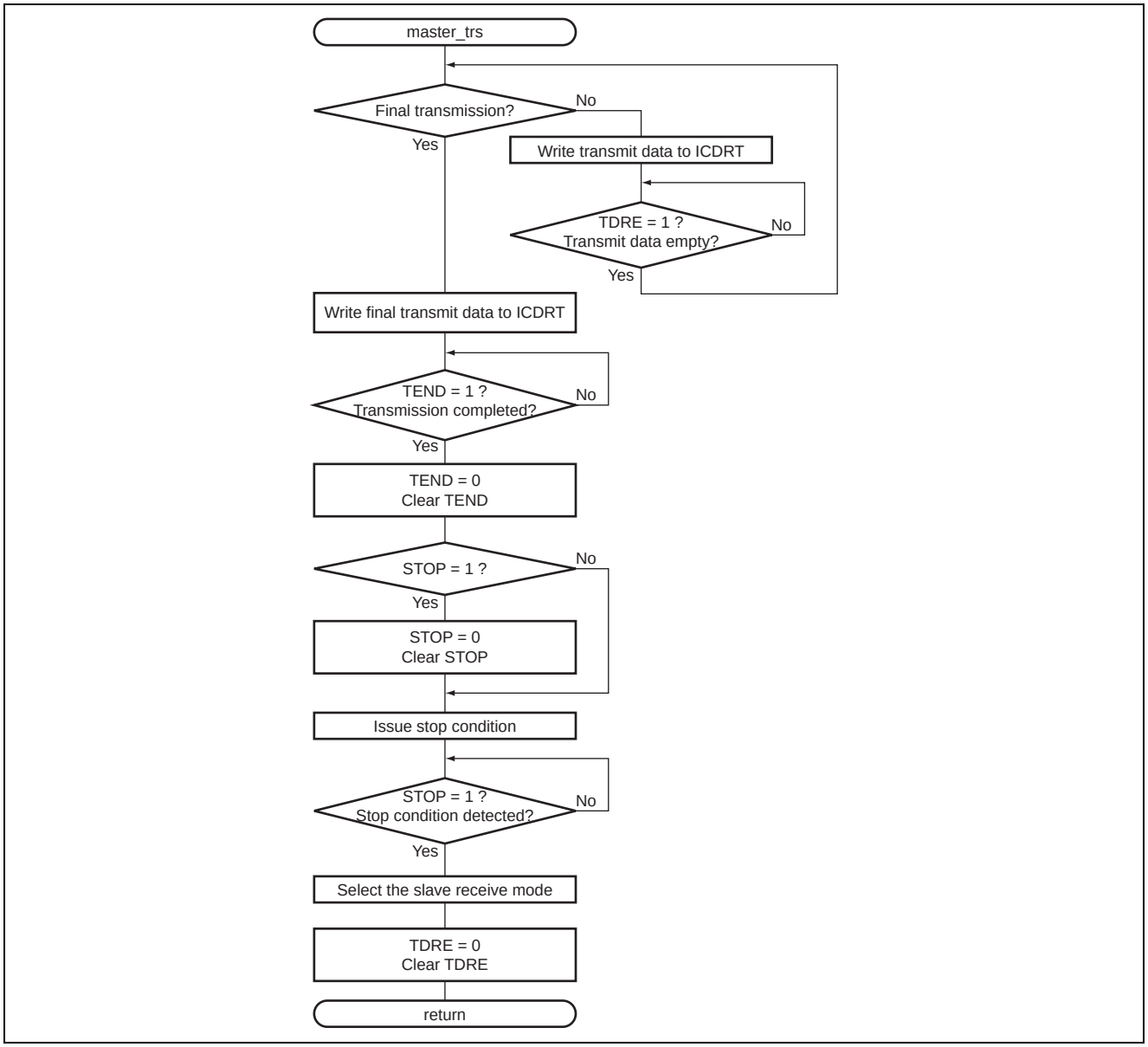
- ICSR I²C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 • When a start condition (including re-transfer) has been issued [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
6	TEND	Undefined	R/W	Transmit end [Setting condition] • When the rising edge of the ninth clock cycle of SCL is detected while the value of TDRE is 1 [Clearing conditions] • When 0 is written in TEND after it was read as 1 • When data is written to ICDRT with an instruction
3	STOP	Undefined	R/W	Stop condition detection flag [Setting condition] • When a stop condition is detected after frame transfer [Clearing condition] • When 0 is written to STOP after it was read as 1

- ICDRT I²C bus transmit data register Address: H'F07E

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R/W	I²C bus transmit data register ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the I²C bus shift register (ICDRS) it transfers the transmit data which has been written to ICDRT to ICDRS and starts transferring data. Continuous transfer is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. The initial value of ICDRT is H'FF.
6	Bit 6	Undefined	R/W	
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

3. Flowchart


master_trs
Final transmission?
No
Yes
Write transmit data to ICDRT
TDRE = 1 ?
Transmit data empty?
No
Yes
Write final transmit data to ICDRT
TEND = 1 ?
Transmission completed?
No
Yes
TEND = 0
Clear TEND
STOP = 1 ?
No
Yes
STOP = 0
Clear STOP
Issue stop condition
STOP = 1 ?
Stop condition detected?
No
Yes
Select the slave receive mode
TDRE = 0
Clear TDRE
return

5.4.5 master_rcv() Function

1. Module Specifications

- Master receive operation

Table 10 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
6	RCVD	0	R/W	Reception disabled This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	1	R/W	Master/slave selection
4	TRS	0	R/W	Transmit/receive selection In the master mode with the I²C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

- ICCR2 I²C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
7	BBSY	1	R/W	Bus busy This bit functions both as a flag indicating whether the I²C bus is occupied or released and to issue start/stop conditions in the master mode. This bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. It is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Also follow this procedure when re-transmitting a start condition. Write 0 to BBSY and 0 to SCP to issue a stop condition. Use the MOV instruction to issue start/stop conditions.
6	SCP	0	R/W	Start/stop issue condition disable bit The SCP bit controls the issue of start/stop conditions in the master mode. This bit is always read as 1. If 1 is written to it the value is not stored.

- ICSR I²C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 • When a start condition (including re-transfer) has been issued [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
6	TEND	Undefined	R/W	Transmit end [Setting condition] • When the rising edge of the ninth clock cycle of SCL is detected while the value of TDRE is 1 [Clearing conditions] • When 0 is written in TEND after it was read as 1 • When data is written to ICDRT with an instruction
5	RDRF	Undefined	R/W	Receive data register full [Setting condition] • When receive data is transferred from ICDRS to ICDRR [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When ICDRR is read with an instruction
3	STOP	Undefined	R/W	Stop condition detection flag [Setting condition] • When a stop condition is detected after a frame transfer [Clearing condition] • When 0 is written to STOP after it was read as 1

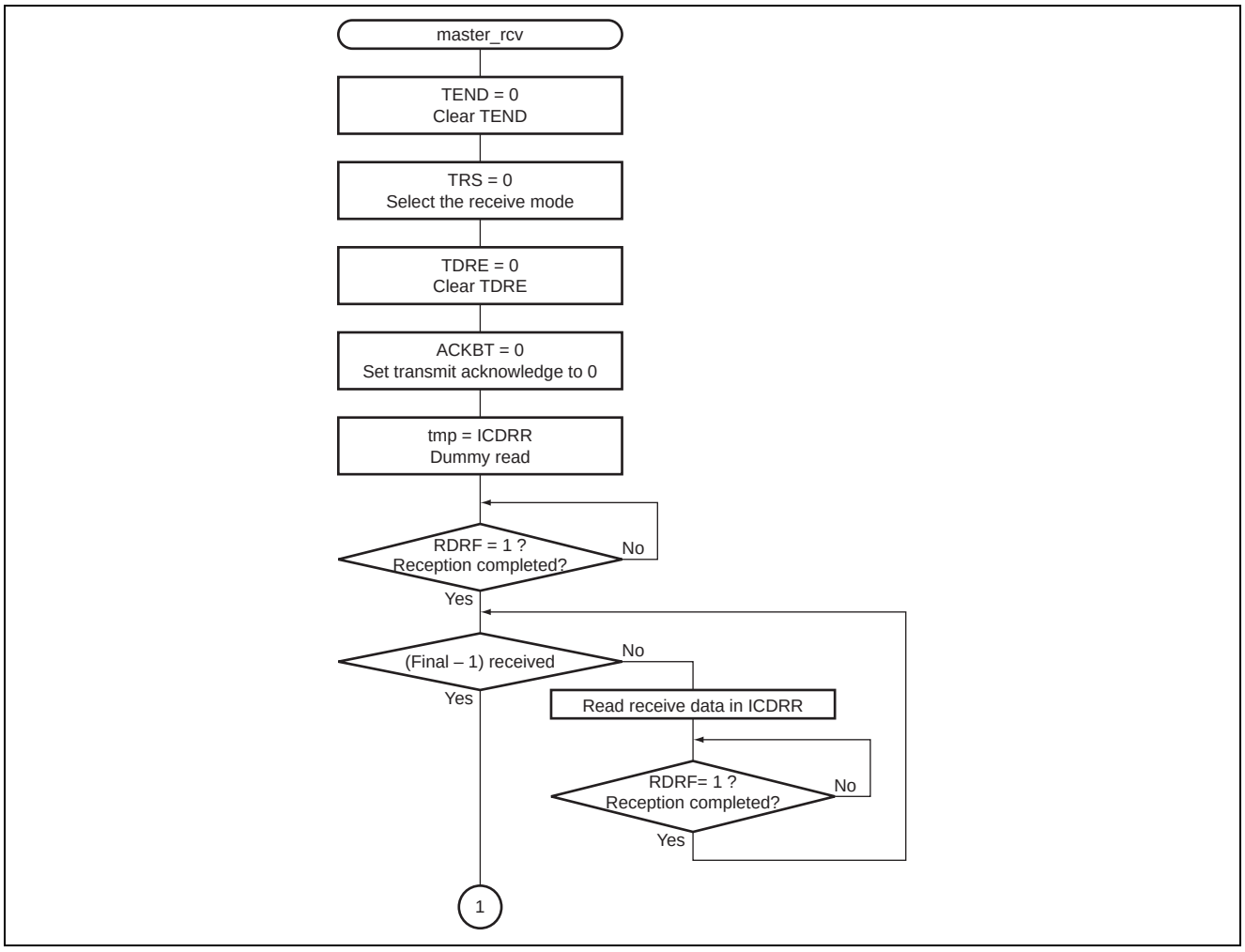
- ICIER I²C bus interrupt enable register Address: H'F07B

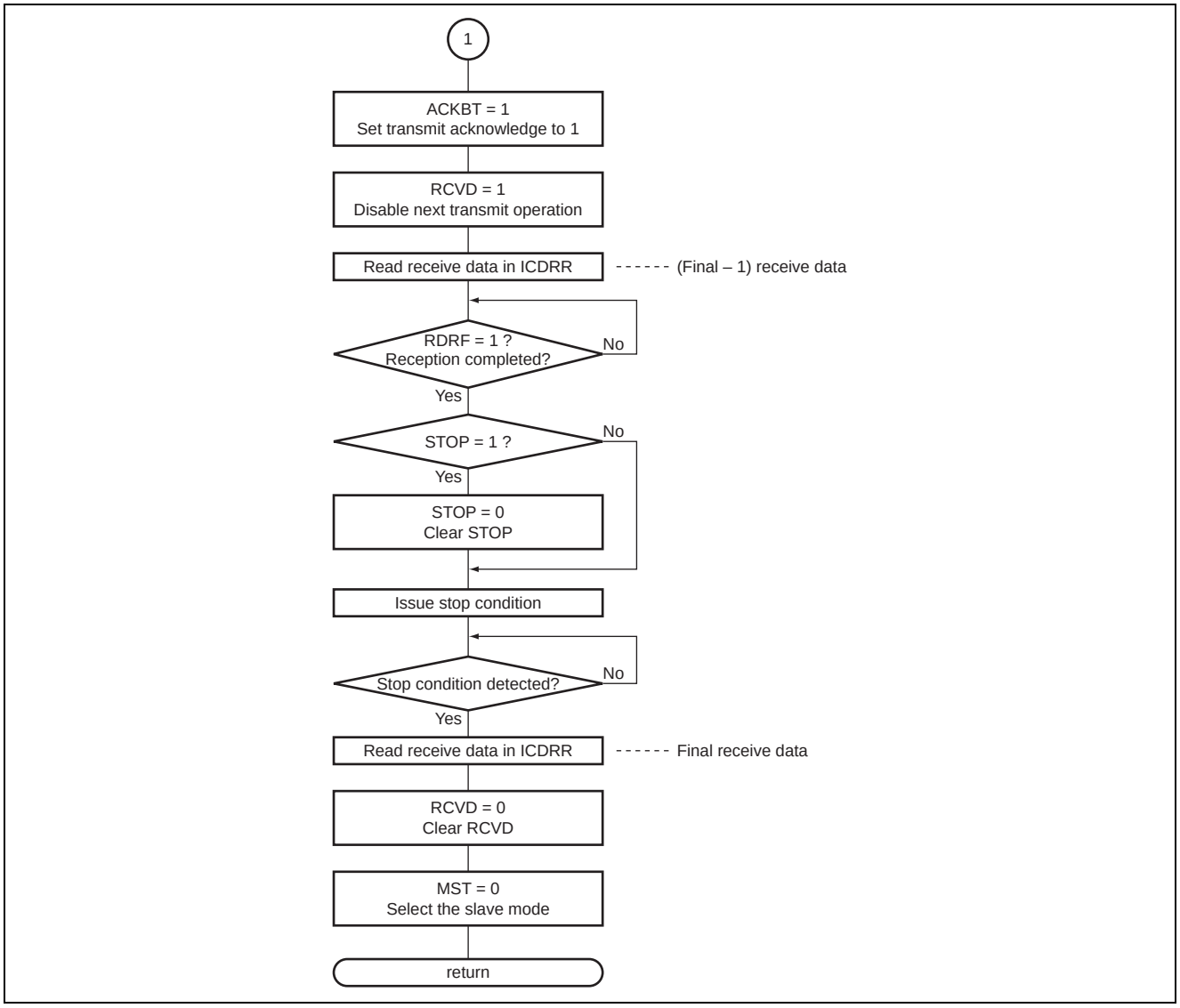
Bit	Bit Name	Set Value	R/W	Description
0	ACKBT	0	R/W	Transmit acknowledge In the receive mode, this bit specifies the bit to be sent at the acknowledge timing. 0: 0 sent at acknowledge timing 1: 1 sent at acknowledge timing

- ICDRR I²C bus receive data register Address: H'F07F

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R	I²C bus receive data register
6	Bit 6	Undefined	R	ICDRR is an 8-bit register that stores receive data. After one byte of data is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, so the CPU cannot write to it. The initial value of ICDRR is H'FF.
5	Bit 5	Undefined	R	
4	Bit 4	Undefined	R	
3	Bit 3	Undefined	R	
2	Bit 2	Undefined	R	
1	Bit 1	Undefined	R	
0	Bit 0	Undefined	R	

3. Flowchart





5.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
D, B	H'F780

6. Description of Software (Slave)

In this sample task I²C bus interface 2 module initialization, slave receive, and slave transmit operations are performed. The functions used by the slave program are described below.

6.1 Functions

Table 11 List of Slave Program Functions

Function Name	Description
main	Controls slave communication
IIC2_init	Initializes I²C2 module
slave_rcv	Slave receive operation
slave_trs	Slave transmit operation

6.2 Constants

Table 12 shows the constants used in this sample task.

Table 12 Constants

Label Name	Constant Value	Description	Used in
SIZE	4	Transmit/receive data size	slave_trs slave_rcv

6.3 RAM Usage

Table 13 shows the RAM used in this sample task.

Table 13 RAM Usage

Label Name	Description	Memory Consumption	Used in
s_data[SIZE]	Buffer for storing ransmit/receive data	4 bytes	slave_trs slave_rcv

6.4 Modules

6.4.1 main() Function

1. Module Specifications

- Controls slave communication

Table 14 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

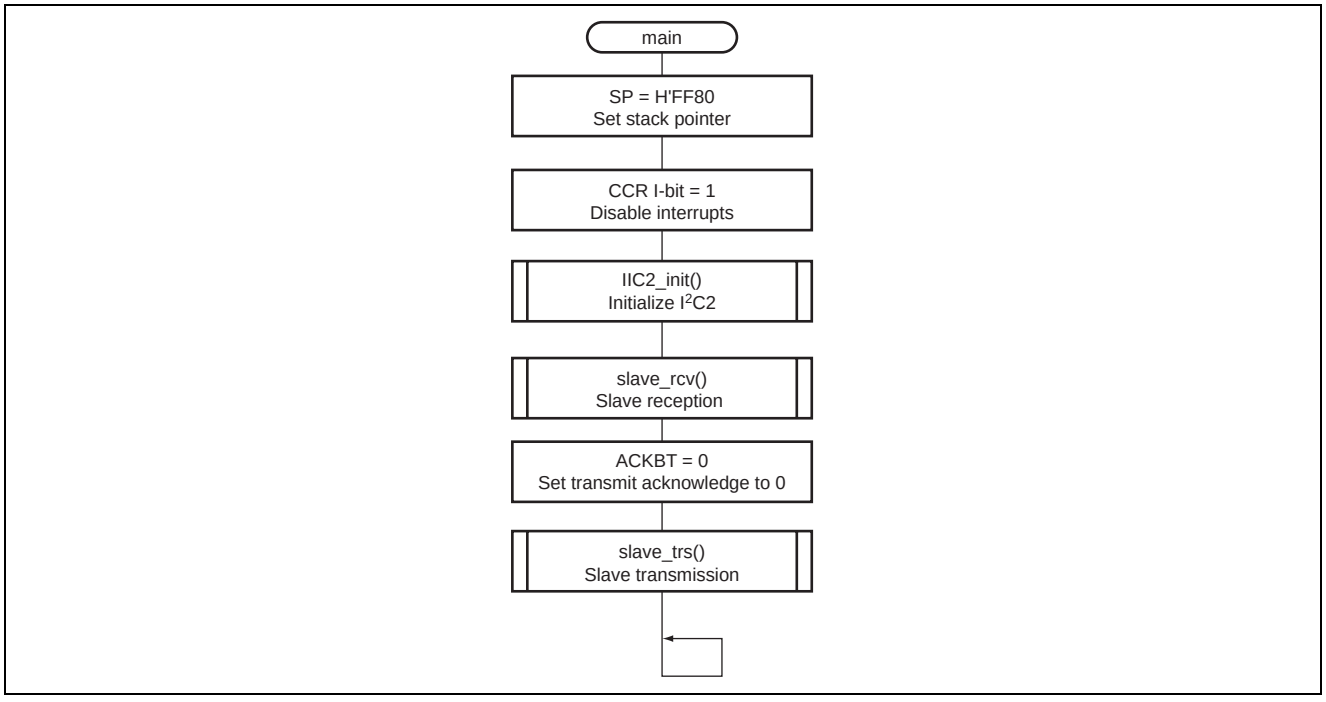
2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICIER I²C bus interrupt enable register Address: H'F07B

Bit	Bit Name	Set Value	R/W	Description
0	ACKBT	0	R/W	Transmit acknowledge In the receive mode, this bit specifies the bit to be sent at the acknowledge timing. 0: 0 sent at acknowledge timing 1: 1 sent at acknowledge timing

3. Flowchart



6.4.2 IIC2_init() Function

1. Module Specifications

- Initializes I²C bus interface 2 module

Table 15 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
7	ICE	1	R/W	I²C bus interface 2 enable 0: The module is halted. (SCL and SDA pins are set to the port/serial function.) 1: The module is enabled for transfer operations. (SCL and SDA pins are bus-driven state.)
6	RCVD	0	R/W	Reception disabled This bit enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception
5	MST	0	R/W	Master/slave selection
4	TRS	0	R/W	Transmit/receive selection In the master mode with the I²C bus format, MST and TRS are both reset by hardware when arbitration is lost, causing a transition to the slave receive mode. The value of the TRS bit should be changed between transfer frames. The following operation modes can be selected by the MST and TRS bits in combination. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode

- ICCR2 I²C bus control register 2 Address: H'F079

Bit	Bit Name	Set Value	R/W	Description
5	SDAO	1	R/W	SDA output value control This bit is used with SDAOP (bit 4) for modifying the output level of SDA. This bit should not be manipulated when a transfer is in progress. • When 0 is read, SDA pin outputs a low level • When 0 is written, SDA pin changes to low level output • When 1 is read, SDA pin outputs a high level • When 1 is written, SDA pin changes to Hi-Z output (high output by external pull-up resistor)
4	SDAOP	0	R/W	SDAO write protection This bit controls changes in the output level of the SDA pin by modifying the SDAO bit. To change the output level, use the MOV instruction to clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0. This bit is always read as 1.

- ICMR I²C bus mode register Address: H'F07A

Bit	Bit Name	Set Value	R/W	Description
7	MLS	0	R/W	MSB-first/LSB-first selection 0: MSB-first 1: LSB-first Clear this bit to 0 when the I²C bus format is used.
3	BCWP	1	R/W	BC write protection This bit controls writes to bits BC2 to BC0. To modify BC2 to BC0 clear this bit to 0 and use the MOV instruction. • When 0 is written, values of BC2 to BC0 are set • When read, 1 is always read • When 1 is written, settings of BC2 to BC0 are invalid
2	BC2	0	R/W	Bit counter 2 to 0 These bits specify the number of data bits to be transferred next. When read, the remaining number of transfer bits is indicated. In the I²C bus format an acknowledge bit is added to the data transferred. Bits BC2 to BC0 should be set during an interval between transfer frames. Furthermore, if bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL signal is low. The value of bits BC2 to BC0 returns to 000 at the end of a data transfer including the acknowledge bit. 000: 9 bits 001: 2 bits 010: 3 bits 011: 4 bits 100: 5 bits 101: 6 bits 110: 7 bits 111: 8 bits
1	BC1	0	R/W	
0	BC0	0	R/W	

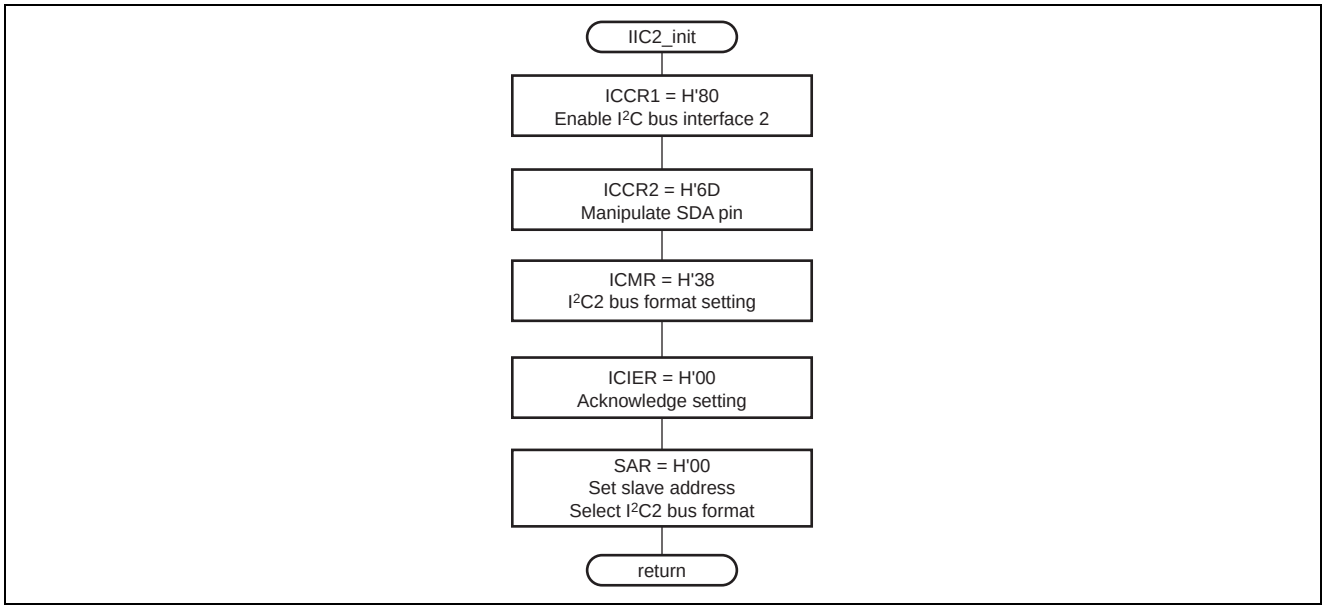
- ICIER I²C bus interrupt enable register Address: H'F07B

Bit	Bit Name	Set Value	R/W	Description
2	ACKE	0	R/W	Acknowledge bit judgment selection 0: The value of the receive acknowledge bit is ignored, and transfer continues. 1: If the receive acknowledge bit is 1, transfer is halted.
0	ACKBT	0	R/W	Transmit acknowledge In the receive mode, this bit specifies the bit to be sent at the acknowledge timing. 0: 0 sent at acknowledge timing 1: 1 sent at acknowledge timing

- SAR Slave address register Address: H'F07D

Bit	Bit Name	Set Value	R/W	Description
7 to 1	SVA6 to SVA0	All 0	R/W	Slave address 6 to 0 These bits set a unique address differing from the addresses of other slave devices connected to the I²C bus.
0	FS	0	R/W	Format select 0: I²C bus format selected 1: Clock-synchronous serial format selected

3. Flowchart



6.4.3 slave_rcv() Function

1. Module Specifications

- Slave receive operation

Table 16 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICIER I²C bus interrupt enable register Address: H'F07B

Bit	Bit Name	Set Value	R/W	Description
0	ACKBT	0	R/W	Transmit acknowledge In the receive mode, this bit specifies the bit to be sent at the acknowledge timing. 0: 0 sent at acknowledge timing 1: 1 sent at acknowledge timing

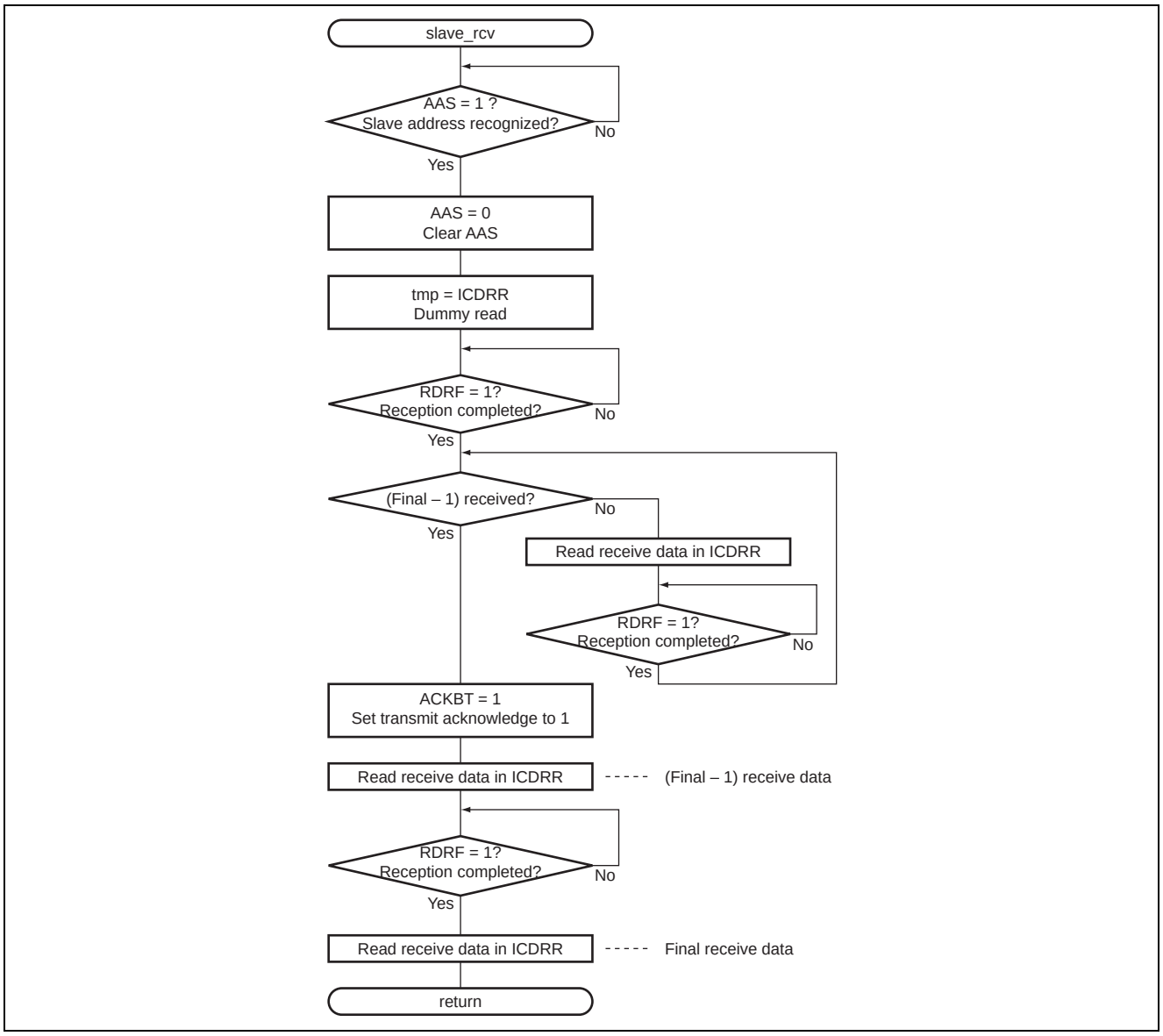
- ICSR I²C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
5	RDRF	Undefined	R/W	Receive data register full [Setting condition] • When receive data is transferred from ICDRS to ICDRR [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When ICDRR is read with an instruction
1	AAS	0	R/W	Slave address recognition flag In the slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR. [Setting condition] • When the slave address is detected in the slave receive mode [Clearing condition] • When 0 is written to AAS after it was read as 1

- ICDRR I²C bus receive data register Address: H'F07F

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R	I²C bus receive data register
6	Bit 6	Undefined	R	ICDRR is an 8-bit register that stores receive data. After one byte of data is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, so the CPU cannot write to it. The initial value of ICDRR is H'FF.
5	Bit 5	Undefined	R	
4	Bit 4	Undefined	R	
3	Bit 3	Undefined	R	
2	Bit 2	Undefined	R	
1	Bit 1	Undefined	R	
0	Bit 0	Undefined	R	

3. Flowchart



6.4.4 slave_trs() Function

1. Module Specifications

- Slave transmit operation

Table 17 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- ICCR1 I²C bus control register 1 Address: H'F078

Bit	Bit Name	Set Value	R/W	Description
4	TRS	1	R/W	Transmit/receive selection When the slave address is matched on first frame after a start condition is detected, and the eighth data bit (R/W) is 1, TRS is set to 1. 0: Receive mode 1: Transmit mode

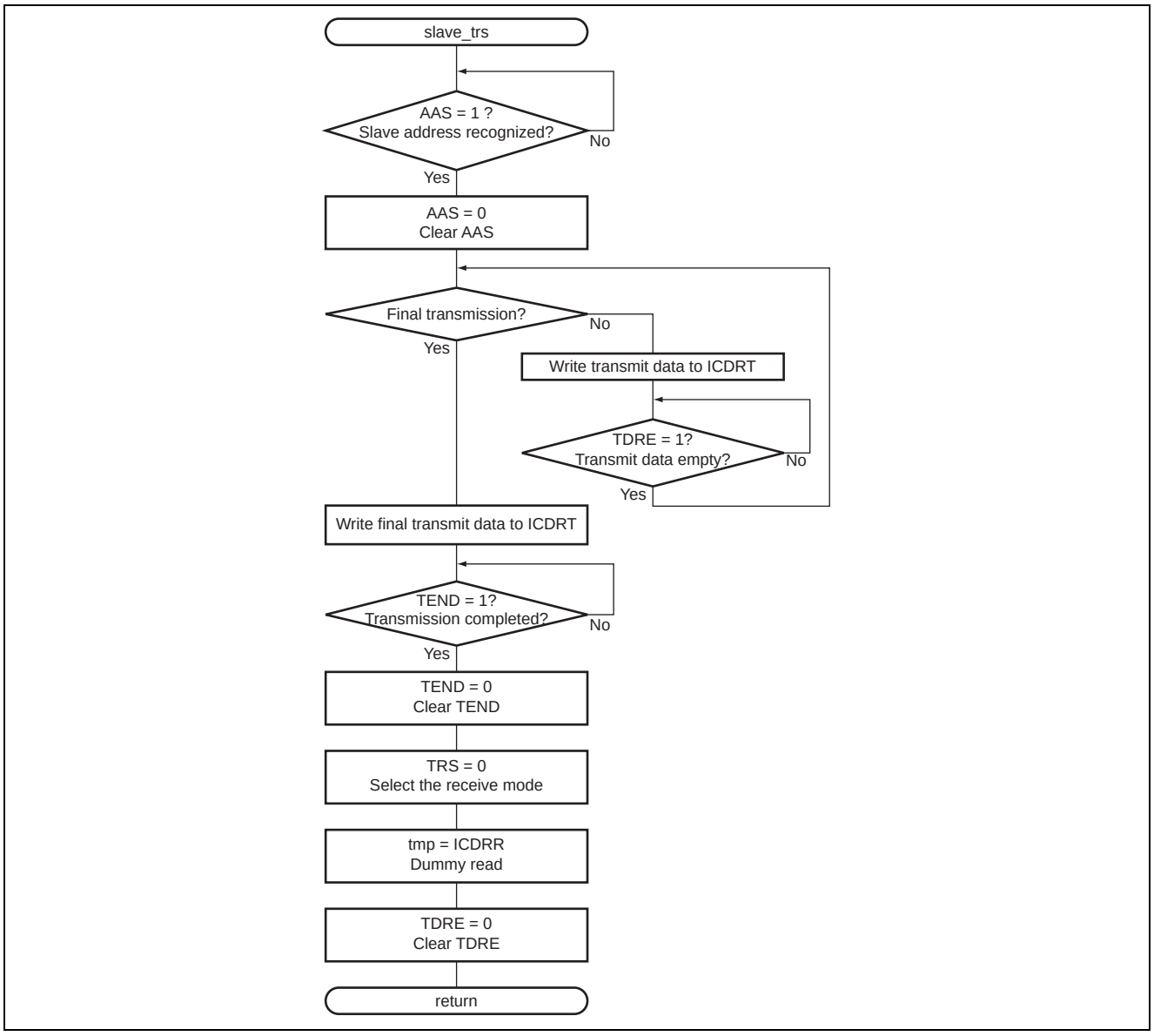
- ICSR I²C bus status register Address: H'F07C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/W	Transmit data register empty [Setting conditions] • When data is transferred from ICDRT to ICDRS and ICDRT becomes empty • When the TRS bit is set to 1 [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When data is written to ICDRT with an instruction
6	TEND	Undefined	R/W	Transmit end [Setting condition] • When the rising edge of the ninth clock cycle of SCL is detected while the value of TDRE is 1 [Clearing conditions] • When 0 is written in TEND after it was read as 1 • When data is written to ICDRT with an instruction
1	AAS	0	R/W	Slave address recognition flag In the slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR. [Setting condition] • When the slave address is detected in the slave receive mode [Clearing condition] • When 0 is written to AAS after it was read as 1

- ICDRT I²C bus transmit data register Address: H'F07E

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R/W	I²C bus transmit data register
6	Bit 6	Undefined	R/W	ICDRT is an 8-bit readable/writable register that stores transmit data. When ICDRT detects space in the I²C bus shift register (ICDRS) it transfers the transmit data which was written to ICDRT to ICDRS and starts transferring data. Continuous transfer is possible if the next transmit data is written to ICDRT while data transfer to ICDRS is in progress. The initial value of ICDRT is H'FF.
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

3. Flowchart



6.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

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