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April 1st, 2010
Renesas Electronics Corporation

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H8/36912, H8/36902 Groups

On-Chip Oscillator Trimming

Introduction

The timer W input capture function is used to trim the on-chip oscillator of the H8/36912.

Target Device

H8/36912

Contents

1. Specifications 2
2. Functions Used 3
3. Principles of Operation 6
4. Description of Software 8
5. Flowcharts 14

1. Specifications

The timer W input capture function is used to trim the on-chip oscillator of the H8/36912. An illustration of procedure for trimming the on-chip oscillator used in this sample task is shown in figure 1.

Data to be set in the RC trimming data register (RCTRMDR) is calculated based on the external reference clock input to timer W input capture A (the FTIOA pin).

In this sample task the frequency of the reference clock input to the FTIOA pin is 100 kHz and the on-chip oscillation frequency is trimmed to 9 MHz. Furthermore, the clock generated by the on-chip oscillator is output from pin PC1 for operation checking. Note that the on-chip oscillation frequency is trimmed to within an error range of 5%.

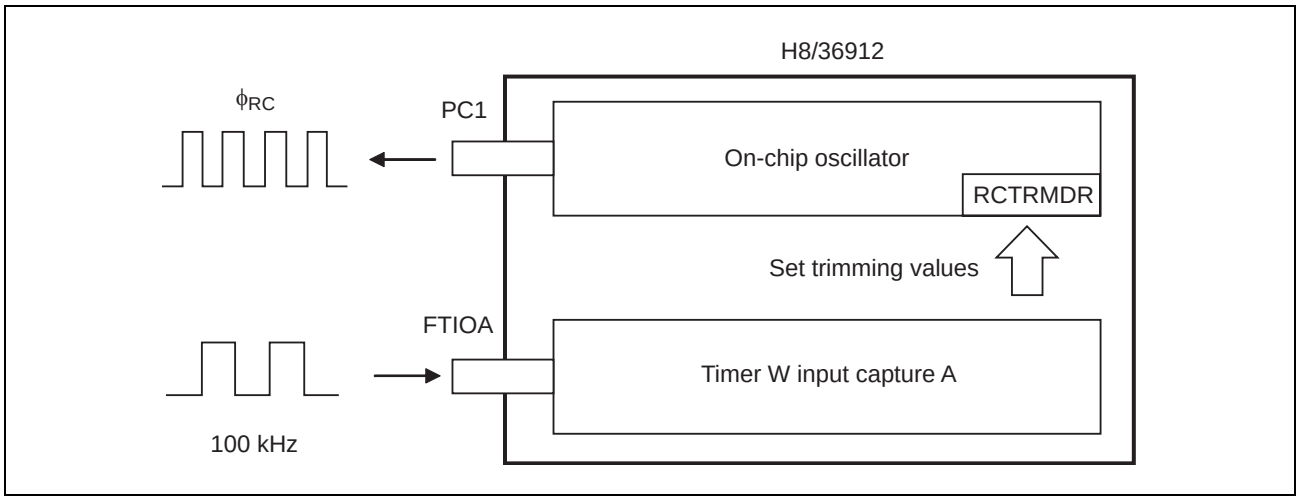


Figure 1 On-Chip Oscillator Trimming

2. Functions Used

2.1 Functions

In this sample task, trimming of the on-chip oscillator is performed. A block diagram of the timer W input capture and trimming operation is shown in figure 2. A description of the functions used in the sample task is provided below.

- On-chip oscillator functions
  - — Clock control/status register (CKCSR)

    Selects the port C function, controls switching the system clocks, and indicates the system clock state.
  - — RC trimming data protect register (RCTRMDPR)

    Controls RCTRMDPR itself and writing to RCTRMDR. Use the MOV instruction to rewrite this register. Bit manipulation instructions cannot be used to change the settings.
  - — RC trimming data register (RCTRMDR)

    Stores the trimming data for the on-chip oscillator frequency.

- Timer W functions
  - — Timer mode register W (TMRW)

    Selects the general register functions and the timer output mode.
  - — Timer control register W (TCRW)

    Selects the TCNT counter clock source, selects a clearing condition, and specifies the timer output levels.
  - — Timer status register W (TSRW)

    Shows the status of interrupt requests.
  - — Timer I/O control register 0 (TIOR0)

    Selects the functions of GRA and GRB, and specifies the functions of the FTIOA and FTIOB pins.
  - — Timer counter (TCNT)

    A 16-bit readable/writable up-counter. TCNT must always be read or written to in 16-bit units; 8-bit access is not allowed. The initial value of TCNT is H'0000.
  - — General registers A and C (GRA and CRC)

    Each general register is a 16-bit readable/writable register that can function as either an output compare register or an input capture register. Also, GRC can be used as a buffer register for GRA.

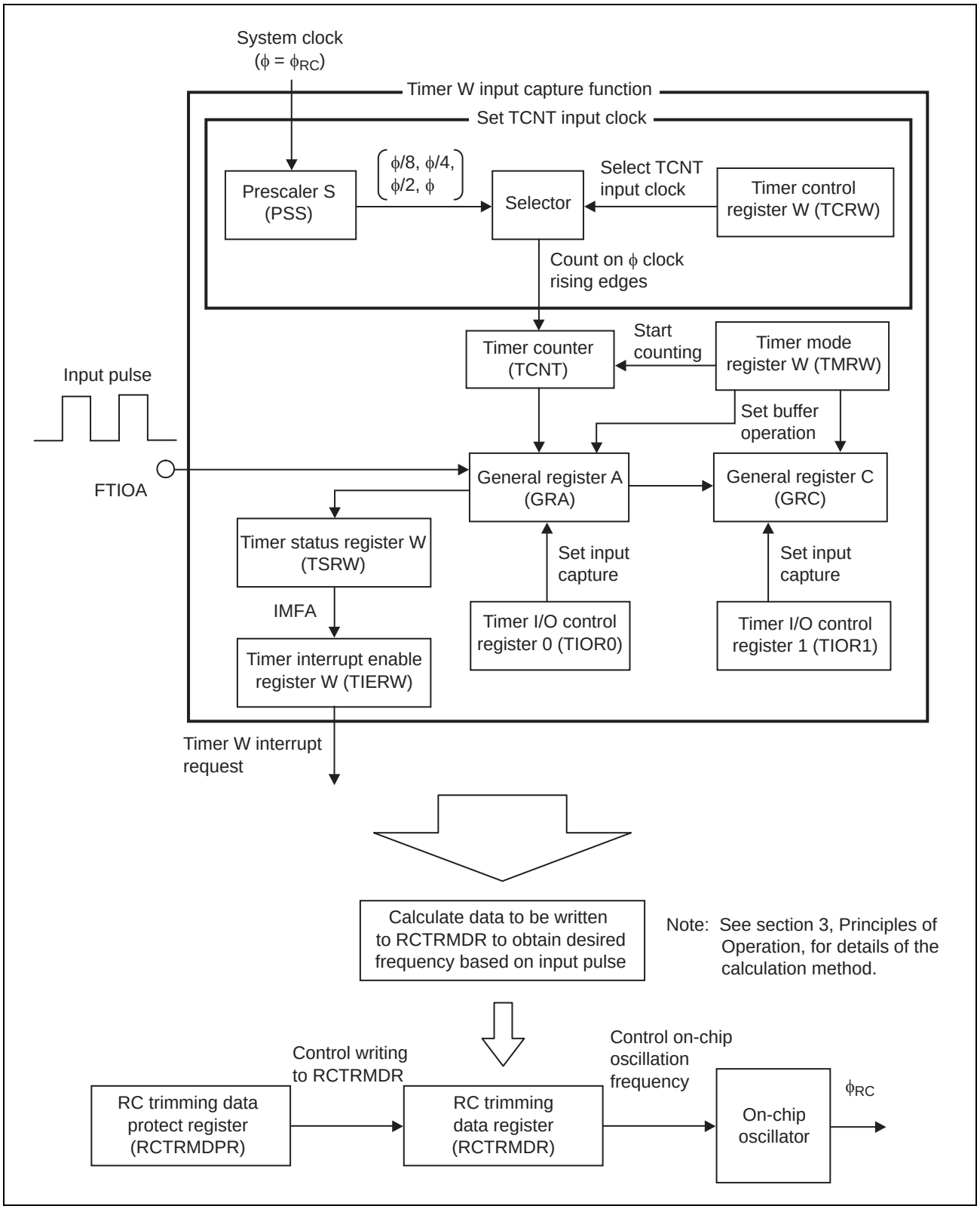


Figure 2 Block Diagram of Timer W Input Capture and Trimming

2.2 Assignment of Functions

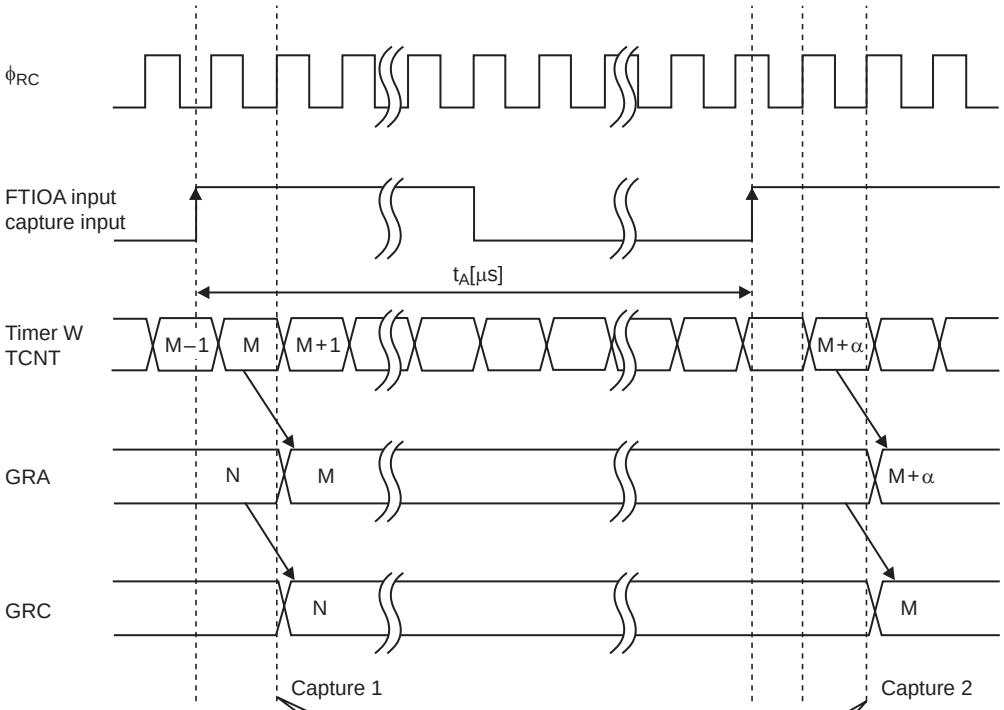
Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, trimming of the on-chip oscillator is performed.

Table 1 Assignment of Functions

Elements	Description
CKCSR	Controls on-chip oscillator clock output
TMRW	Controls the timer counter, sets GRC as buffer register for GRA
TCRW	Sets ϕ as the TCNT counter clock source
TIERW	Enables input capture A interrupts
TSRW	Input capture A interrupt request flag
TIOR0	Specifies that input capture to GRA is performed at rising edge of FTIOA pin
TIOR1	Sets GRC to the GRA buffer function
TCNT	16-bit counter that counts rising edges of ϕ
GRA	TCNT value is transferred at GRA input capture
GRC	GRA value is sent to buffer register GRC at GRA input capture
TCSRWD	Stops the watchdog timer operation

3. Principles of Operation

Trimming of the on-chip oscillator is performed by using the timer W input capture function to input an external reference pulse. Using the hardware and software processing shown in figures 3 and 4 the on-chip oscillator is trimmed.



Hardware Processing
(1) Stop TCNT (2) Start TCNT count operation
Software Processing
Initial settings (1) Stop WDT operation (2) Stop TCNT operation (3) Set input capture function (4) Set GRC to GRA buffer function (5) Clear cnt to 0 (6) Start TCNT count operation (7) Enable interrupts

Hardware Processing
(1) Transfer GRA value to GRC (2) Transfer TCNT counter value to GRA (3) Set IMFA to 1
Software Processing
(1) Start interrupt processing based on IMFA flag (2) Clear IMFA to 0 (3) Increment cnt

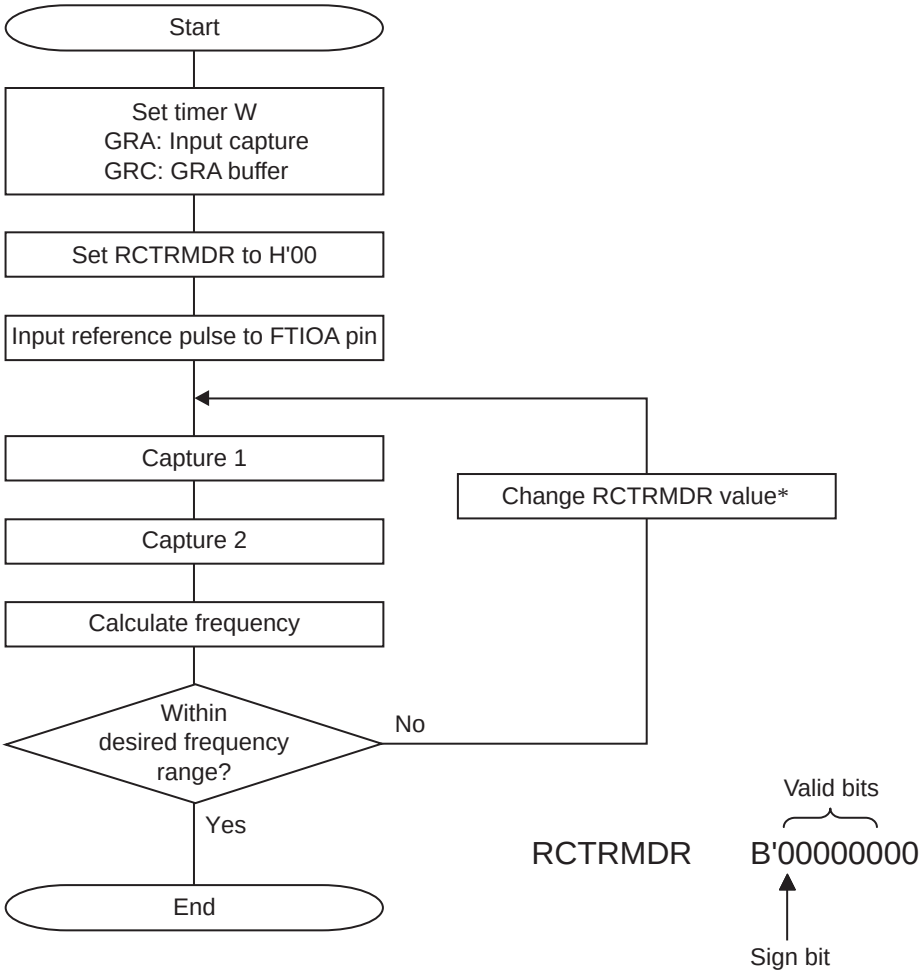
Hardware Processing
(1) Transfer GRA value to GRC (2) Transfer TCNT counter value to GRA (3) Set IMFA to 1
Software Processing
(1) Start interrupt processing based on IMFA flag (2) Clear IMFA to 0 (3) Clear IMIEA to 0 (4) Increment cnt

The equation shown below can be used to obtain the oscillation frequency of the on-chip oscillator.
Since the input capture input is sampled at ϕ_{RC} the calculated value has a sampling error of ±1 clock (ϕ_{RC}).

$$\phi_{RC} = \{(M + \alpha) - M\} / t_A \quad [MHz]$$

ϕ_{RC}: Oscillation frequency of on-chip oscillator [MHz]
t_A: Reference clock frequency [µs]
M: Timer W counter value (M < TCNT)

Figure 3 Principles of Operation 1



Note: * Compare the measured frequency to the desired frequency to determine if it is higher or lower, then decide the value of RCTRMDR one bit at a time, starting from the MSB. This sample task uses the setting method shown below. However, trimming is not possible if ϕ_{RC} is higher than the desired frequency when the sign bit is set to 1, because the frequency is already at its minimum value (H'80). Also, trimming is not possible if the frequency is not within the desired range after setting all the valid bits to 1.

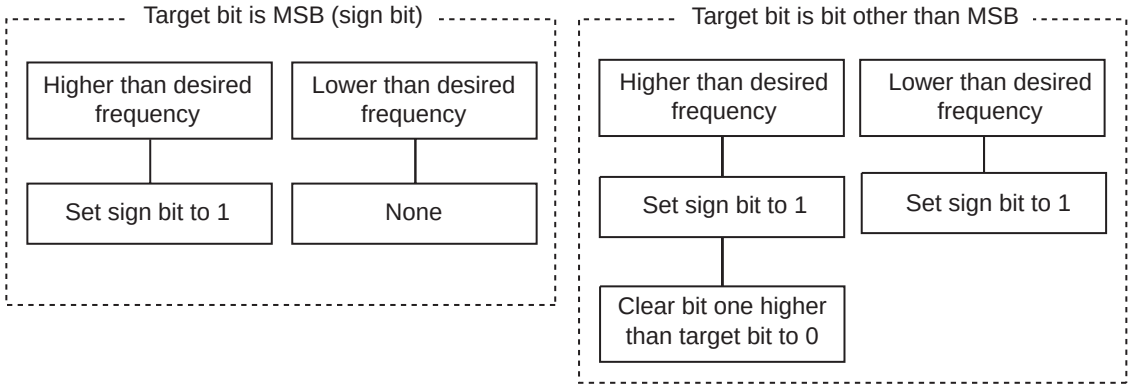


Figure 4 Principles of Operation 2

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Module Name	Description
main	Stops the watchdog timer operation, controls the RC trimming data register, outputs the on-chip oscillator clock, sets input capture, controls TCNT, and controls interrupts
twint	Handles input capture interrupts, clears IMFA, disable input capture interrupts, and increments cnt
trimming	Calculates the measured frequency, rewrites RCTRMDR, and increments tr_cnt
labs	Standard function included in stdlib.h. Calculates absolute values using long-type data as arguments, and returns the result as long-type data

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- CKCSR Clock control/status register Address: H'F734

Bit	Bit Name	Set Value	R/W	Description
7	PMRC1	1	R/W	Port C function select bits 1 and 0
6	PMRC0	0	R/W	

PMRC1	PMRC0	PC1	PC0
0	0	I/O	I/O
1	0	CLKOUT	I/O
0	1	I/O	OSC1 (external clock input)
1	1	OSC2	OSC1

- RCTRMDPR RC trimming data protect register Address: H'F736

Bit	Bit Name	Set Value	R/W	Description
7	WRI	0	W	Write inhibit Writes to this register are valid only when 0 is written to this bit. This bit is always read as 1.
6	PRWE	1	R/W	Protect information write enable Bits 5 and 4 can be written to when this bit is set to 1. [Setting condition] • When 0 is written to the WRI bit and 1 is written to the PRWE bit [Clearing conditions] • Reset • When 0 is written to the WRI bit and 0 is written to the PRWE bit
5	LOCKDW	0	R/W	Trimming data register lock down The RC trimming data register (RCTRMDR) cannot be written to when this bit is set to 1. Once this bit is set to 1, this register cannot be written to until a reset is input even if 0 is later written to this bit. [Setting condition] • When 0 is written to the WRI bit and 1 is written to the LOCKDW bit while the PRWE bit is set to 1 [Clearing condition] • Reset
4	TRMDRWE	1	R/W	Trimming date register write enable This register can be written to when the LOCKDW bit is 0 and this bit is 1. [Setting condition] • When 0 is written to the WRI bit and 1 is written to the LOCKDW bit while the PRWE bit is set to 1 [Clearing conditions] • Reset • When 0 is written to the WRI bit and 0 is written to the LOCKDW bit while the PRWE bit is set to 1

- RCTRMDR RC trimming data register Address: H'F737

Bit	Bit Name	Set Value	R/W	Description
7	TRMD7	(0)*	R/W	Trimming data
6	TRMD6	(0)*	R/W	In the flash memory version, trimming data is loaded from flash memory to this register immediately after a reset. These bits are always read as undefined values.
5	TRMD5	(0)*	R/W	
4	TRMD4	(0)*	R/W	
3	TRMD3	(0)*	R/W	The frequency changes as follows, using TRMD7 as the sign bit: (minimum frequency) H'80 ← H'FC ← H'00 → H'04 → H'7C (maximum frequency)
2	TRMD2	(0)*	R/W	
1	TRMD1	0	R	
0	TRMD0	0	R	

Note: * In the flash memory version, these bits are initialized using trimming data values from flash memory.

- TMRW Timer mode register W Address: H'FF80

Bit	Bit Name	Set Value	R/W	Description
7	CTS	1	R/W	Counter start TCNT counter operation is halted when this bit is 0, and the counter operates when this bit is 1.
4	BUFEA	1	R/W	Buffer operation A Selects the GRC function. 0: GRC operates as an input capture/output compare register 1: GRC operates as the buffer register for GRA

- TCRW Timer control register W Address: H'FF81

Bit	Bit Name	Set Value	R/W	Description
7	CCLR	0	R/W	Counter clear The TCNT value is cleared by compare match A when this bit is 1. When this bit is 0, TCNT operates as a free-running counter.
6	CKS2	0	R/W	Clock select 2 to 0
5	CKS1	0	R/W	Selects the clock input to TCNT.
4	CKS0	0	R/W	000: Internal clock: counts on ϕ 001: Internal clock: counts on $\phi/2$ 010: Internal clock: counts on $\phi/4$ 011: Internal clock: counts on $\phi/8$ 1XX: Counts on rising edges of external event (FTCI)

Note: X: Don't care

- TIERW Timer interrupt enable register W Address: H'FF82

Bit	Bit Name	Set Value	R/W	Description
0	IMIEA	1	R/W	Input capture/compare match interrupt enable A When this bit is set to 1, IMIA interrupt requests using IMFA in TSRW are enabled.

- TSRW Timer status register W Address: H'FF83

Bit	Bit Name	Set Value	R/W	Description
7	OVF	0	R/W	Timer overflow flag [Setting condition] • When TCNT overflows from H'FFFF to H'0000 [Clearing condition] • When this bit is read as 1 and then 0 is written to it
0	IMFA	0	R/W	Input capture/compare match flag A [Setting condition] • When the TCNT value is transferred to GRA by an input capture signal when GRA is functioning as an input capture register [Clearing condition] • When this bit is read as 1 and then 0 is written to it

- TIOR0 Timer I/O control register 0 Address: H'FF84

Bit	Bit Name	Set Value	R/W	Description
2	IOA2	1	R/W	I/O control A2 Selects the GRA function. 0: GRA functions as an output compare register 1: GRA functions as an input capture register
1	IOA1	0	R/W	I/O control A1 and A0
0	IOA0	0	R/W	When IOA2 = 1 00: GRA input capture at rising edge of FTIOA pin 01: GRA input capture at falling edge of FTIOA pin 1X: Input capture at rising and falling edges of FTIOA pin

Note: X: Don't care

- TIOR1 Timer I/O control register 1 Address: H'FF85

Bit	Bit Name	Set Value	R/W	Description
2	IOC2	1	R/W	I/O control C2 Selects the GRC function. 0: Functions as an output compare register 1: Functions as an input capture register If GRA buffer operation has been selected by BUFEA in TMRW, the same function as GRA should be selected.
1	IOC1	0	R/W	I/O control C1 and C0
0	IOC0	0	R/W	When IOC2 = 1 00: GRC input capture at rising edge of FTIOC pin 01: GRC input capture at falling edge of FTIOC pin 1X: Input capture at rising and falling edges of FTIOC pin

Note: X: Don't care

- TCNT Timer counter Address: H'FF86

  Description: A 16-bit readable/writable up-counter. TCNT must always be read or written to in 16-bit units; 8-bit access is not allowed. The initial value of TCNT is H'0000.

  Set value: H'0000

- GRA General register A Address: H'FF88

  Description: A 16-bit readable/writable register to which TCNT values are transferred during input capture operation. GRA must always be read or written to in 16-bit units; 8-bit access is not allowed.

  Set value: —

  Note: —: Undefined

- GRC General register C Address: H'FF8C

  Description: A 16-bit readable/writable register. When GRC is set as the buffer of GRA, during input capture operation TCNT values are transferred to GRA and then from GRA to the buffer register GRC. TCNT values are transferred at the rising edge of the FTIOA. GRC must always be read or written to in 16-bit units; 8-bit access is not allowed.

  Set value: —

  Note: —: Undefined

- TCSRWD Timer control/status register WD Address: H'FFC0

Bit	Bit Name	Set Value	R/W	Description
5	B4WI	0	R/W	Bit 4 write inhibit Bit 4 in this register can be written to only when 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	1	R/W	Timer control/status register W write enable Writing to bits 2 and 0 in this register is enabled when this bit is set to 1. When writing 0 to this bit, the value written to bit 5 must be 0 as well.
3	B2WI	0	R/W	Bit 2 write inhibit Bit 2 in this register can be written to only when 0 is written to this bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog timer on TCWD (timer counter WD) starts counting up when this bit is set to 1 and halts when the this bit is cleared to 0. The watchdog timer is enabled in the initial state. Clear this bit to 0 if the watchdog timer will not be used. [Clearing conditions] • Reset • When 0 is written to the B2WI bit and 0 is written to the WDON bit while the TCSRWE bit is set to 1 [Setting condition] • When 0 is written to the B2WI bit and 1 is written to the WDON bit while the TCSRWE bit is set to 1

4.4 Constants Used

The constants used in this sample task are shown in table 3.

Table 3 Constants Used

Label	Constant Value	Description	Used in
ERROR	7	Error code	main trimming
HZ	9	Desired frequency [MHz]	trimming
IN_PERIOD	10	Pulse cycle input to FTIOA pin [10 µs]	
MAX_FRE	105	105% of desired frequency (used to determine if frequency is in desired frequency range)	
MIN_FRE	95	95% of desired frequency (used to determine if frequency is in desired frequency range)	
OK	0	OK code	

4.5 RAM Usage

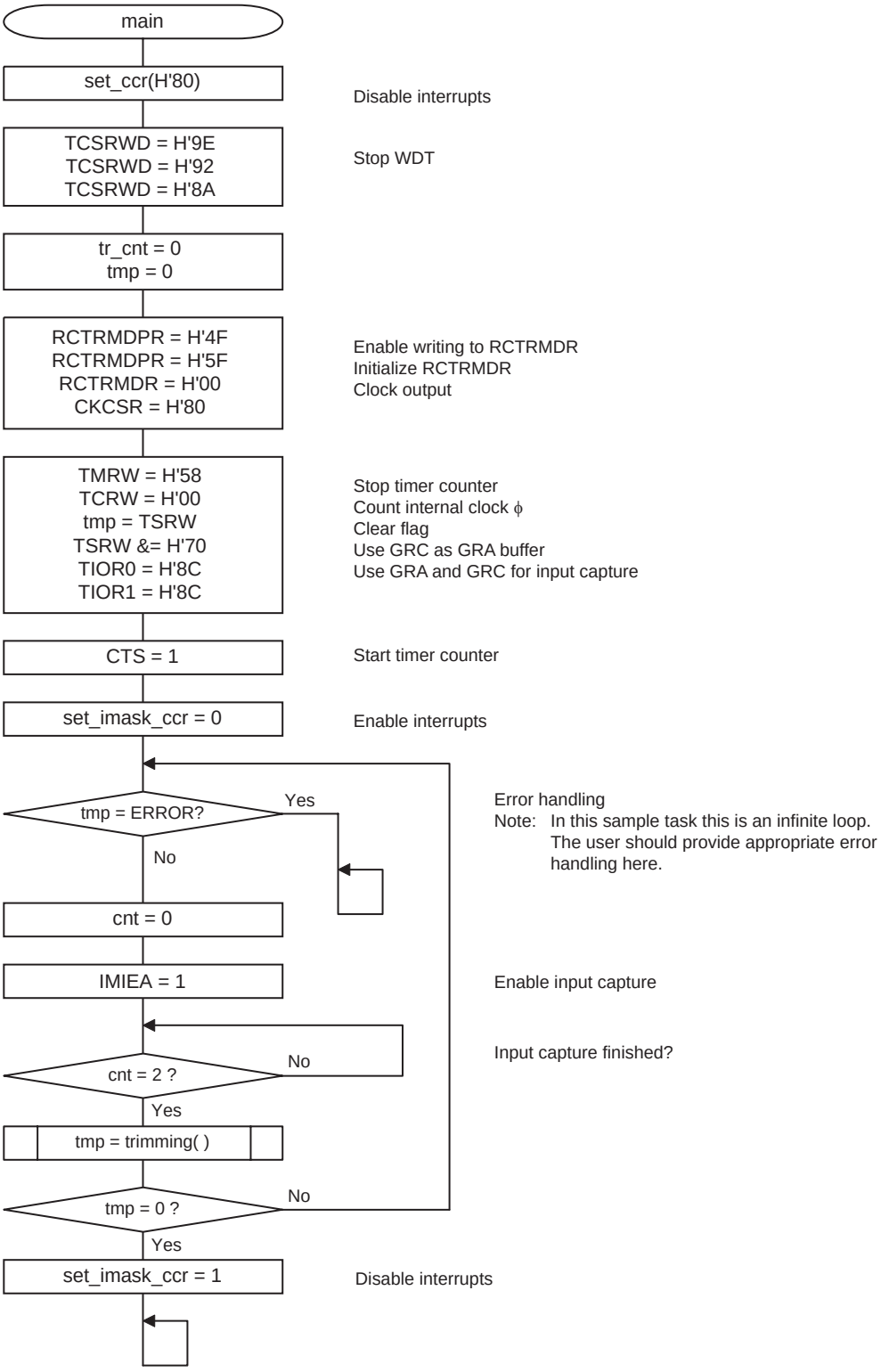
The RAM usage in this sample task is shown in table 4.

Table 4 RAM Usage

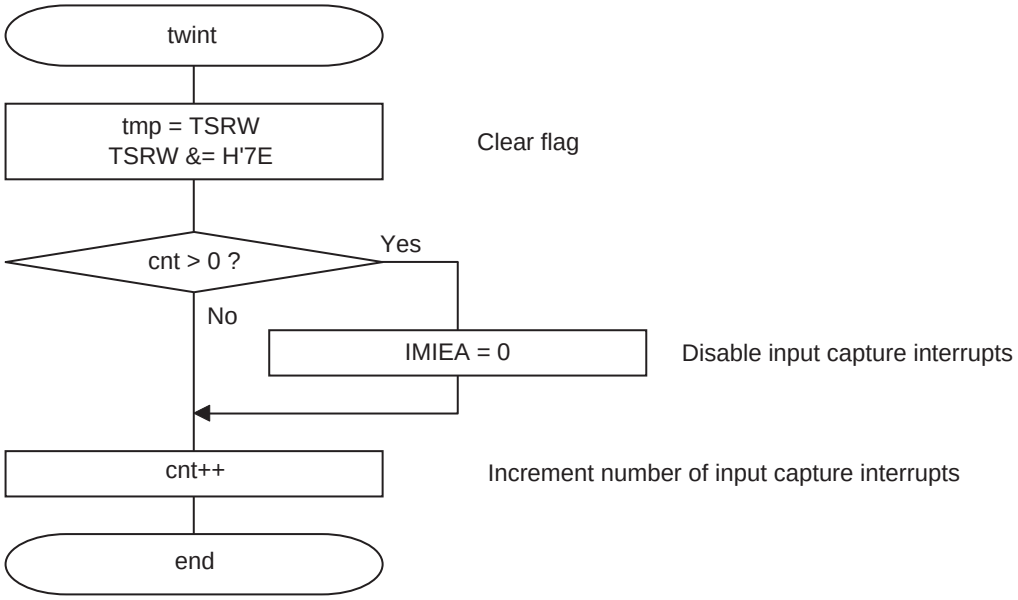
Constant	Description	Amount of Memory Used	Used in
cnt	Number of input captures	1 byte	main
tr_cnt	Number of times trimming data is rewritten	1 byte	main trimming

5. Flowcharts

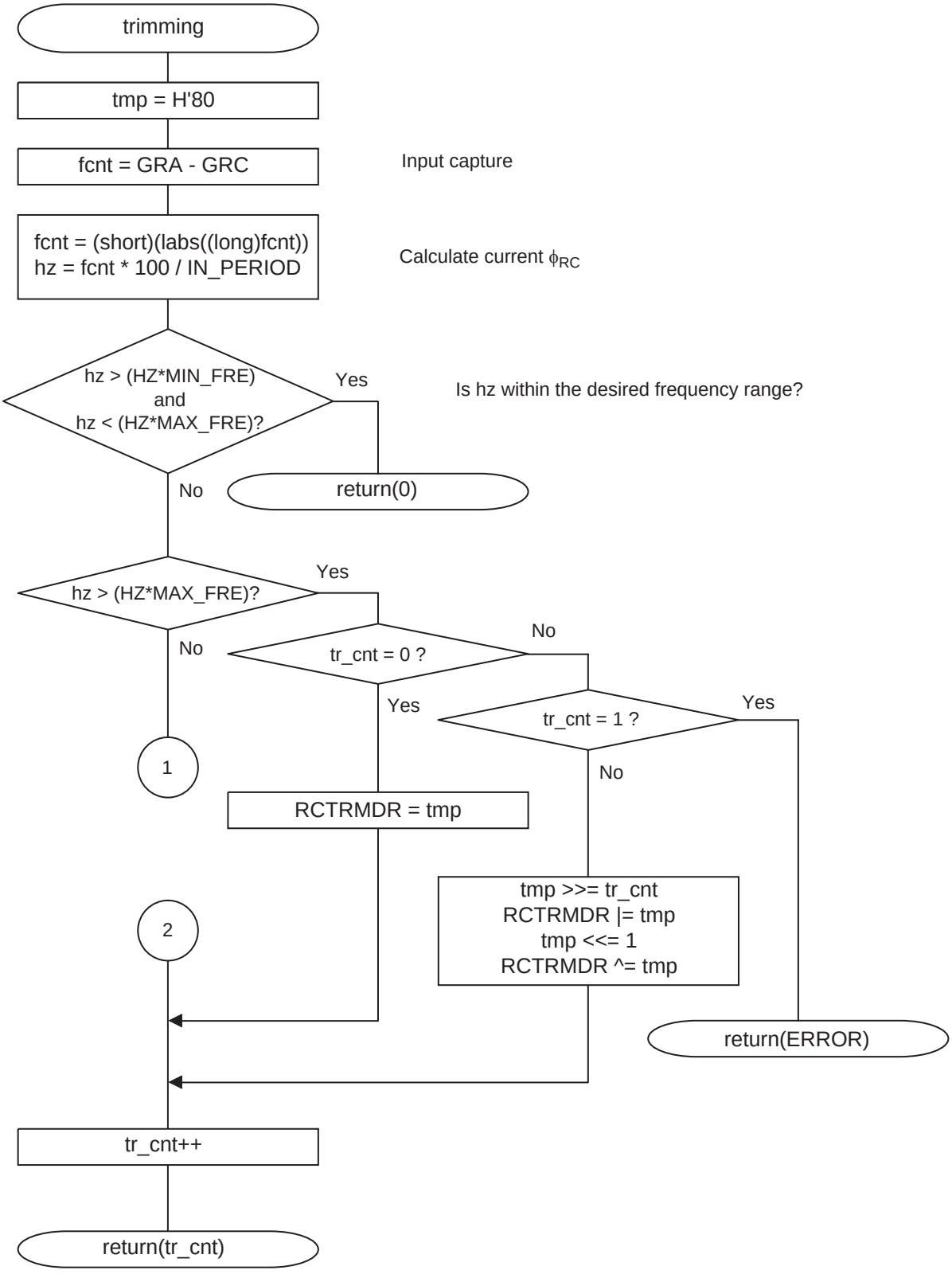
5.1 main

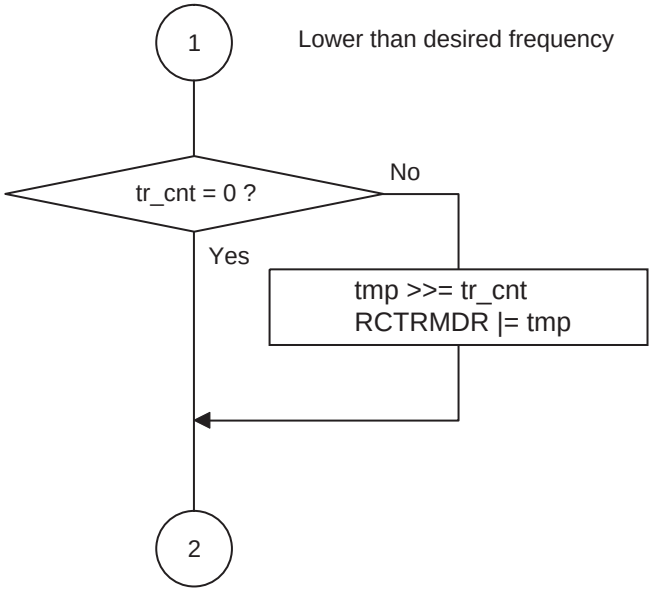


5.2 twint


twint
tmp = TSRW
TSRW &= H'7E
Clear flag
cnt > 0 ?
Yes
No
IMIEA = 0
Disable input capture interrupts
cnt++
Increment number of input capture interrupts
end

5.3 trimming


trimming
tmp = H'80
fcnt = GRA - GRC
Input capture
fcnt = (short)(labs((long)fcnt))
hz = fcnt * 100 / IN_PERIOD
Calculate current ϕRC
hz > (HZ*MIN_FRE)
and
hz < (HZ*MAX_FRE)?
Yes
Is hz within the desired frequency range?
No
return(0)
hz > (HZ*MAX_FRE)?
Yes
No
tr_cnt = 0 ?
No
Yes
tr_cnt = 1 ?
Yes
No
1
RCTRMDR = tmp
tmp >>= tr_cnt
RCTRMDR |= tmp
tmp <<= 1
RCTRMDR ^= tmp
2
return(ERROR)
tr_cnt++
return(tr_cnt)



5.4 Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'002A
P	H'0100
B	H'FD80

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Dec.20.04	—	First edition issued

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