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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

Low-Voltage Detection (LVD) Function

Introduction

This application uses the low-voltage detection circuit (LVD) to detect a fall in the external power supply voltage via the ExtD and ExtU pins. It executes interrupt processing according to the voltage detected on the ExtD and ExtU pins.

Target Device

H8/36912

Contents

1. Specifications

Figure 1 shows the circuit connections in this sample task. Table 1 summarizes the characteristics of the external input voltage detection circuit of the power-supply voltage detection and low-voltage detection interrupt circuit (LVDI).

The ExtD and ExtU pins are connected as shown in figure 1 and the voltages on them are defined as VextD and VextU, respectively. The LVD monitors the VextD and VextU to detect a fall in the external power supply voltage.

In this sample task, P20 is specified as an output pin to be used for confirming the operation and its output is set to 0 as the initial state.

If VextD falls below the Vexd voltage, a low-voltage interrupt occurs and the P20 output is brought high.

If the Vcc of the microcomputer does not falls below the Vreset1 voltage and VextU increases to the Vexd voltage or greater, a voltage-rise interrupt occurs and the P20 output is brought low.

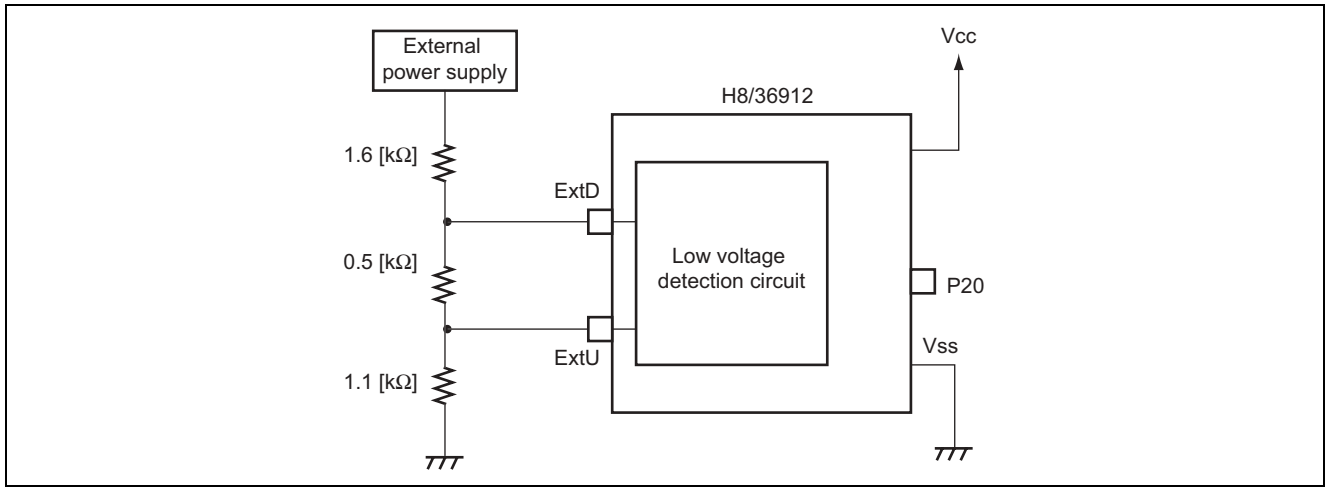


Figure 1 Example of Circuit Connections

Table 1 Characteristics of External Input Voltage Detection Circuit of the Power-Supply Voltage Detection and Low-Voltage Detection Interrupt Circuit (LVDI)

Item	Symbol	Measurement Condition	Values			Unit
			Min.	Typ.	Max.	
Reset detection voltage	Vreset1	LVDSEL = 0	2.0	2.3	2.7	V
ExtD/ExtU input detection voltage	Vexd	—	0.85	1.15	1.45	V
ExtD input voltage range	VextD	VextD > VextU	–0.3	—	Either Avcc + 0.3 or Vcc + 0.3, whichever is lower	V
ExtU input voltage range	VextU					

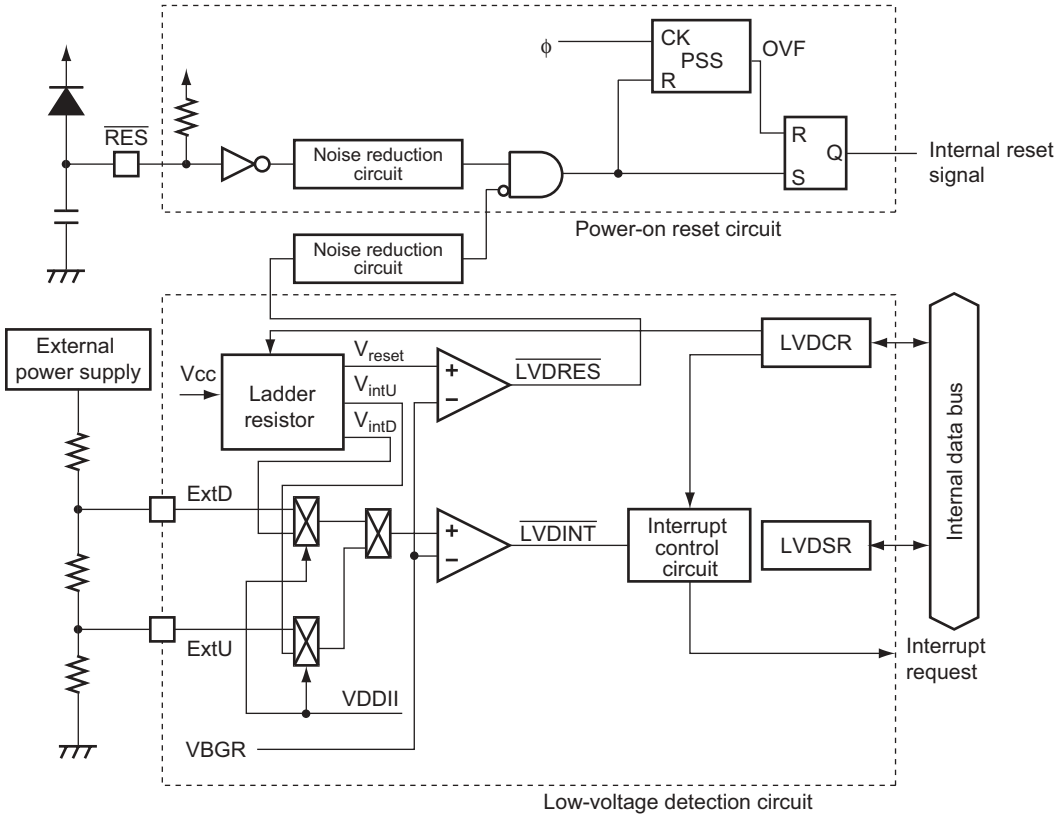
2. Description of Functions

2.1 Microcomputer Functions Used

In this sample task, the internal low-voltage detection circuit (LVD) is used to control operation during low voltage. Figure 2 shows a block diagram of the power-on reset circuit and low-voltage detection circuit.

The functions used in this sample task are described blow.

- System clock (ϕ)
  The system clock is a reference clock used to drive the CPU and peripheral functions. In this sample task, the internal operating frequency is 8 MHz.
- Prescaler S (PSS)
  The prescaler S (PSS) is a 13-bit counter which takes ϕ as input and increments by 1 for each clock cycle.
- Low-voltage detection control register (LVDCR)
  LVDCR enables or disables the low-voltage detection circuit and BGR circuit, selects the voltage for comparison by the LVDI circuit, sets the detection level for the LVDR circuit, enables or disables a reset by the LVDR circuit, and enables or disables generation of an interrupt when the power-supply voltage rises or falls.
- Low-voltage detection status register (LVDSR)
  LVDSR indicates whether the power-supply voltage falls below or rises above the given values.
- Port mode register 1 (PMR1)
  PMR1 specifies the P14 pin as an $\overline{\text{IRQ0}}$ input pin.
- Interrupt edge select register (IEGR1)
  IEGR1 selects the edge (rising or falling) for interrupt request generation by the $\overline{\text{IRQ0}}$ pin.
- Interrupt enable register 1 (IENR1)
  IENR1 is set to enable the $\overline{\text{IRQ0}}$ pin interrupt.
- Interrupt flag register 1 (IRR1)
  IRR1 contains the IRQ0 interrupt request status flag.
- Timer control/status register WD (TCSRWD)
  TCSRWD controls the writing to TCSRWD and TCWD. The TCSRWD register also provides the function to control the watchdog timer operation and indicate the status. To modify the TCSRWD value, a MOV instruction should be used. Note that the TCSRWD cannot be modified by bit handling instructions.
- Port control register 2 (PCR2)
  Each bit of PCR2 selects the input/output of the corresponding port 2 pin which is used as a general I/O port.
- Port data register 2 (PDR2)
  PDR2 is a general I/O port data register for port 2.



[Legend]
PSS: Prescaler S
LVDCR: Low-voltage detection control register
LVDSR: Low-voltage detection status register
VBGR: Reference voltage from BGR
ExtD: Voltage compared to detect a fall in the externally input power supply voltage
ExtU: Voltage compared to detect a rise in the externally input power supply voltage
VDDII: Bit 5 of LVDCR

Figure 2 Block Diagram of Power-On Reset Circuit and Low-Power Detection Circuit

2.2 Function Assignment

Table 2 shows the assignment of functions used in this sample task.

In this sample task, the LVD function is used based on the function assignment shown in table 2.

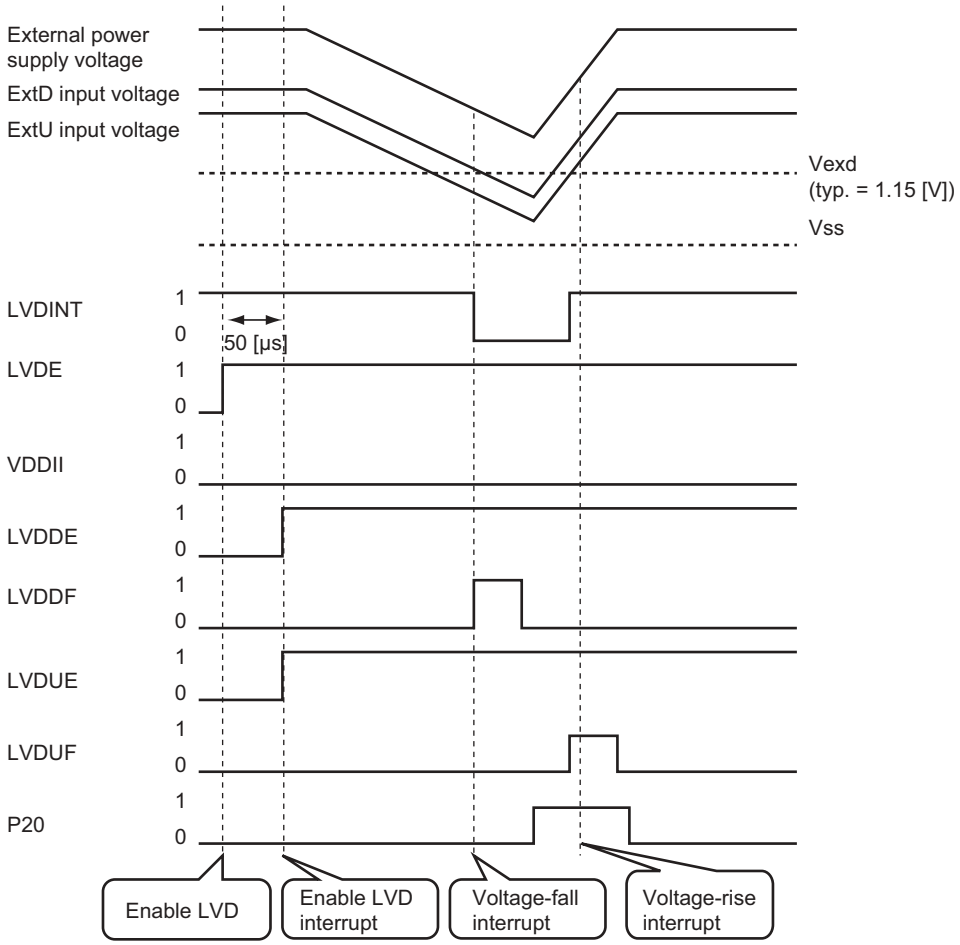
Table 2 Assignment of Functions

Element	Description
LVDCR	Provides settings for the low-voltage detection circuit.
LVDSR	Used to check whether the power supply voltage has fallen below or risen above a specific voltage.
PMR1	Sets up the P14 pin as $\overline{\text{IRQ0}}$ input pin.
IEGR1	Selects falling edge detection for the $\overline{\text{IRQ0}}$ pin input.
IENR1	Enables interrupt requests by the $\overline{\text{IRQ0}}$ pin.
IRR1	Indicates the IRQ3 interrupt request status flag.
TCSRWD	Stops the watchdog timer.
PCR2	Sets up P20 to function as an output pin, which is used to confirm the operation.
PDR2	Sets an output value for P20, which is used to confirm the operation.

3. Principles of Operation

Figure 3 shows the operation timing of the low-voltage detection interrupt circuit. Table 3 summarizes the hardware and software processing performed in the operation shown in figure 3.

When Vcc of the microcomputer falls below 2.3 V (typ.), a low-voltage-detection reset occurs.



[Legend]
LVDINT: LVD interrupt signal
LVDE: LVD interrupt enable
VDDII: LVDI external comparison voltage input disable
LVDDE: Voltage-fall interrupt enable
LVDDF: LVD power-supply voltage fall flag
LVDUE: Voltage-rise interrupt enable
LVDUF: LVD power-supply voltage rise flag

Figure 3 Operation Timing of Low-Voltage Detection Interrupt Circuit (When the ExtU and ExtD pin inputs are used for voltage detection)

Table 3 Hardware and Software Processing

No.	Item	Hardware Processing	Software Processing
1	Enable LVD	Enable the LVD circuit	1. Disable interrupts. 2. Stop the WDT. 3. Sets the use of the LVD circuit. 4. Wait until the LVD circuit is stabilized using a software timer.
2	Enable LVD interrupt	None	1. Clear LVDDF and LVDUF to 0. 2. Set LVDDE and LVDUE for enabling. 3. Specify P20 as an output port and set the P20 output to 0. 4. Set up an IRQ0 interrupt. 5. Enable interrupts.
3	Voltage-fall iInterrupt	1. Set LVDDF to 1. 2. Generate an IRQ0 interrupt request.	1. Clear IRRI0 to 0. 2. Clear LVDDF to 0. 3. Set the P20 output to 1.
4	Voltage-rise interrupt	1. Set LVDUF to 1. 2. Generate an IRQ0 interrupt request.	1. Clear IRRI0 to 0. 2. Clear LVDUF to 0. 3. Set the P20 output to 0.

4. Description of Software

4.1 Modules

Table 4 shows the modules used in this sample task.

Table 4 Description of Modules

Label Name	Function
main	Stops the watchdog timer and sets up the P20 pin, low-voltage detection circuit, and IRQ0 interrupt.
Ivdint	LVD interrupt processing routie that clears the IRRI0 flag and switches the P20 output value according to the LVD interrupt flag status.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- LVDCR: Low-Voltage Detection Control Register (Address: H'F730)

Bit	Bit Name	Setting	R/W	Function
7	LVDE	1	R/W	LVD Enable 0: The low-voltage detection circuit is not used. 1: The low-voltage detection circuit is used. When the BGRE bit in this register is cleared to 0, the low-voltage detection circuit is not used regardless of the LVDE bit setting.
6	BGRE	1	R/W	BGR Enable 0: The BGR circuit* is not used. 1: The BGR circuit* is used.
5	VDDII	0	R/W	External LVDI Comparison Voltage Input Disable 0: External voltage is used for comparison by the LVDI circuit. 1: Internal voltage is used for comparison by the LVDI circuit.
3	LVDSEL	0	R/W	LVDR detection level selection 0: Reset detection voltage is 2.3 V (typ.) 1: Reset detection voltage is 3.6 V (typ.) When the falling or rising voltage detection interrupt is used, the reset detection voltage should be specified as 2.3 V (typ.)
2	LVDRE	1	R/W	LVDR enable 0: Disables a reset by LVDR. 1: Enables a reset by LVDR.
1	LVDDE	1	R/W	Voltage-fall interrupt enable 0: Disables iInterrupt request on a fall in power-supply voltage. 1: Enables iInterrupt request on a fall in power-supply voltage.
0	LVDUE	1	R/W	Voltage-rise interrupt enable 0: Disables iInterrupt request on a rise in power-supply voltage. 1: Enables iInterrupt request on a rise in power-supply voltage.

Note: * A circuit that outputs a stable reference voltage over the entire ranges of the operating voltage and operating temperature that are given in the "Electrical Characteristics".

- LVDSR: Low-Voltage Detection Status Register (Address: H'F731)

Bit	Bit Name	Setting	R/W	Function
1	LVDDF	0*	R/W	LVD power-supply voltage fall flag [Setting condition] When an external power supply voltage falls and the VextD detected via the ExtD pin falls below 1.15 V (typ.). [Clearing condition] When 0 is written to this bit after 1 is read from it.
0	LVDUF	0*	R/W	LVD power-supply voltage rise flag [Setting condition] When the VextD detected via the ExtD pin falls below 1.15 V (typ.) while the LVDUE bit in LVDCR is set to 1 and then VextU rises above 1.15 V (typ.) before the power supply voltage falls below Vreset1 (2.3 V typ). [Clearing condition] When 0 is written to this bit after 1 is read from it.

Note: Reset during initialization by LVDR.

- TCSRWD: Timer Control/Status Register (Address: H'FFC0)

Bit	Bit Name	Setting	R/W	Function
5	B4WI	0	R/W	Bit-4 Write Disable Writing to bit 4 of this register is only enabled when a 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	1	R/W	Timer Control/Status Register WD Write Disable When this bit is set to 1, writing to bits 0 and 2 of this register is enabled. Note that bit 5 should be cleared to 0 when writing to this bit.
3	B2WI	0	R/W	Bit-2 Write Disable Writing to bit 2 of this register is only enabled when a 0 is written to this bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On When this bit is set to 1, TCWD starts counting up. When cleared to 0, TCWD stops counting. The watchdog timer is ON with the initial value of this bit. When not using the watchdog timer, this bit should be cleared to 0. [Clearing conditions] • Reset • When B2WI and WDON are cleared to 0 while TCSRWE = 1. [Setting condition] • When B2WI is cleared to 0 and WDON is set to 1 while TCSRWE = 1.

- PDR2: Port Data Register 2 (Address: H'FFD5)

Bit	Bit Name	Setting	R/W	Function
0	P20	0	R/W	Stores port 2 output value. When this register is read, the value of this register is read for a bit whose corresponding bit in PCR2 is set to 1; for a bit whose corresponding bit in PCR2 is clear, the pin state is read regardless of the value of this register.

- PMR1: Port Mode Register 1 (Address: H'FFE0)

Bit	Bit Name	Setting	R/W	Function
4	IRQ0	1	R/W	Selects the P14/$\overline{\text{IRQ0}}$ pin function. 0: General I/O port P14 1: $\overline{\text{IRQ0}}$ input pin

- PCR2: Port Control Register 2 (Address: H'FFE5)

Bit	Bit Name	Setting	R/W	Function
0	PCR20	1	W	When this bit is set to 1 while the general I/O port function is selected, the corresponding pin functions as an output port; and when cleared to 0, the pin functions as an input port.

- IEGR1: Interrupt Edge Select Register 1 (Address: H'FFF2)

Bit	Bit Name	Setting	R/W	Function
4	IEG0	0	R/W	IRQ0 edge select 0: Detects the falling edge of the $\overline{\text{IRQ0}}$ pin input. 1: Detects the rising edge of the $\overline{\text{IRQ0}}$ pin input.

- IENR1: Interrupt Enable Register 1 (Address: H'FFF4)

Bit	Bit Name	Setting	R/W	Function
0	IEN0	1	R/W	IRQ0 interrupt request enable Setting this bit to 1 enables interrupt requests of the $\overline{\text{IRQ0}}$ pin.

- IRR1: Interrupt Flag Register 1 (Address: H'FFF6)

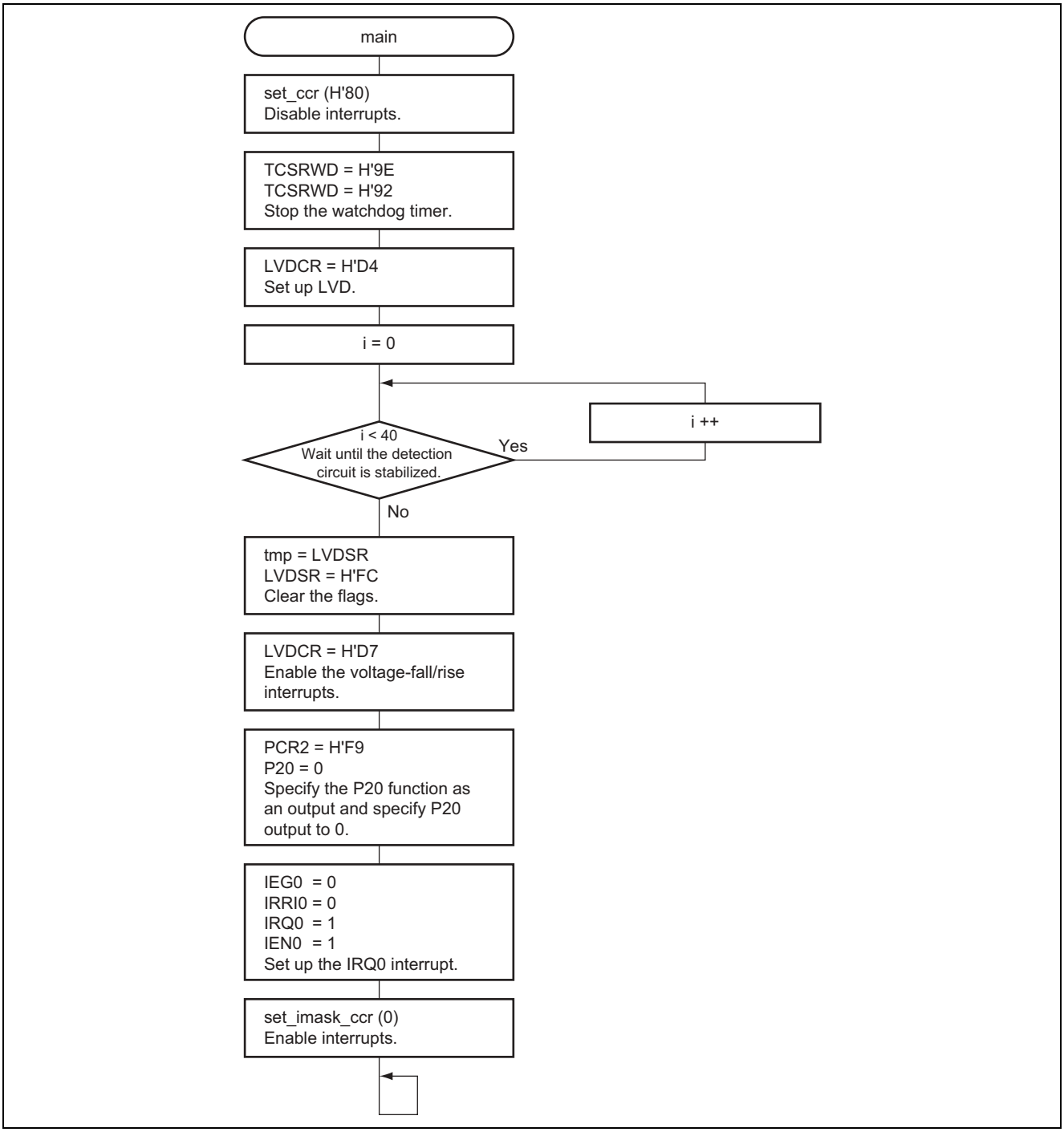
Bit	Bit Name	Setting	R/W	Function
0	IRRI0	0	R/W	IRQ0 interrupt request flag Setting condition: When the $\overline{\text{IRQ0}}$ pin is enabled and the specified edge is detected. Clearing condition: When a 0 is written to this bit.

4.4 RAM Usage

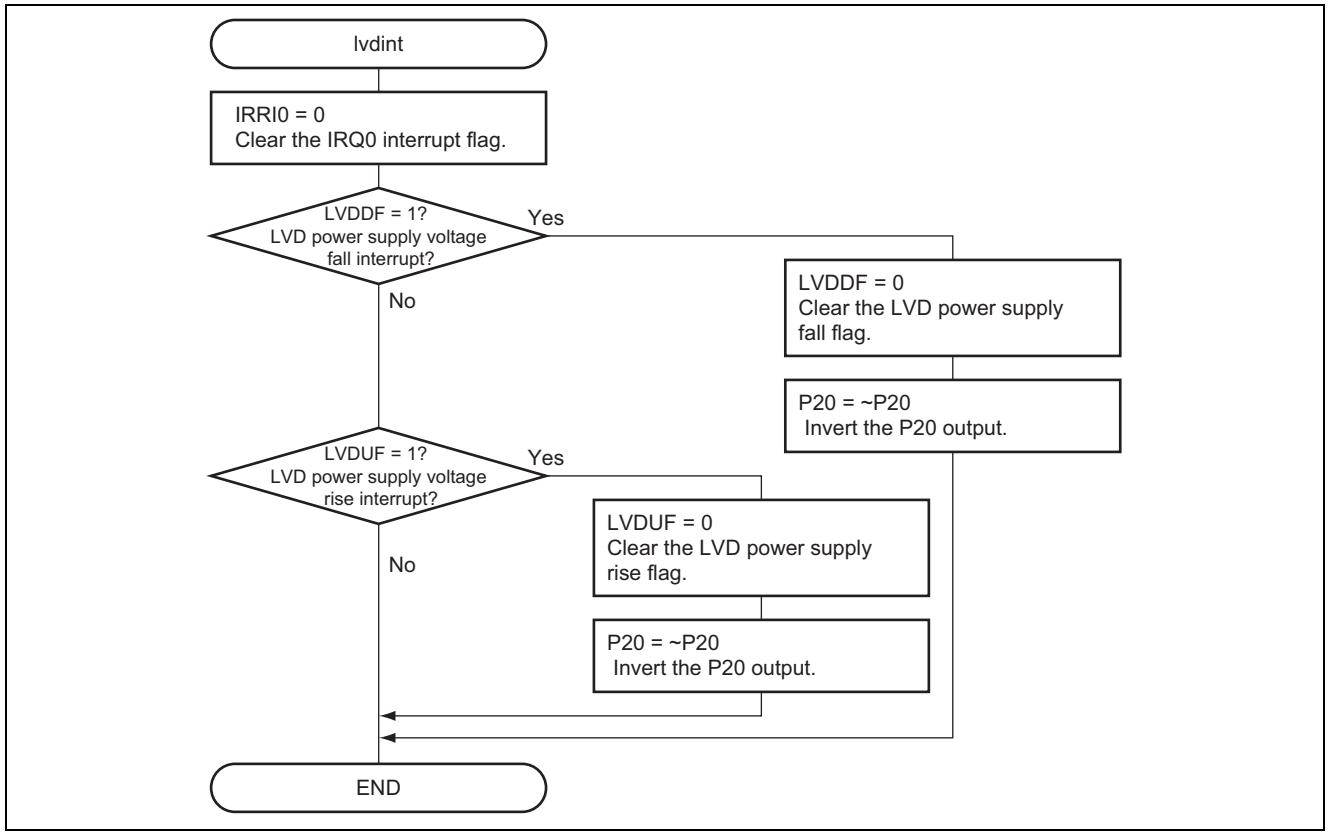
This sample task does not use RAM.

5. Flowchart

5.1 main



5.2 lvdint


lvdint
IRRI0 = 0
Clear the IRQ0 interrupt flag.
LVDDF = 1?
LVD power supply voltage
fall interrupt?
Yes
No
LVDDF = 0
Clear the LVD power supply
fall flag.
P20 = ~P20
Invert the P20 output.
LVDUF = 1?
LVD power supply voltage
rise interrupt?
Yes
No
LVDUF = 0
Clear the LVD power supply
rise flag.
P20 = ~P20
Invert the P20 output.
END

6. Program Listing

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300H Series -H8/36912-                                                                   */
/*  Application Note                                                                            */
/*                                                                                              */
/*  'Set port by LVDI'                                                                          */
/*                                                                                              */
/*  Function                                                                                    */
/*  : LVD (interrupt by Low-Voltage-Detect)                                                     */
/*                                                                                              */
/*  External Clock : 8MHz                                                                       */
/*  Internal Clock : 8MHz                                                                       */
/*  Sub Clock      : 32.768kHz                                                                  */
/*                                                                                              */
/************************************************************************************************/

#include    <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define TCSRWD      *(volatile unsigned char *)0xFFC0    /* Timer Controller/Status Register WD*/
#define TCSRWD_BIT  (*(volatile struct BIT *)0xFFC0)
#define B4WI        TCSRWD_BIT.b5                        /* Bit 4 Write Disable                */
#define TCSRWE      TCSRWD_BIT.b4                        /* Timer Controller/                  */
                                                         /*           Status Register W Enable */
#define B2WI        TCSRWD_BIT.b3                        /* Bit 2 Write Disable                */
#define WDON        TCSRWD_BIT.b2                        /* WD Timer ON                        */

#define LVDCR       *(volatile unsigned char *)0xF730    /* Low-Voltage-Detect control register*/
#define LVDCR_BIT   (*(volatile struct BIT *)0xF730)
#define LVDE        LVDCR_BIT.b7                         /* LVD Enable                         */
#define BGRE        LVDCR_BIT.b6                         /* BGR Enable                         */
#define VDDII       LVDCR_BIT.b5                         /* Select LVDI comparative voltage    */
#define LVDSEL      LVDCR_BIT.b3                         /* LVDI Detection Level Select        */
#define LVDRE       LVDCR_BIT.b2                         /* LVDR Enable                        */
#define LVDDE       LVDCR_BIT.b1                         /* LVD voltage Descent Enable         */
#define LVDUE       LVDCR_BIT.b0                         /* LVD voltage UP Enable              */
#define LVDSR       *(volatile unsigned char *)0xF731    /* Low-Voltage-Detect Status Register */
#define LVDSR_BIT   (*(volatile struct BIT *)0xF731)
#define LVDDF       LVDSR_BIT.b1                         /* LVD Power-Supply Voltage Fall      */
#define LVDUF       LVDSR_BIT.b0                         /* LVD Power-Supply Voltage Rise      */
#define PMR1        *(volatile unsigned char *)0xFFE0    /* Port Mode Register 1               */
#define PMR1_BIT    (*(volatile struct BIT *)0xFFE0)
#define IRQ0        PMR1_BIT.b4                          /* P14/IRQ0 Pin Function Switch       */
```

```
#define IEGR1       *(volatile unsigned char *)0xFFF2    /* Interrupt Edge Select Register     */
#define IEGR1_BIT   (*(volatile struct BIT *)0xFFF2)
#define IEG0        IEGR1_BIT.b0                         /* IRQ0 Edge Select                   */
#define IENR1       *(volatile unsigned char *)0xFFF4    /* Interrupt Enable Register 1        */
#define IENR1_BIT   (*(volatile struct BIT *)0xFFF4)
#define IEN0        IENR1_BIT.b0                         /* IRQ0 Interrupt Enable              */
#define IRR1        *(voltage unsigned char *)0xFFF6     /* Interrupt Request Register 1       */
#define IRR1_BIT    (*(volatile struct BIT *)0xFFF6)
#define IRRI0       IRR1_BIT.b0                          /* IRQ0 Interrupt Request Flag        */

#define PCR2        *(volatile unsigned char *)0xFFE5    /* Port Control Register 2            */
#define PCR2_BIT    (*(volatile struct BIT *)0xFFE5)
#define PCR20       PCR2_BIT.b0                          /* Port Control Register 2 bit 0      */
#define PDR2        *(volatile unsigned char *)0xFFD5    /* Port Data Register 2               */
#define PDR2_BIT    (*(volatile struct BIT *)0xFFD5)
#define P20         PDR2_BIT.b0                          /* Port Data Register 2 bit 0         */

#pragma interrupt (lvdint)
/************************************************************************************************/
/*  Function define                                                                             */
/************************************************************************************************/
void main ( void );
void lvdint ( void );

/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section     V1                                   /* VECTOR SECTOIN SET                 */
void (*const VEC_TBL1[])(void) = {
    main
};

#pragma section     V2                                   /* VECTOR SECTOIN SET                 */
void (*const VEC_TBL2[])(void) = {
    lvdint                                               /* LVD interrupt                      */
};

#pragma entry main(sp=0xFF80)
#pragma section                                          /* P                                  */
/************************************************************************************************/
/*  Main Program                                                                                */
/************************************************************************************************/
void main ( void )
{
    unsigned char tmp, i;

    set_ccr(0x80);                                       /* Interrupt Disable                  */

    TCSRWD = 0x9E;                                       /* STOP                               */
    TCSRWD = 0x92;                                       /* WD                                 */

    LVDCR = 0xD4;                                        /* Set up LVD                         */
    for(i=0; i<40; i++);                                 /* Wait Detection circuit stable time */
                                                         /*                          (50us over) */

    tmp = LVDSR;
    LVDSR = 0xFC;                                        /* Clear LVDDF, LVDUF                 */
    LVDCR = 0xD7;                                        /* Set LVDDE, LVDUE                   */
```

```
    PCR2 = 0xF9;                                    /* P20 -> output                    */
    P20 = 0;                                        /* For the movement confirmation    */

    IEG0 = 0;                                       /* IRQ0 Interrupt Edge Select       */
    IRRI0 = 0;                                      /* Clear IRQ0 Interrupt Flag        */
    IRQ0 = 1;
    IEN0 = 1;                                       /* IRQ0 Interrupt Enable            */

    set_imask_ccr(0);                               /* Interrupt Enable                 */

    while(1);
}

/****************************************************************************************/
/*  LVD Interrupt                                                                       */
/****************************************************************************************/
void lvdint ( void )
{
    IRRI0 = 0;                                      /* Clear IRQ0 Interrupt Flag        */

    if(LVDDF == 1){                                 /* LVD Power-Supply Voltage Fall ?  */
        LVDDF = 0;
        P20 = ~P20;                                 /* For the movement confirmation    */
    }
    else if(LVDUF == 1){                            /* LVD Power-Supply Voltage Rise ?  */
        LVDUF = 0;
        P20 = ~P20;                                 /* For the movement confirmation    */
    }
}
```

Link Address Specification

Section Name	Address
CV1	H'0000
CV2	H'001C
P	H'0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.28.04	—	First edition issued

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