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April 1st, 2010
Renesas Electronics Corporation

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H8/300H SLP Series

Counting Up Using RTC Free Running Counter Function

Introduction

The free running counter function of the realtime clock (RTC) is used to increment an 8-bit counter set in RAM. The 8-bit counter is incremented by RTC overflow, and when overflow occurs when the 8-bit counter reaches H'FF, the counter is initialized to H'00 and continues counting up.

Target Device

H8/38076R

Contents

1. Specifications

- The free running counter function of the realtime clock (RTC) is used to increment an 8-bit counter set in RAM.
- When the second data register/free running counter data register (RSECDR) overflows, an RTC interrupt request is generated.
- The 8-bit counter set in RAM counts up from H'00 in RTC interrupt processing. When the counter is incremented when H'FF, it is initialized to H'00 and continues counting up again.
- The RTC interrupt is set to be generated every 3.2768 ms when the free running counter (RSECDR) overflows.

2. Functions Used

2.1 Functions

In this sample task, the RTC free running counter function is used to increment an 8-bit counter set in RAM. A block diagram of the RTC free running counter function is shown in figure 1. The block diagram of the RCT free running counter function is explained below.

- System clock (ϕ)

  A 10-MHz clock used as the reference clock for operating the CPU and peripheral functions
- Prescaler S (PSS)

  A 13-bit counter with ϕ as input, incremented every cycle
- RTC interrupt flag register (RTCFLG)

  The status register for interrupt requests. In this sample task, the RTC interrupt request flag (FOIFG) is set to 1 when RTC free running counter overflows. A flag is not cleared automatically when the corresponding interrupt is accepted. The flag should be cleared by writing 0 to it.
- Second data register/free running counter data register (RSECDR)

  Functions as the 8-bit counter read register during operation as a free running counter. In this sample task, the input clock is set to ϕ/128.
- RTC control register 1 (RTCCR1)

  Performs RTC operation stop/start and reset control.
- RTC control register 2 (RTCCR2)

  Controls enabling/disabling of interrupts. In this sample task, interrupts due to free running counter overflow are enabled.
- Clock source select register (RTCCSR)

  Selects the clock source. In this sample task, RSECDR operates as a free running counter counting on ϕ/128.
- Interrupt enable register 1 (IENR1)

  Controls enabling/disabling of interrupt requests. In this sample task, RTC interrupt requests are enabled.

An example of calculation of the free running counter data register (RSECDR) overflow cycle is shown below.

$$\text{RSECDR overflow cycle} = \frac{1}{\text{System clock} / 128} \times 256$$
$$= 3.2768 \text{ ms}$$

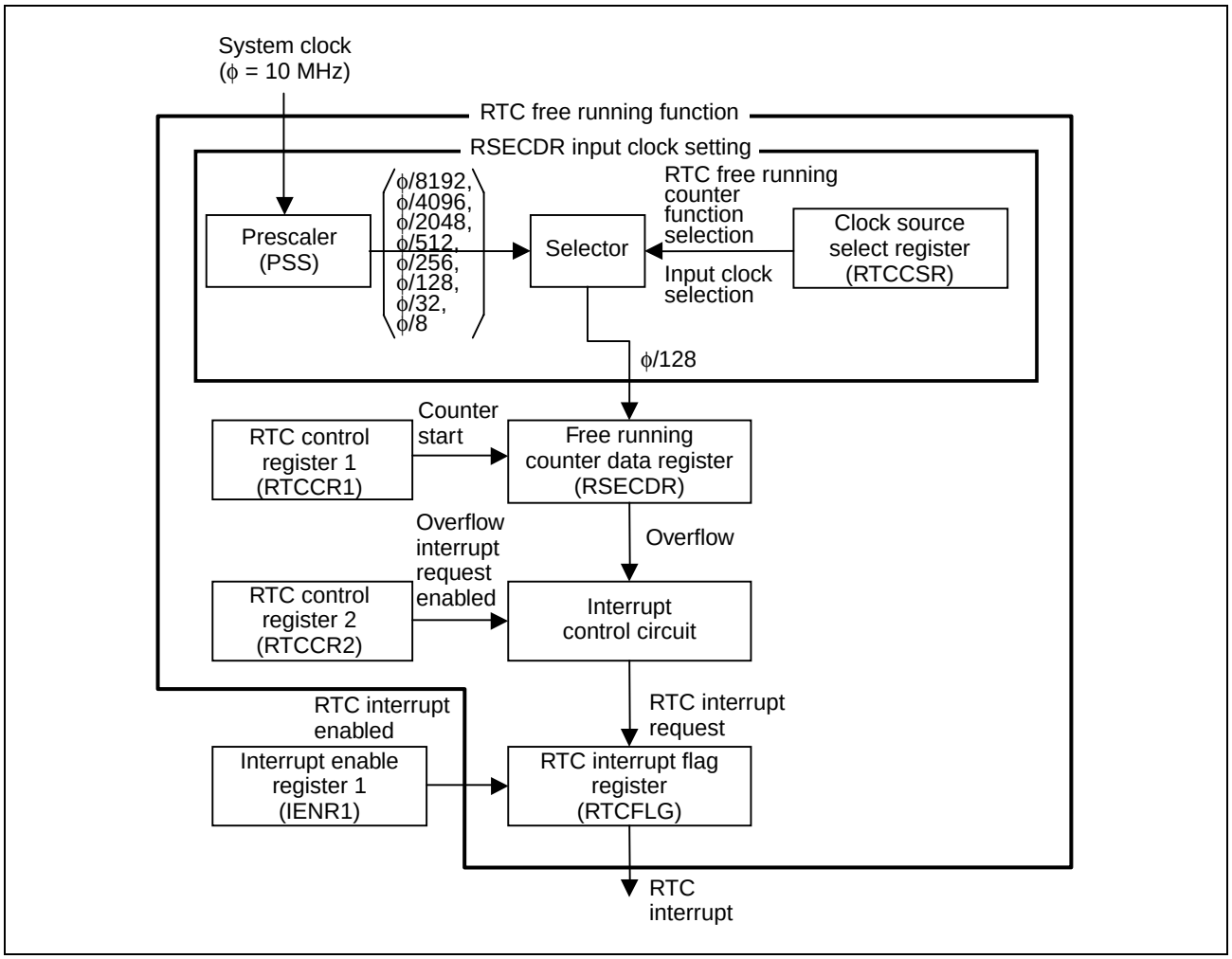


Figure 1 Block Diagram of RTC Free running Counter

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, counting up is performed by using the RTC free running counter function.

Table 1 Assignment of Functions

Elements	Description
RTCFLG	Free running counter overflow interrupt flag
RSECDR	RTC free running counter
RTCCR1	Start/stop of RTC operation and reset control
RTCCR2	RTC free running counter overflow interrupt enabling
RTCCSR	Selects ϕ/128 as clock source
IENR1	RTC interrupt request enabling

3. Principles of Operation

- The principles of operation of this sample task are illustrated in figure 2. Using the hardware and software processing shown in figure 2, 8-bit counter (cnt) is incremented using the RTC free running counter function.
- When RSEDCR overflows when cnt is H'FF, cnt is initialized to H'00 and continues counting.

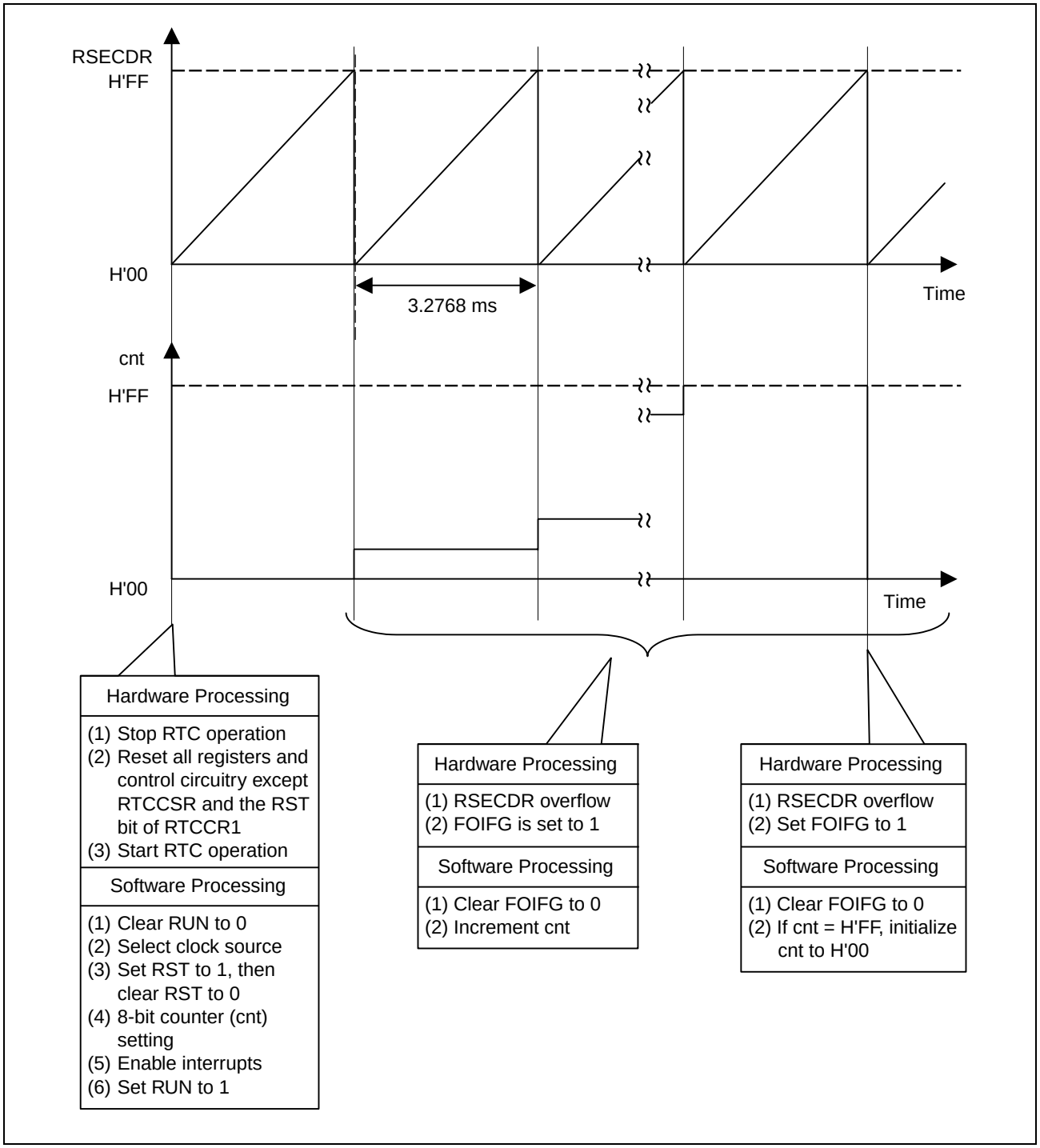


Figure 2 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
Main	RTC free running counter function initial setting and interrupt enabling
Rtcint	RTC free running counter overflow interrupt processing, FOIFG flag clearing, 8-bit counter incrementing and initialization

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- RTCFLG RTC interrupt flag register Address: H'F067

Bit	Bit Name	Set Value	R/W	Description
7	FOIFG	0	R/W*	[Setting condition] When free running counter overflows [Clearing condition] When 0 is written to FOIFG when FOIFG = 1

Note: * Only a 0 can be written to clear the flag.

- RSEDCR Second data register/free running counter data register Address: H'F068

  Function: Functions as the 8-bit counter read register during operation as a free running counter.

  Set value: H'00

  R/W: R

- RTCCR1 RTC control register 1 Address: H'F06C

Bit	Bit Name	Set Value	R/W	Description
7	RUN	1	R/W	RTC operation start 0: Stops RTC operation 1: Starts RTC operation
4	RST	0	R/W	Reset 0: Normal operation 1: Resets all registers and control circuitry except RTCCSR and this bit. After being set to 1, this bit must always be cleared to 0.

- RTCCR2 RTC control register 2 Address: H'F06D

Bit	Bit Name	Set Value	R/W	Description
7	FOIE	1	R/W	Free running counter overflow interrupt enable 0: Disables an overflow interrupt 1: Enables an overflow interrupt

- RTCCSR Clock source select register Address: H'F06F

Bit	Bit Name	Set Value	R/W	Description
3	RCS3	0	R/W	Clock source selection
2	RCS2	0	R/W	0000: ϕ/8 ..... Free running counter operation
1	RCS1	1	R/W	0001: ϕ/32 ..... Free running counter operation
0	RCS0	0	R/W	0010: ϕ/128 ..... Free running counter operation
				0011: ϕ/256 ..... Free running counter operation
				0100: ϕ/512 ..... Free running counter operation
				0101: ϕ/2048 ..... Free running counter operation
				0110: ϕ/4096 ..... Free running counter operation
				0111: ϕ/8192 ..... Free running counter operation
				1xxx: 32.768 kHz ..... RTC operation

Note: x: Don't care

- IENR1 Interrupt enable register 1 Address: H'FFF3

Bit	Bit Name	Set Value	R/W	Description
7	IENRTC	1	R/W	RTC interrupt request enable The RTC interrupt request is enabled when this bit is set to 1.

4.4 RAM Usage

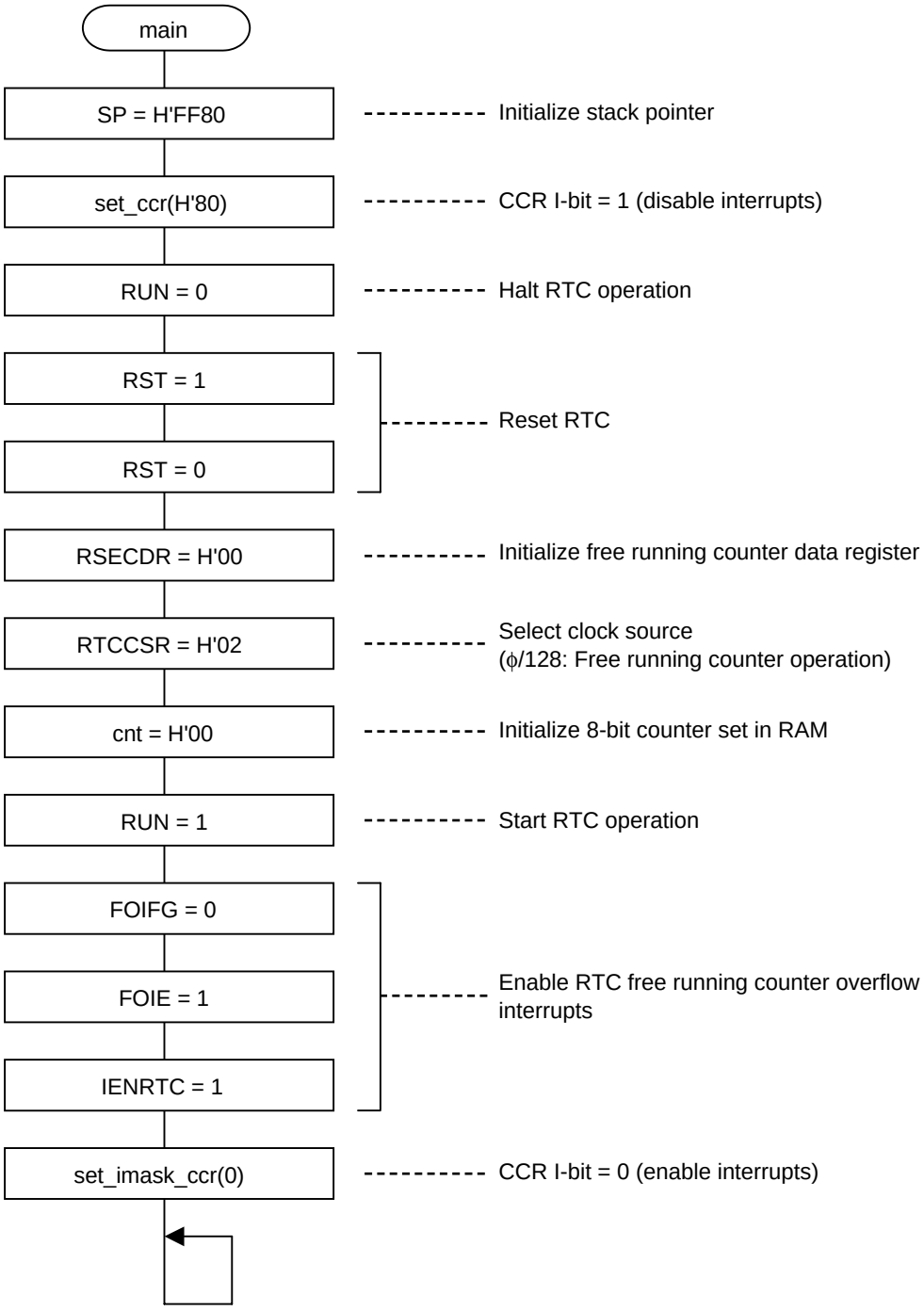
Table 3 describes RAM usage in this sample task.

Table 3 RAM Usage

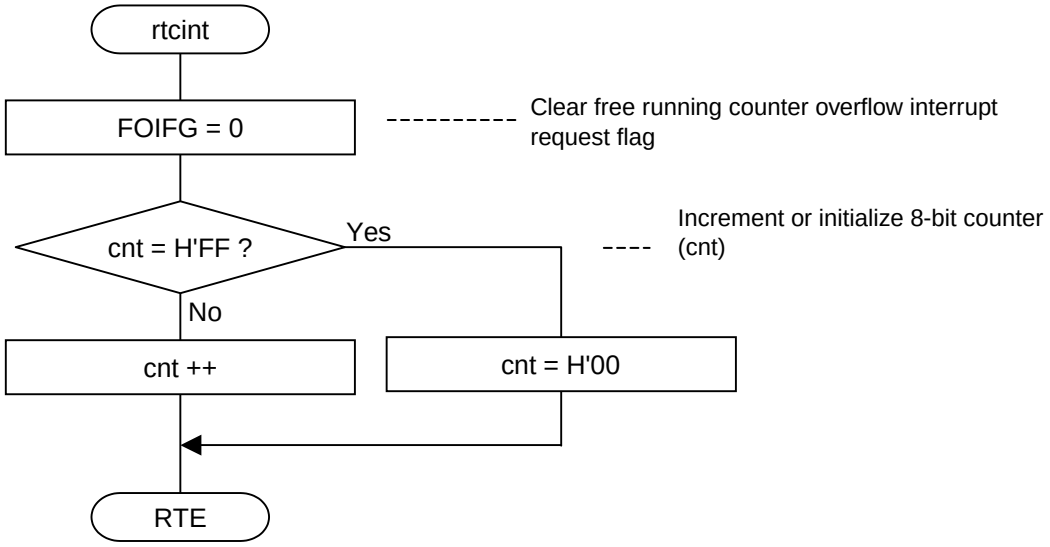
Label	Description	Amount of Memory Used	Used in
cnt	8-bit counter	1 byte	main, rtcint

5. Flowcharts

5.1 main



5.2 rtcint



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'0034
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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