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H8SX Family

Generating One-Shot Pulse Output

Introduction

A one-shot pulse is output in synchronization with the falling edge of an external signal. The delay and pulse width of the one-shot pulse can be set as desired.

Target Device

H8SX/1653

Contents

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3. Description of Modules Used 3
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1. Specifications

(1) A one-shot pulse is output in synchronization with the falling edge of an external signal as shown in figure 1.
(2) The buffer operation of TPU_3, and transfer function of the DMAC are used.
(3) Any desired value can be set for the delay and pulse width.

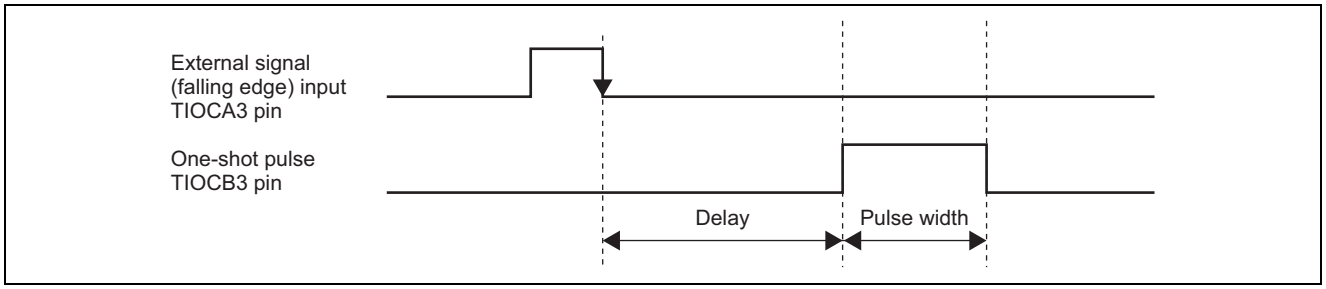


Figure 1 One-Shot Pulse Output

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 2 Section Setting

Address	Section Name	Description
H'001000	P	Program area

3. Description of Modules Used

In this sample task, a one-shot pulse is output by using DMAC_0, DMAC_1, and TPU_3. Figure 2 shows a block diagram of the on-chip modules used in this sample task. In this sample task, the following functions of the TPU and DMAC modules are used to produce one-shot pulse output.

- TPU_3
  - Transfers the buffer register contents to the general registers on compare match (buffer operation).
  - Separately specifies general registers to function as output compare/input capture registers.
  - Clears the counter by input capture.
- DMAC_0
  - Activates the DMAC by input capture of the TPU.
  - Transfers the value for one-shot pulse delay to TGRB_3.
- DMAC_1
  - Activates the DMAC by input capture of the TPU.
  - Transfers the compare match output setting value to TIORH_3.

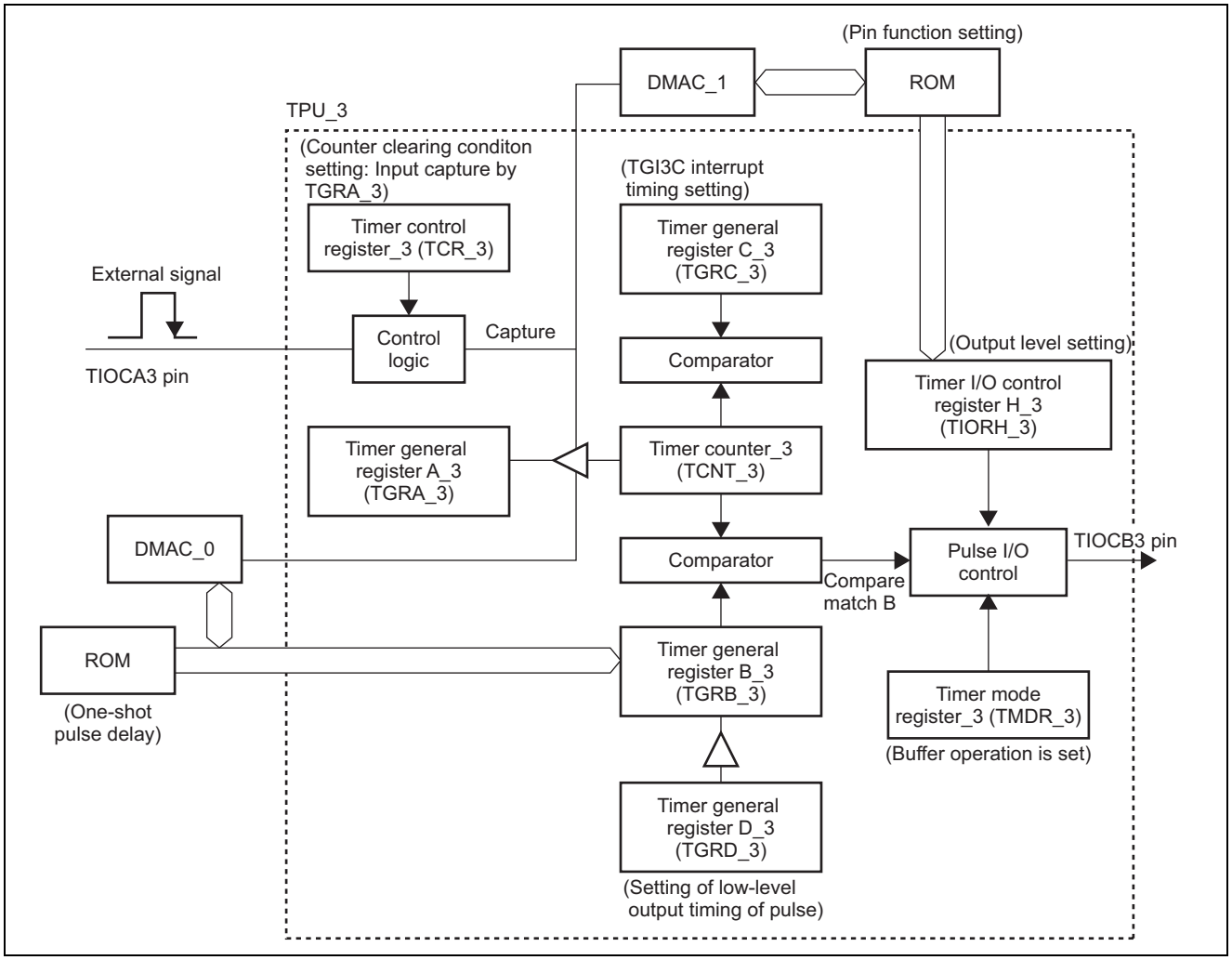


Figure 2 Block Diagram of One-Shot Pulse Output

4. Description of Operation

4.1 Description of One-Shot Pulse Output Operation

Figure 3 illustrates the operation of one-shot pulse output. The hardware processing and software processing of figure 3 are explained in table 3.

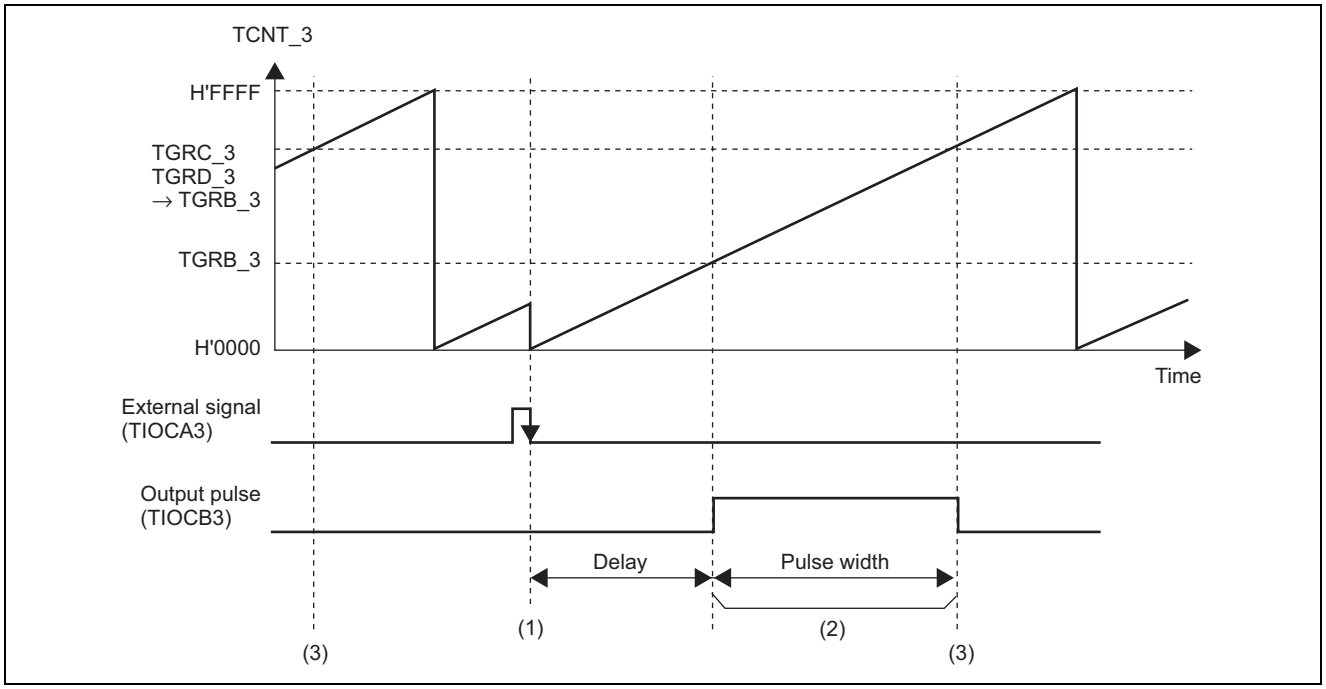


Figure 3 Operation of One-Shot Pulse Output

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	• TPU_3 (a) Generate input capture A. (b) Output initial output value "0" from the TIOCB0 pin. • DMAC_0 (a) Transfer the one-shot pulse delay value to TGRB_3. • DMAC_1 (a) Transfer the pin function setting to TIORH_3.	No processing
(2)	• TPU_3 (a) Generate compare match B. (b) Buffer operation: Transfer the TGRD_3 contents to TGRB_3. (c) Toggle the output on the TIOCB3 pin.	No processing
(3)	• TPU_3 (a) Generate compare match C. (b) Generate a TGI3C interrupt.	• TGI3C interrupt processing (a) Disable the TIOCB3 pin output. (b) Clear the status flag.

4.2 One-Shot Pulse Delay Timing

Figure 4 shows the delay timing of the one-shot pulse output. The delay time from the falling edge on the TIOCA3 pin till the point at which the TIOCB3 pin goes high is the value obtained by adding three clock cycles to the TGRB_3 setting, as shown in figure 4.

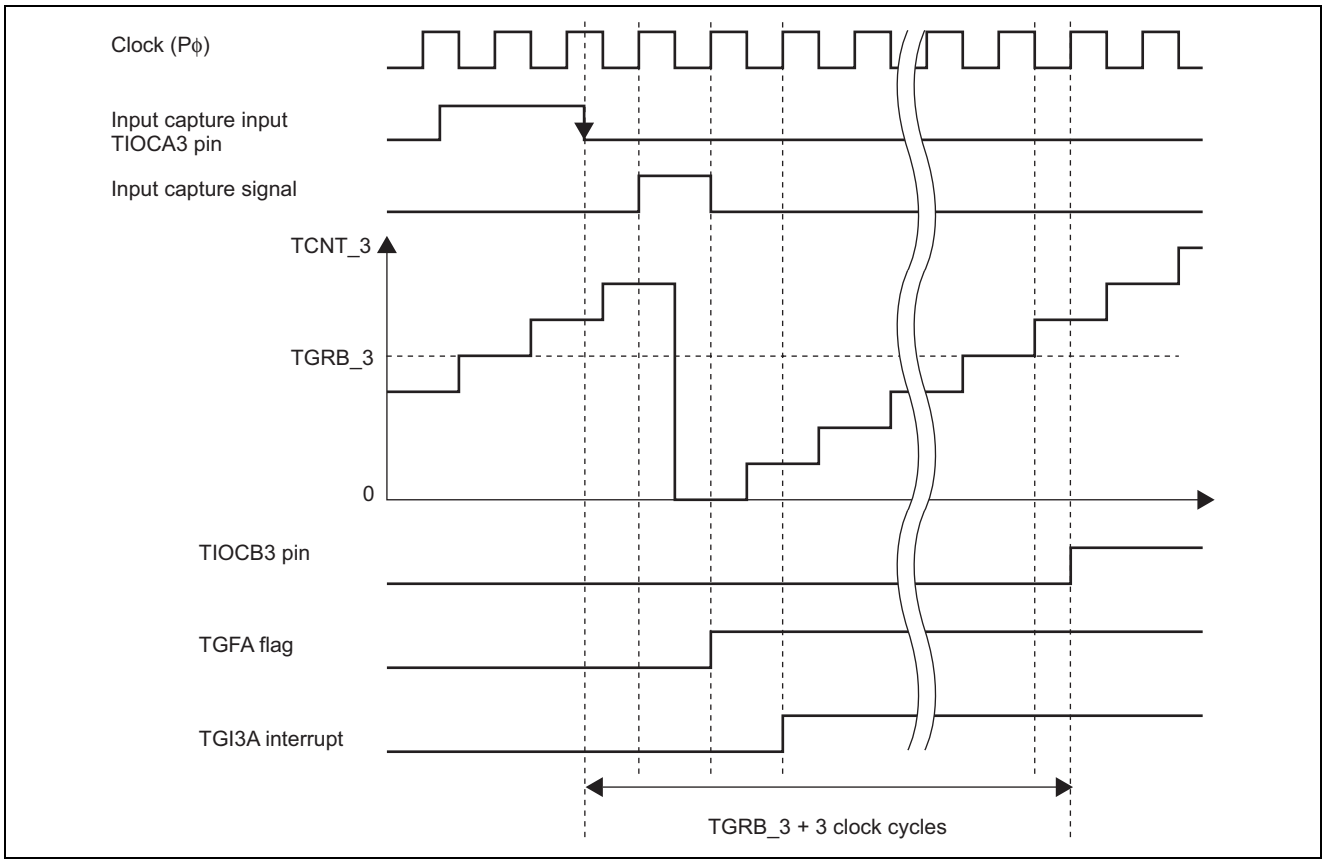


Figure 4 One-Shot Pulse Delay Timing

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR, configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Sets the values for delay and pulse width in TGRB_3 and TGRD_3, respectively, and sets the TGI3C interrupt timing in TGRC_3 to outputs a one-shot pulse.
tgi3c_int	Input capture interrupt handling routine

5.2 Vector Table

Table 5 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main
TPU_3 TGI3C	103	H'0001A0	tgi3c_int

5.3 ROM Usage

Table 6 ROM Usage

Type	Variable Name	Setting	Description	Used In
unsigned short	set_dly	H'8000	Delay time Specifies the delay for a one-shot pulse. Delay = (set_dly + 3)/(Pϕ/1) = (H'8000 + 3)/24 MHz ≈ 2048 [μs] Taking into consideration the DMAC operation time, operation is possible in the following range. H'0020 < set_dly < H'FFFE	main
unsigned short	one_rst	H'9000	Low-Level Output Timing Specifies the low-level output timing of a one-shot pulse. The pulse width is given as below from set_dly and one_rst. Pulse width = (one_rst − set_dly)/(Pϕ/1) = (H'9000 − H'8000)/24 MHz = 256 [μs] Taking into consideration the DMAC operation time, operation is possible in the following ranges. one_rst − set_dly ≥ 1 H'0021 < one_rst < H'FFFF	main
unsigned char	io_cntr	H'39	Pin Function Setting This setting is transferred to TIORH_3 to specify the functions of the TIOCA3 and TIOCB3 pins. • Toggle output from the TIOCA3 pin on compare match with TGRB_3 • Input capture takes place on the falling edge of the TIOCB3 pin	main

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

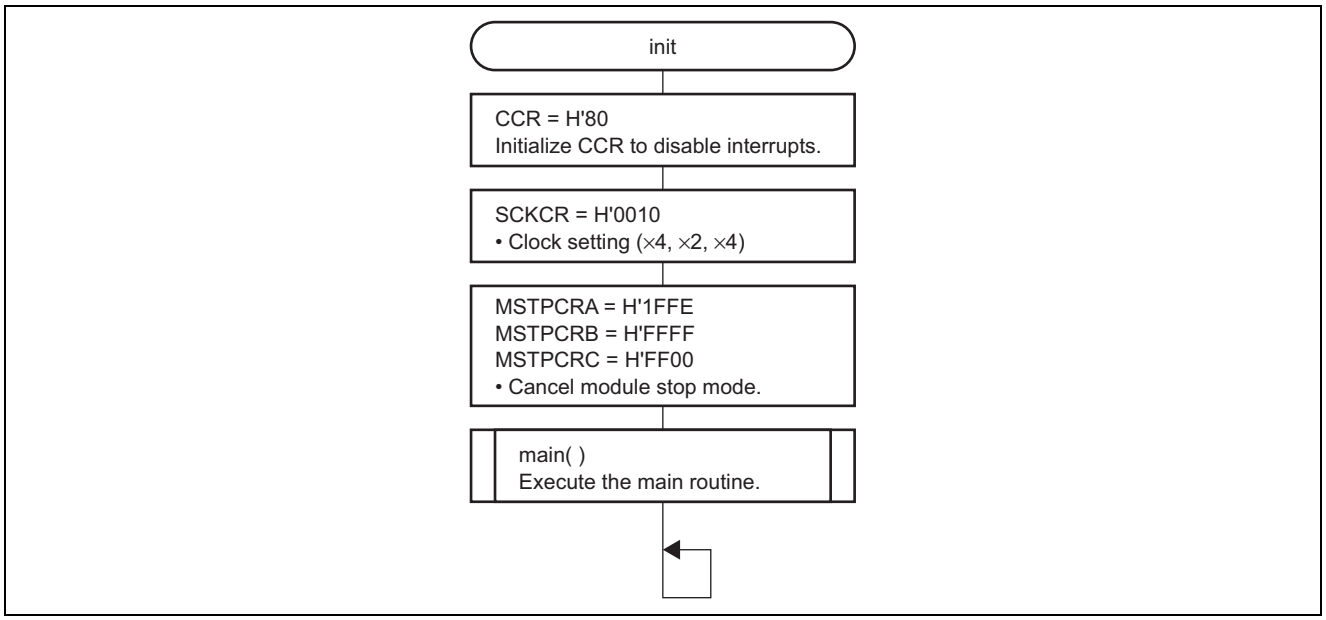
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart



5.4.2 main Function

(1) Functional overview

Main routine which sets the delay and pulse width for the one-shot pulse.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 2 input buffer control register (P2ICR) Address: H'FFFB91

Bit	Bit Name	Setting	R/W	Function
1	P21ICR	1	R/W	0: Input buffer of the P21 pin is disabled and the input signal is fixed high 1: Input buffer of the P21 pin is enabled and the pin state is reflected in the corresponding on-chip peripheral module

- Port function control register 9 (PFCR9) Address: H'FFFBC9

Bit	Bit Name	Setting	R/W	Function
5	TPUMS3A	1	R/W	TPU I/O Pin Multiplex Function Select Selects the TIOCA3 function. 0: Specifies P21 as the output compare output or input capture input pin 1: Specifies P23 as the input capture input pin and P21 as the output compare output pin

- DMA source address register_0 (DSAR_0) Address: H'FFFC00
  Function: Specifies the source address of data transfer.
  Setting: &set_dly
- DMA destination address register_0 (DDAR_0) Address: H'FFFC04
  Function: Specifies the destination address of data transfer.
  Setting: &TGRB_3
- DMA transfer count register_0 (DTCR_0) Address: H'FFFC0C
  Function: Specifies the size of the data for transfer. When DTCR_0 = H'00000000, the DMAC operates in free-running mode.
  Setting: H'00000000
- DMA block size register_0 (DBSR_0) Address: H'FFFC10
  Function: Specifies the repeat size in repeat transfer mode. When DBSR_0 = H'00000000, the repeat size is the maximum value.
  Setting: H'00000000

- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

Bit	Bit Name	Setting	Function	
31	DTE	0	R/W	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: Transfer end interrupt by the transfer counter has not been requested 1: Transfer end interrupt by the transfer counter has been requested
15	DTSZ1	0	R/W	Data Access Size 1, 0
14	DTSZ0	1	R/W	01: Data is accessed in word units (16 bits)
13	MDS1	1	R/W	Transfer Mode Select 1, 0
12	MDS0	0	R/W	10: Repeat transfer mode
7	DTF1	1	R/W	Data Transfer Factor 1, 0
6	DTF0	0	R/W	10: DMAC is activated by an on-chip module interrupt
5	DTA	1	R/W	Data Transfer Acknowledge This bit is valid in DMA transfer triggered by an on-chip module interrupt. This bit enables or disables automatic clearing of the interrupt source flag selected by DMRSR. 0: Clearing of the on-chip module interrupt source flag in DMA transfer is disabled. Since the interrupt source is not cleared in DMA transfer, it should be cleared by the CPU or DTC transfer. 1: Clearing of on-chip module interrupt source flag in DMA transfer is enabled. The interrupt source is cleared in DMA transfer, and an interrupt request is not generated to the CPU or DTC.

Note: * Only 0 can be written to clear the flag after reading the flag as 1.

- DMA address control register_0 (DACR_0) Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Function
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
26	RPTIE	0	R/W	Repeat Size End Interrupt Enable 0: Disables repeat size end interrupts 1: Enables repeat size end interrupts
25	ARS1	0	R/W	Area Select 1, 0
24	ARS0	0	R/W	00: Select the source address side as the repeat area in repeat transfer mode
21	SAT1	0	R/W	Source Address Update Mode 1, 0
20	SAT0	0	R/W	00: Source address is fixed
17	DAT1	0	R/W	Destination Address Update Mode 1, 0
16	DAT0	0	R/W	00: Destination address is fixed

- DMA source address register_1 (DSAR_1) Address: H'FFFC20
  Function: Specifies the source address of data transfer.
  Setting: &io_cntr

- DMA destination address register_1 (DDAR_1) Address: H'FFFC24
  Function: Specifies the destination address of data transfer.
  Setting: &TIORH_3

- DMA transfer count register_1 (DTCR_1) Address: H'FFFC2C
  Function: Specifies the size of data for transfer. When DTCR_1 = H'00000000, the DMAC operates in free-running mode.
  Setting: H'00000000

- DMA block size register_1 (DBSR_1) Address: H'FFFC30
  Function: Specifies the repeat size in repeat transfer mode. When DBSR_1 = H'00000000, the repeat size is the maximum value.
  Setting: H'00000000

- DMA mode control register_1 (DMDR_1) Address: H'FFFC34

Bit	Bit Name	Setting	Function	
31	DTE	0	R/W	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: Transfer end interrupt by the transfer counter has not been requested 1: Transfer end interrupt by the transfer counter has been requested
15	DTSZ1	0	R/W	Data Access Size 1, 0
14	DTSZ0	0	R/W	00: Data is accessed in byte units (8 bits)
13	MDS1	1	R/W	Transfer Mode Select 1, 0
12	MDS0	0	R/W	10: Repeat transfer mode
7	DTF1	1	R/W	Data Transfer Factor 1, 0
6	DTF0	0	R/W	10: DMAC is activated by an on-chip module interrupt
5	DTA	1	R/W	Data Transfer Acknowledge This bit is valid in DMA transfer triggered by an on-chip module interrupt. This bit enables or disables automatic clearing of the interrupt source flag selected by DMRSR. 0: Clearing of the on-chip module interrupt source flag in DMA transfer is disabled. Since the interrupt source is not cleared in DMA transfer, it should be cleared by the CPU or DTC transfer. 1: Clearing of on-chip module interrupt source flag in DMA transfer is enabled. The interrupt source is cleared in DMA transfer, and an interrupt request is not generated to the CPU or DTC.

Note: * Only 0 can be written to clear the flag after reading the flag as 1.

- DMA address control register_1 (DACR_1) Address: H'FFFC38

Bit	Bit Name	Setting	R/W	Function
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
26	RPTIE	0	R/W	Repeat Size End Interrupt Enable 0: Disables repeat size end interrupts 1: Enables repeat size end interrupts
25	ARS1	0	R/W	Area Select 1, 0
24	ARS0	0	R/W	00: Select the source address side as the repeat area in repeat transfer mode
21	SAT1	0	R/W	Source Address Update Mode 1, 0
20	SAT0	0	R/W	00: Source address is fixed
17	DAT1	0	R/W	Destination Address Update Mode 1, 0
16	DAT0	0	R/W	00: Destination address is fixed

- DMA module request select register_0 (DMRSR_0) Address: H'FFFD20

  Function: 8-bit readable/writable register that specifies the on-chip module interrupt source. In this sample task, the on-chip module interrupt source is set as the TGI3A interrupt (101) of TPU_3.

  Setting: 101

- DMA module request select register_1 (DMRSR_1) Address: H'FFFD21

  Function: 8-bit readable/writable register that specifies the on-chip module interrupt source. In this sample task, the on-chip module interrupt source is set as the TGI3A interrupt (101) of TPU_3.

  Setting: 101

- Port 2 data register (P2DR) Address: H'FFFF51

Bit	Bit Name	Setting	R/W	Function
0	P20DR	0	R/W	0: P20 pin is low 1: P20 pin is high

- Port 2 data direction register (P2DDR) Address: H'FFFB81

Bit	Bit Name	Setting	R/W	Function
0	P20DDR	1	R/W	0: P20 pin functions as an input pin 1: P20 pin functions as an output pin

- Timer start register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	0	R/W	These bits start or stop the operation of the corresponding TCNT.
3	CST3	1	R/W	
2	CST2	0	R/W	0: Stops counting by TCNT_5 to TCNT_0
1	CST1	0	R/W	1: Starts counting by TCNT_5 to TCNT_0
0	CST0	0	R/W	

- Timer control register_3 (TCR_3) Address: H'FFFFF0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT_3 counter clearing condition.
5	CCLR0	1	R/W	001: TCNT_3 cleared by TGRA_3 compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT_3 counter clock.
0	TPSC0	0	R/W	000: Internal clock Pϕ/1

- Timer mode register_3 (TMDR_3) Address: H'FFFFF1

Bit	Bit Name	Setting	R/W	Function
5	BFB	0	R/W	Buffer Operation B Specifies whether TGRB is to operate normally, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare does not take place. 0: TGRB operates normally 1: TGRB is used together with TGRD for buffer operation

- Timer I/O control register H_3 (TIORH_3) Address: H'FFFFF2

Bit	Bit Name	Setting	R/W	Function
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	These bits specify the function of the TIOCB3 pin.
5	IOB1	0	R/W	When TGRB_3 functions as an output compare register:
4	IOB0	0	R/W	0000: Output disabled
3	IOA3	1	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of the TIOCA3 pin.
1	IOA1	0	R/W	When TGRA_3 functions as an input capture register:
0	IOA0	1	R/W	1001: Input capture is performed on the falling edge of the capture input signal from the TIOCB3 pin

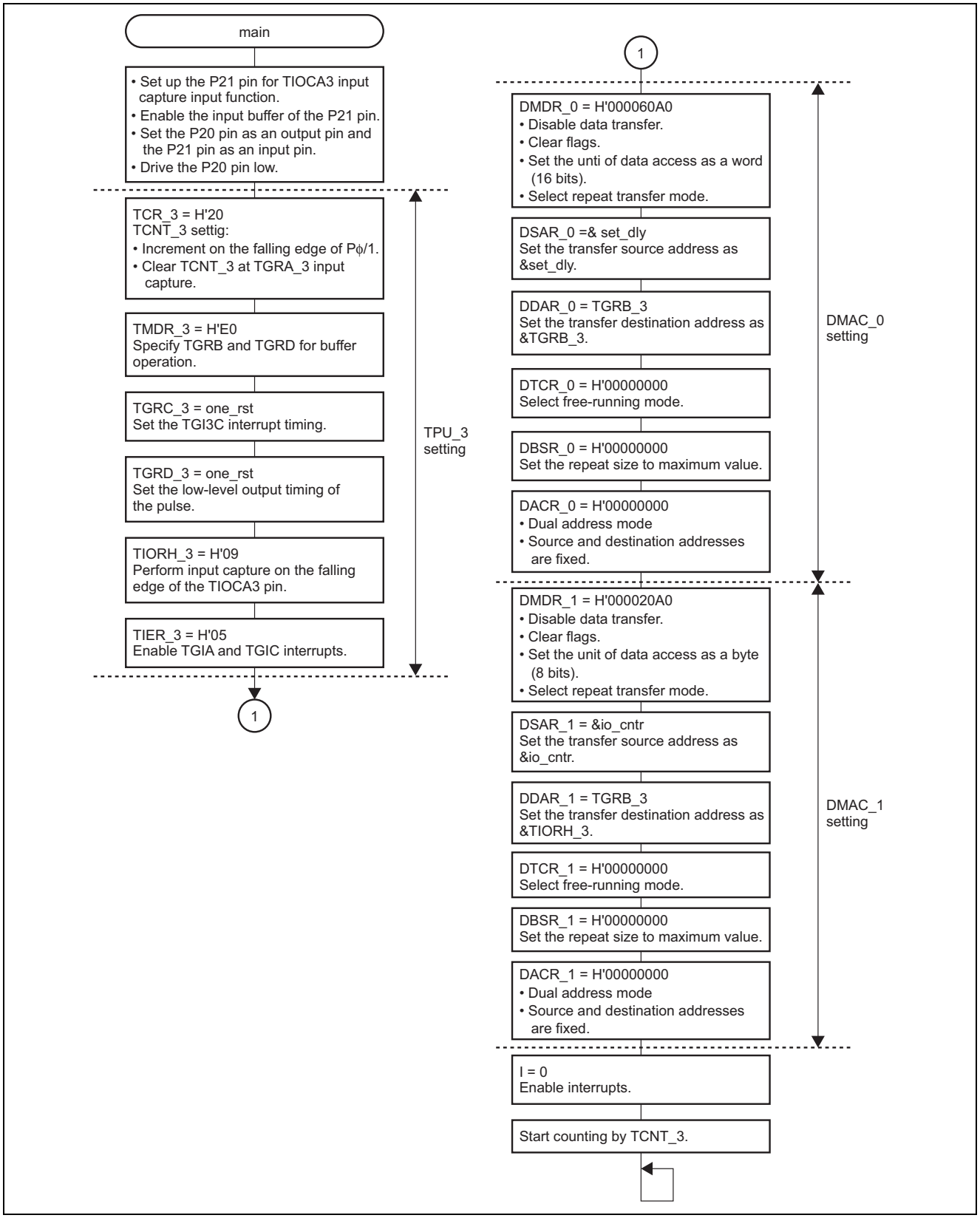
- Timer interrupt enable register_3 (TIER_3) Address: H'FFFFF4

Bit	Bit Name	Setting	R/W	Function
2	TGIEC	1	R/W	TGR Interrupt Enable C Enables or disables interrupt requests (TGIC) by the TGFC bit when the TGFC bit in TSR is set to 1. 0: Interrupt requests (TGIC) by TGFC bit is disabled 1: Interrupt requests (TGIC) by TGFC bit is enabled
0	TGIEA	1	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit is disabled 1: Interrupt requests (TGIA) by TGFA bit is enabled

- Timer general register C_3 (TGRC_3) Address: H'FFFFFC
  Function: Used as an output compare register. Sets the TGI3C interrupt timing.
  Setting: one_rst

- Timer general register D_3 (TGRD_3) Address: H'FFFFFE
  Function: Used as an output compare register. Sets the low-level output timing of the pulse.
  Setting: one_rst

(5) Flowchart


main
• Set up the P21 pin for TIOCA3 input capture input function.
• Enable the input buffer of the P21 pin.
• Set the P20 pin as an output pin and the P21 pin as an input pin.
• Drive the P20 pin low.
TCR_3 = H'20
TCNT_3 settig:
• Increment on the falling edge of Pϕ/1.
• Clear TCNT_3 at TGRA_3 input capture.
TMDR_3 = H'E0
Specify TGRB and TGRD for buffer operation.
TGRC_3 = one_rst
Set the TGI3C interrupt timing.
TGRD_3 = one_rst
Set the low-level output timing of the pulse.
TIORH_3 = H'09
Perform input capture on the falling edge of the TIOCA3 pin.
TIER_3 = H'05
Enable TGIA and TGIC interrupts.
TPU_3 setting
1
1
DMDR_0 = H'000060A0
• Disable data transfer.
• Clear flags.
• Set the unti of data access as a word (16 bits).
• Select repeat transfer mode.
DSAR_0 =& set_dly
Set the transfer source address as &set_dly.
DDAR_0 = TGRB_3
Set the transfer destination address as &TGRB_3.
DTCR_0 = H'00000000
Select free-running mode.
DBSR_0 = H'00000000
Set the repeat size to maximum value.
DACR_0 = H'00000000
• Dual address mode
• Source and destination addresses are fixed.
DMAC_0 setting
DMDR_1 = H'000020A0
• Disable data transfer.
• Clear flags.
• Set the unit of data access as a byte (8 bits).
• Select repeat transfer mode.
DSAR_1 = &io_cntr
Set the transfer source address as &io_cntr.
DDAR_1 = TGRB_3
Set the transfer destination address as &TIORH_3.
DTCR_1 = H'00000000
Select free-running mode.
DBSR_1 = H'00000000
Set the repeat size to maximum value.
DACR_1 = H'00000000
• Dual address mode
• Source and destination addresses are fixed.
DMAC_1 setting
I = 0
Enable interrupts.
Start counting by TCNT_3.

5.4.3 tgi3c_int Function

(1) Functional overview

TGI3C interrupt processing

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer I/O control register H_3 (TIORH_3) Address: H'FFFFF2

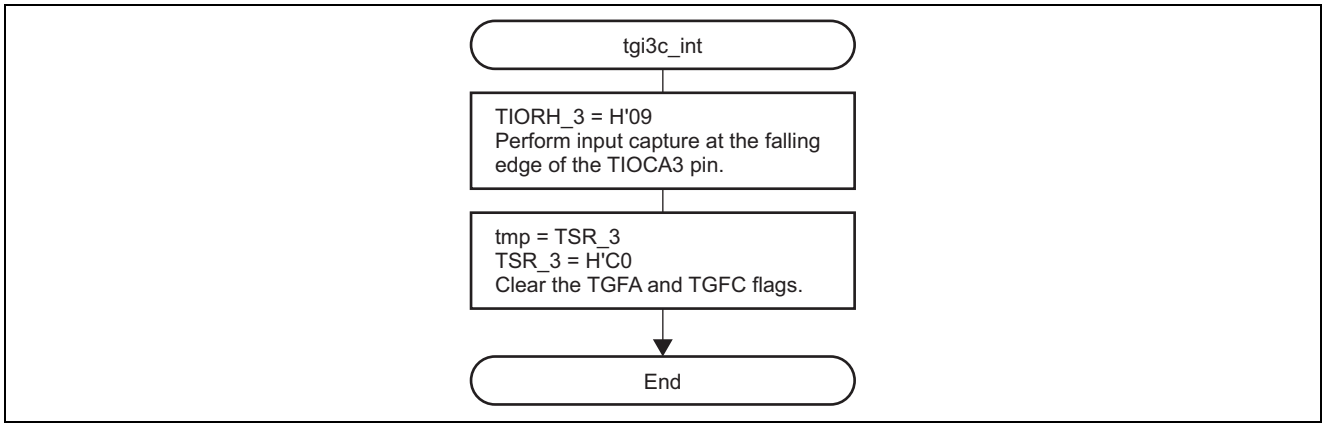
Bit	Bit Name	Setting	R/W	Function
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	These bits specify the function of the TIOCB3 pin.
5	IOB1	0	R/W	When TGRB_3 functions as an output compare register:
4	IOB0	0	R/W	0000: Output disabled
3	IOA3	1	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of the TIOCA3 pin.
1	IOA1	0	R/W	When TGRA_3 functions as an input capture register:
0	IOA0	1	R/W	1001: Input capture is performed on the falling edge of the TIOCB3 pin

- Timer status register_3 (TSR_3) Address: H'FFFFF5

Bit	Bit Name	Setting	R/W	Function
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C When TGRC functions as an output compare register: [Setting condition] • When TCNT_3 = TGRC_3 [Clearing condition] • When 0 is written to TGFC after reading TGFC = 1
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA functions as an input capture register: [Setting condition] • When the TCNT_3 value is transferred to TGRA_3 driven by the input capture signal [Clearing conditions] • When the DMAC is activated by a TGIA interrupt while the DTA bit in DMDR of the DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1

Note: * Only 0 can be written to clear the flag.

(5) Flowchart


tgi3c_int
TIORH_3 = H'09
Perform input capture at the falling edge of the TIOCA3 pin.
tmp = TSR_3
TSR_3 = H'C0
Clear the TGFA and TGFC flags.
End

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		Description	
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