

G.722 on μ PD7701x

The ITU-T Recommendation G.722 describes an audio codec that provides high-quality digital speech coding with a signal bandwidth of 50 Hz to 7 kHz and a data transmission rate of 64 kbits/s. Moreover, a data and signalling channel can be operated with a bit rate of 8 kbits/s or 16 kbits/s.

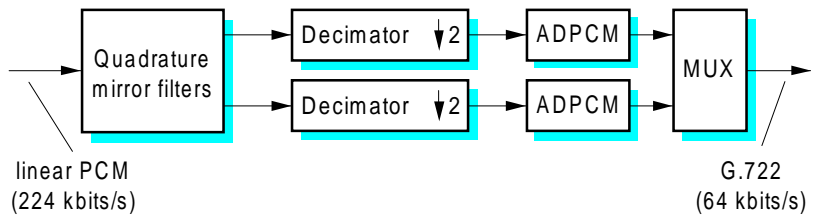
NEC's μ PD7701x 16-bit fixed point DSP family needs only 23% of the available time load for realising a full duplex G.722 codec. This gives the user the advantage to implement additional functions or to combine several codecs in one single low cost, low power device.

Introduction to ITU-T Rec. G.722

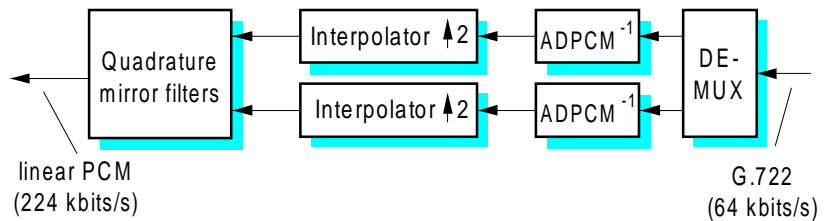
The G.722 coding algorithm uses sub-band adaptive differential pulse code modulation (SB-ADPCM) for coding an audio signal with a bandwidth of 7 kHz, which is sampled at 16 kHz with 14-bit resolution. G.722 reduces the data transmission rate from 224 kbits/s to 64 kbits/s.

In the encoder a quadrature mirror filter is used to split the input signal into two sub-bands of 0 to 4 kHz and 4 to 8 kHz respectively. The reduced bandwidth allows downsampling by 2 in each sub-band. An adaptive differential PCM is applied in every sub-band, thus leading to two codewords, a 6-bit codeword in the lower sub-band and a 2-bit codeword in the upper one. Both codewords are combined and the resulting octets are transmitted at a rate of 8000 octets/s, thus yielding 64 kbits/s. The quantiser stepsize is adapted in 8 kHz intervals.

The decoding process consists of inverse quantisation of the codewords and reconstruction of the sub-band signals using adaptive prediction.



G.722 encoder



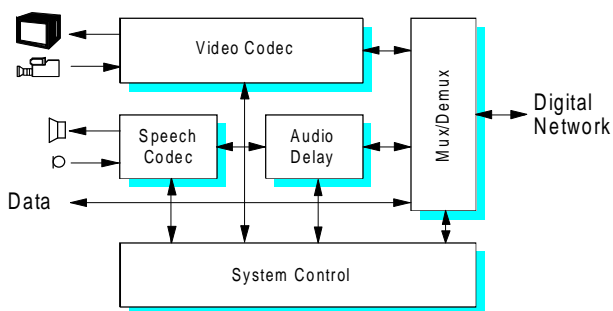
G.722 decoder

After upsampling a 24-coefficient quadrature mirror filter reconstructs the linear PCM signal from the lower and higher sub-band signals.

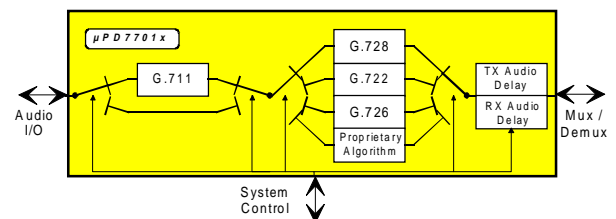
Application areas

The following list shows some typical application areas for G.722:

Videophone: The strictly simplified block diagram of a videophone is shown below. The audio and video codec are important and



complex blocks of such a videophone. Depending on the transmission rate that is available on the digital network different compression algorithms can be selected in the audio codec. For high-quality wide-band coding the G.722 can be used.



ISDN: The G.722 algorithm permits high quality digital speech transmission in an integrated services digital network. The potential applications comprise high end feature phones and public broadcast reporting systems.

Multipoint conference systems are another promising application field for G.722 speech coding.

Features and Options

The G.722 implementation on NEC's μ PD7701x family combines the processing power of this family with the flexibility of a general purpose DSP. Additional functions as well as the optimisation of I/O configuration can be implemented according to the user's requirements. The following list shows the features of NEC's G.722 modules:

- Testprogram for testing decoder and encoder separately against ITU-T testpattern available
- G.722 object code fully relocatable in the DSP-memory
- G.722 encoder and decoder source code for μ PD7701x family available
- No external memory required
- Three G.722 decoding modes selectable: As a G.722 channel may also carry up to 16 kbits/s

How to use G.722 on μ PD7701x

From the programmer's point of view the G.722 software consists of four modules: the actual encoder and decoder

- G722_encoder, G722_decoder

and two initialisation modules

- G722_encoder_init, G722_decoder_init

which have to be used prior to running the encoder/decoder. The modules are activated via

signalling and user information, there are three modes of operation.

Mode 1 for 64 kbits/s speech transmission

Mode 2 for 56 kbits/s speech transmission
+ 8 kbits/s user- and control information

Mode 3 for 48 kbits/s speech transmission
+ 16 kbits/s user- and control information

- Delay line implementation for synchronisation of audio- and video signals in video systems possible
- Easy combination of G.722 modules with G.728 and G.711 ITU-T Recommendation compliant modules. These modules are also available from NEC.
- I/O interface optimising: The I/O timing as well the data protocol can be changed according to the user's requirements.

Processor and System Requirements

The computational load for encoder and decoder is listed in the following table. The worst case processor time load for full duplex G.722 processing is 23%. The free timeload can be used for power reduction (software controlled power save mode) or for implementation of additional features as for example up- and down sampling filters or other codec algorithms.

	Time load Mips	Program memory (32 bit)	Data RAM (16 bit)	Data ROM (16 bit)
G.722 Encoder	3.98	524	80	340
G.722 Decoder	3.7	513	82	
G.722 Full Duplex	7.68	1037	162	

How to get G.722 on μ PD7701x

The complete μ PD7701x software in form of the assembler source can be obtained from NEC. A Programmer's Manual describes in detail the programs and provides information how to suit them to certain requirements. For evaluation purposes the package is completed with some test S/W for verification of the G.722 implementation against the G.722 ITU-T test sequences on the debugger board IE-77016-PC,

equipped with a DSP module IE-77016-CM-EM6

or similar. Moreover NEC guides with intensive support to suit the μ PD7701x program to special needs for S/W as well as H/W implementation.

An alternative is the usage of the μ PD77523, a μ PD7701x based firmware chip that provides full duplex G.722 functionality as well as G.728 and G.711. It is the easiest way to come to a working G.722 system.

		μPD77016	μPD77015	μPD77017	μPD77018	7701x core*
Internal memory	Instruction ROM	-	4k x 32 bit	12k x 32 bit	24k x 32 bit	user defined
	Instruction RAM	1.5k x 32 bit	256 x 32 bit			user defined
	Data ROM	-	2 x 2k x 16 bit	2 x 4k x 16 bit	2 x 12k x 16 bit	user defined
	Data RAM	2 x 2k x 16 bit	2 x 1k x 16 bit	2 x 2k x 16 bit	2 x 3k x 16 bit	user defined
External memory	Instr. memory	48k x 32 bit	-			-
	Data memory	2 x 48k x 16 bit	2 x 16k x 16 bit			user defined
ALU bus		40 bit				
Multiplier		16 x 16 --> 31 bit				
Barrelshifter		40 bit				
Working registers		8 x 40 bit				
Loop/repeat counter		1 repeat counter / 4 nested loop counters				
Host I/F, max. throughput		8 bit, 8.25 Mbytes/s				user defined
Serial I/F, max. throughput		2 SIOs, 8/16 bit, 16.6 Mbits/s				user defined
Interrupts		4 external, 6 internal				10
Min. instruction cycle time		30 ns				< 20 ns
Master clock for 33 Mips		66 MHz	33, 16.5, 8.25, 4.125 MHz (int. PLL)			t.b.f.
Power supply		+5 V	+3 V			
Typical power dissipation		0.7 W	90 mW	120 mW	150 mW	t.b.f.
Power down modes		0.4 W (halt)	3 mW (halt), 3 μW (stop)			t.b.f.
Packages		160 QFP	100 TQFP			user defined

*under development

μPD7701x Family Overview

NECs new μPD7701x 16-bit fixed point DSP family offers one of the most advanced architectures on the market. Their members are characterised by a clearly structured Harvard architecture with:

- Two identical memory banks (X, Y) with separate address computation units
- Powerful 16/40-bit arithmetic operation unit
- Program control unit with high performance loop counter
- Memory-mapped peripherals
- JTAG-based on-chip debug hardware and boundary scan facilities

All μPD7701x devices share the same core architecture but have a couple of device specific characteristics which are summarised in the table.

Devices under development will extend this family with a DSP core and more variants in performance/speed.

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